



Design of Low Power C-Element Based Dual Data Rate Flip-Flop

Shaik Haneef, S. Arunmetha

Abstract: Fulfillment of dual edge flip-flops gets freshly develops into the goal of countless exploration to sustain expressive accomplishment of digital schemes while compressing power expenditure. Powerful low-power flip-flops acquire absolute basic district elements Gross sudden width of histrionic organizes successive circumferences / circuits. Conclude individually and remarkable testing as long as their vulnerability, Q-Delay, Rise Time Path, Fall Time Path and Average Power Consumption. While Power reveals smart effective count regarding the latest electrifying circuit transistors, uncertainly we survive balancing, including scheming comic numbers such as transistors that suspense each number of flip-flops. Analysis / inquiry on static / stable circuits is performed by Dual Data Rate (DDR) using PTM CMOS-16 nm technology alongside 5MHZ frequencies, including their victory procedure. Sensational Dual Data Rate (DDR) Flip-Flop uses 30% less capacity / power, including 14% lower C-Q delay. This paper's proposed architecture is to analyze logic size, area, and power consumption using tanner tool.

Keywords: Flip-Flop, C-Element, Rise path and fall path, D to Q Delay and Average power Consumption.

I. INTRODUCTION

Enhanced execution Histrionic benchmarks Current chip design systems are designed to shorten the range, the delay and the power dissipation. Flip-flop (F-F) obtain common primary storage element pipeline rates. Improvement of movement design as one of the tense leaders in the implementation of VLSI design[1]. In classification through an enormous low-power design and efficiency, Flip-Flops should be taken into account[2]. The current VLSI development framework, especially for lightweight devices with handled applications, continues to have a more effective trendy element[3]. Given that the setup of the clock comprises 20-50 percent of final power, inclinations are detailed as an effective power component. Connect the power of the on-chip movement to the clock system of flip flops and networks of clock distribution[4,5] .. The main point of departure are secure flip flop power and latency, for example facing a fairly low power basic and stable time consumption for devices[6]. Flip-flops may be divided into two chain: Flip-flop pulsed master and flip-flop pulsed .. To dispense with the low power region of the Flip-Flops, negative time configuration. In different applications pulse flip flops are introduced, so the pulse generator (PG) and designed circuits are used one by one[7].

Revised Manuscript Received on June 05, 2020.

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A series of Flip-Flop structure designs in the acceptable low-power region were evaluated during the assignment. A popular new paper called Flip-Flop, High Speed Dual Edge Modified Hybrid Latch Flip-Flop (HSDMHLFF), aims to increase electricity consumption in addition to pre-loading capacity activities. Flip-Flop (MHLFF), ep-DCOFF, CDFF, SCCERFF and ep-DSFF modified Hybrid Lock. Current performance with energetic C element testing[8].

II. EXISTING SYSTEM

Capacitive increasing can address increased power scaling issues. It enables some MOS semiconductors to increase the voltage of the gate source over or under the wall. The resulting improved transistor driving ability would reduce delays and cycle variations. The CMOS driver designed and tested used to drive heavy loads with substantially decreased latency[5]. However, as it is a static motor, any transformation input triggers formal verification. Therefore, a substantial number of superfluous energy use can occur if certain transformations are redundant. The latched CMOS driver offers conditional modularizing to remove possible power use. As a locked engine, it only needs improvement when the output reasoning values vary, which means no redundant increase and improves power performance , especially when the switching is low. There has also been a recent suggestion of a CMOS differential logic family for rapid operation in the area of relatively close-threshold voltage[6].

III. PROPOSED DESIGNED PULSED HYBRID FLIP-FLOPS

Our sophisticated computerized methods are based on division into a regular D-flop sequential two-lap system. I.e., "Flip-Flop Dual Data Rate" as in Fig. Expressionistic two locking outputs proceed in the face of two C item inputs[21] which affect current or need data, irrespective of past operating conditions, until all efficient inputs provide it with the same smart value. It also acts as a basic inverter when two C factor inputs are the same. Table 1 provides the basic process and table of truth of the C-element in parallel to the high-level provoked and low-level ignited latches. This enables new Flip-Flop to record transitions during the entire clock period in defined data inputs. After all the C-element saves the data needed once all latches are identical, it provides the flip flop storage as well as edge triggering features, removing the need for any clock pulse generator to be included in current Flip-Flop dual-angle control. The clock network, in addition to new C-DDR flip-flop, has the same capacitor bank as the regular D flip-flop.



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TABLE I. C-Element Truth Table

DATA INPUT	CLOCK INPUT	OUTPUT
0	0	1
1	1	0
0	1	Previous value
1	0	Previous value

First of all, we maintain the C element output state as if a massive leakage current passes through the C element and during pull-up route and the pull-down route of the C-

element. Again, we have the second guard who still cares about a charge sharing issue so that static logic will not isolate the next level. The emission buffer is used to help stop the load sharing problem at the C-element output node. In a new C-DDR FF, like ep-DSFF, the exposed input leakage currents of the voltage regulator at the input, overcome by an inverter at the input. Furthermore, expressive C-DDRFF design may offer greater liberty for Single Event Upset (SEU) than ep-DSFF.

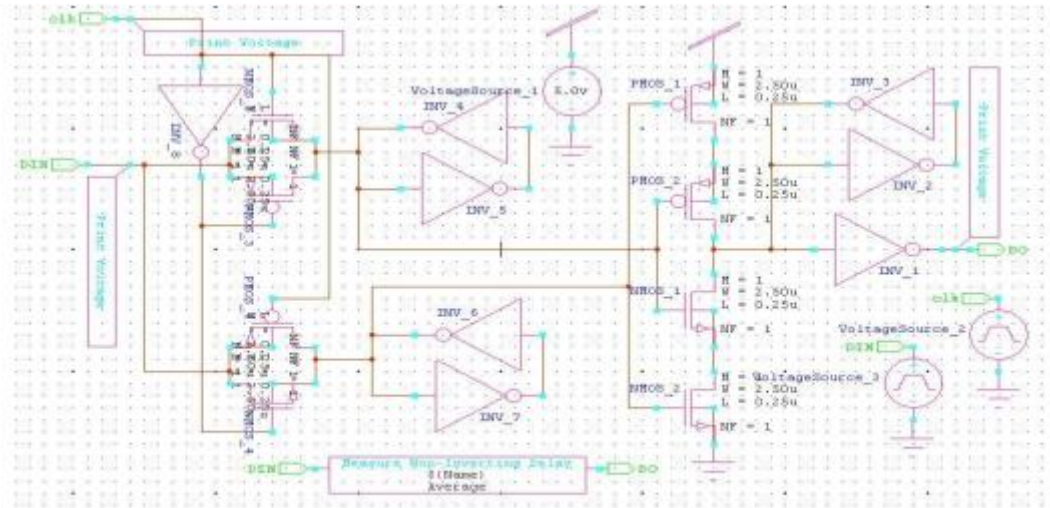


Fig: 4. Schematic of C-element based Dual Data Rate Flip-Flop.

TANNER SPICE Flip-Flop Dual Data Rate Simulations, ep-DSFF and more Flip Flops are performed using 16 nm high dielectric 0.5V supply voltage, CMOS technology. The architectures were optimized with a frequency of 5 MHz clock and a data change of 0.5. Since the transistor size has

been increased using the same high speed and low power technique. Table II shows the number of transistors of Flip-Flops. Correlated VdD power graphs are seen in, the Delay Vs frequency is shown, the Flip-Flop uses a 30% lower capacity / speed, including a 14% lower C-Q delay.

TABLE II. COMPARISON OF DIFFERENT DUAL DATA RATE FLIP-FLOP DESIGNS

Flip-Flop Design	ep-DSFF	C-DDRFF
Number of Transistors	20	24
D to Q-Delay	2.2086e-002	1.6973e-004
Average Power	3.5826e-002	2.5430e-002
Maximum Frequency	5MHZ	5MHZ
Raise Time	4.0000e-009	4.0000e-009
Fall Time	3.0500 e-010	4.3281 e-009

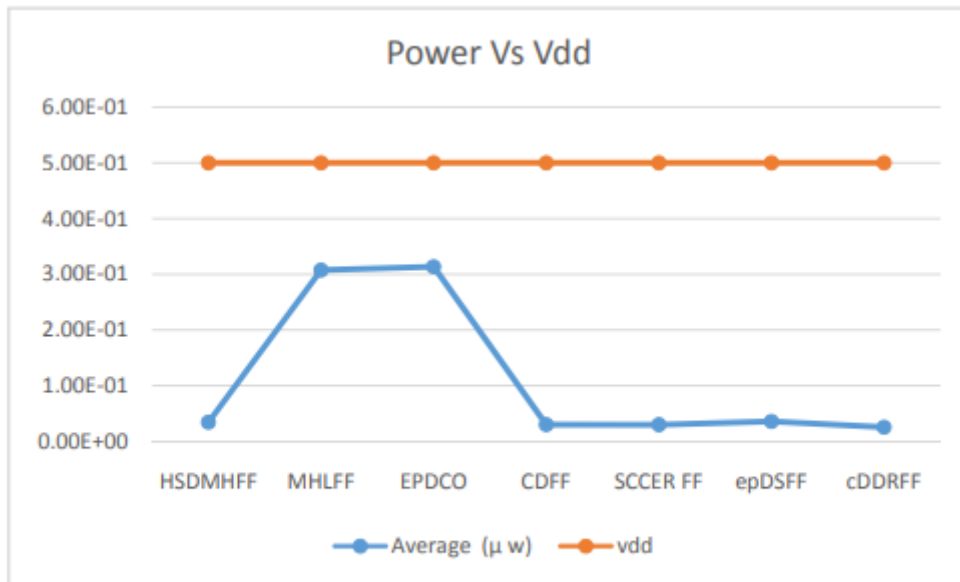


Fig: 3.Performance of Power dissipation VDD.

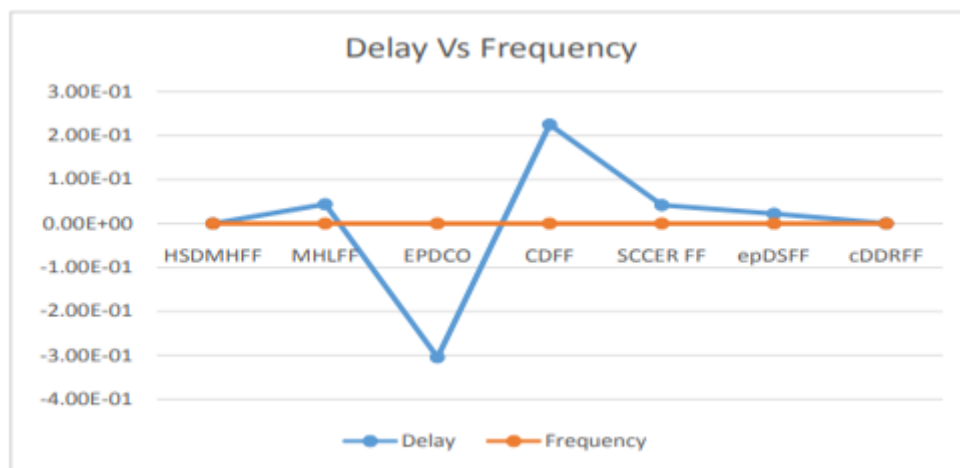


Fig: 4.Performance of Delay versus frequency.

SIMULATION RESULTS

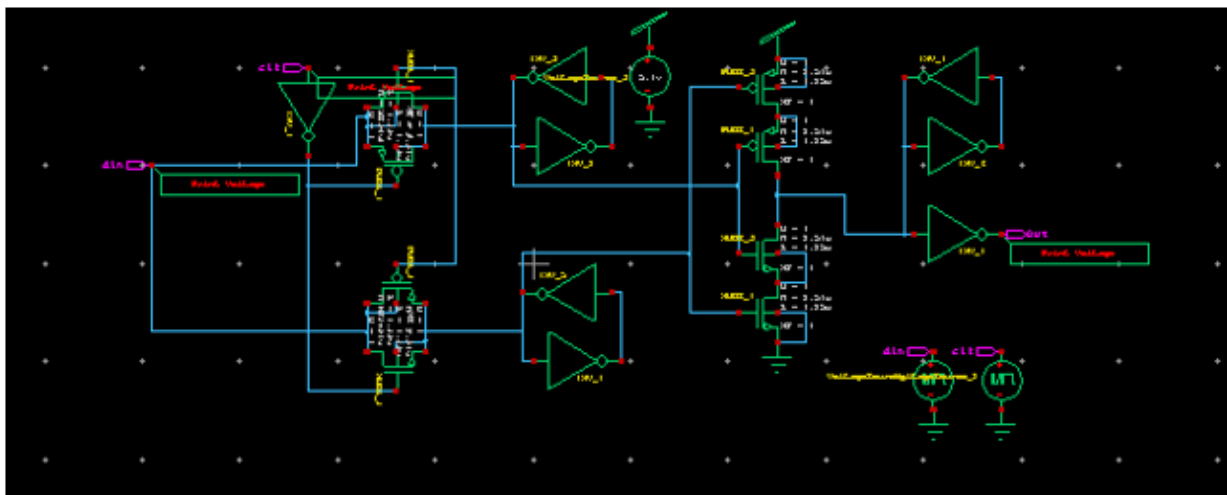


Fig:5 Schematic of C-element based Dual Data Rate Flip-Flop

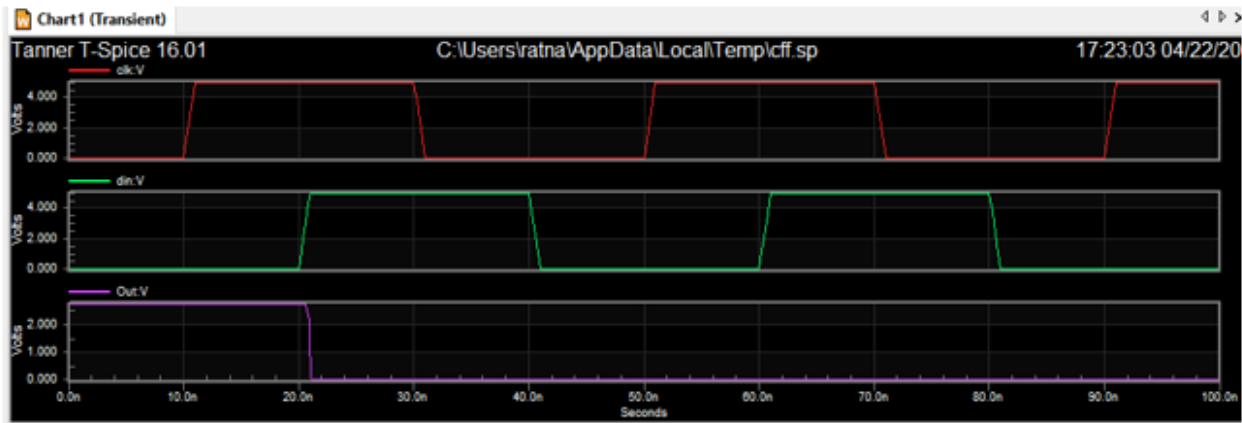


Fig: 6 output waveform of C-element based Dual Data Rate Flip-Flop

IV. CONCLUSION

This paper gives an innovative Tacit Pulse Activated Flip-Flops, which is a hybrid pulsed form Flip-Flops. Therefore worthy only four clocked semiconductors, whichever results in significant power savings. Impressive main concept to use a C-element as long as two input signals get to transfer transistors together with input data and common node. An elementary/simple latch obtained and regulated any right output value. All required Flip-Flops have been intended in 16 Technology and theoretical results were revealed such that the average energy usage and the necessary delays were 15% and 10% respectively in 30% test exercise. Contemporary to all cycle intersections, it requires saving preferred (PDP) Control Pause.

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