Design and Implementation of N-Point FFT Processor for MIMO-OFDM Systems using Radix-N

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***Abstract:** This paper presents Single-path Delay Feedback (SDF) architecture for implementing Fast Fourier Transform (FFT) for Multiple-Input Multiple-Output Orthogonal Frequency Division Frequency Multiplexing (MIMO-OFDM). The architecture of Single-path Delay Feedback and memory scheduling are the basic concepts used to implement the FFT processor with variable length. Depending on the SDF architecture, we implement the FFT processor-based design which is proposed in this paper. In this paper, we use MIMO-OFDM high data rates, high efficiency and high throughput. In this paper, we use radix-4 algorithm to implement the sequence because the speed of the operation is high. The functionality verification and the synthesis are carried out by using XLINIX.14.2.*

***Keywords:** Single-Path Delay Feedback (SDF), Fast Fourier Transform (FFT), Multiple-Input Multiple-Output (MIMO), Orthogonal Frequency Division Multiplexing (OFDM), Radix-4.*

I. INTRODUCTION

Fast Fourier Transform (FFT) is mostly used for many applications. By using this, we easily evaluate the Discrete Fourier Transform (DFT). Among many communication applications digital signal processing is one which uses Fast Fourier Transform.

Decimation in time and Decimation in frequency are two different ways to perform Fast Fourier Transform. FFT is the main block in OFDM as it deals many operations to be done.

By using, MIMO the throughput elevated greatly when compared with existing systems. The lifetime of MIMO-OFDM systems is high while using in wireless The many applications come under the credit of OFDM are wired communication modems such as digital subscriber lines to wireless communication modems.communications. When we combine MIMO with OFDM, the issues are overcome upon each other. When FFT is combined with MIMO we get the results at high speed. By using the combination of MIMO-OFDM with FFT the results are getting a very fast manner, high reliability, high efficiency and high throughput. For these reasons we use a combination of FFT with MIMO-OFDM.

FFT architectures are different types. They are memory-based, cache memory, sequential, parallel, parallel iterative, array and pipelined architectures. Pipelined architectures helped in a better way for the implementation of FFT.

II. ANALYSIS LITERATURE

Fast Fourier Transform is the major block in the Orthogonal Frequency Division Multiplexing systems [5]. OFDM has assigned in a large range of applications from wired communication modems, such as digital subscriber lines to wireless-communication modems, like IEEE802.16 WiMAX or 3GPP Long Term Evaluation (LTE), to process baseband data [5].

Y.G.Li, J.H. Winters and N.R.Sollenberger proposed Multiple-Input Multiple-Output devices, data throughput can be elevated drastically [8]. Hence MIMO-OFDM systems feed data rate and reliability in wireless communication [8]. Without a proper design, the complexity of the FFT processor in MIMO systems increases linearly with the number of data streams [8].

B.G.Jo and M.H.Sunwoo proposed pipeline schemes are the architectures most widely adopted for the implementation of FFT [7]. From the memory access perspective, in-place memory updating schemes perform the computation in the three phases: writing in the inputs, updating intermediate values and reading out the results [7]. In the updating phase, the processor reuses the radix-r processor, such that a single radix-r butterfly is sufficient to complete N-point FFT computation [7]. However, it is non-overlapping characteristics that make the butterfly idle in-memory write and read phases overall process is lengthy [7].

T.S. Basha and others proposed high speed MDC architectures and memory scheduling are very much suitable

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for FFT processor in multiple input multiple output OFDM systems, because the constant multipliers are used to store the twiddle factors instead of ROM, which utilizes 100% area and reduces the delay [5].

III. RADIX-4 SDF

Pipelined architecture is also known as cascaded architecture and is used in most designs. The most commonly used pipelined architectures such as SDC, SDF, MDC and MDF. Pipelined architecture has many advantages compared to other architectures like simplicity, high throughput, fast, small area and energy-efficient implementation.

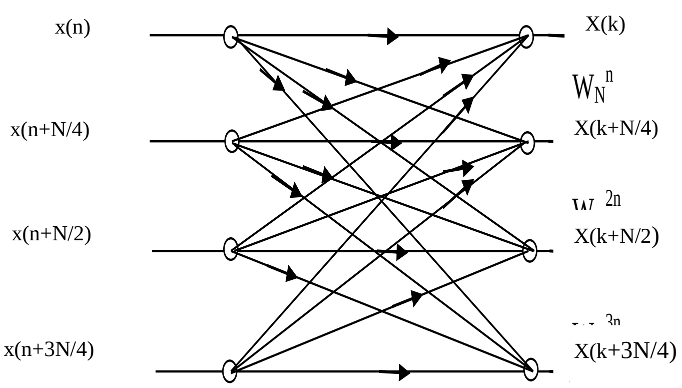


Fig 1 Radix-4 Butterfly Diagram

The Fig 1 represents the radix-4 butterfly diagram. It contains less number of computations compared to radix-2 algorithm. If we use radix-4 algorithm, the twiddle factors are decreased for this reason we choose radix-4 algorithm in this paper. Also these are the benefits for radix-4 algorithm.

By choosing this radix-4 algorithm, the hardware utilization is reduced and the complex multiplier is minimized. Radix-2 algorithm utilizes high power, is the major drawback. The fig 1 shows the basic butterfly diagram for radix-4, which is also used for long length of sequences.

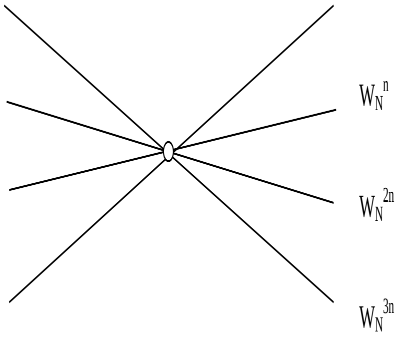


Fig 2 Equivalent graph for fig 1

In the name it is clearly, that it takes 4inputs and gives 4outputs. But for radix-2, it considers only 2 inputs and gives 2 outputs. In Radix-4, the every output comes out with the interconnection of all inputs. For example, the first output is comes out due to internal connection of remaining inputs along with main input. The internal operations are done at here only like multiplication, additions, and subtractions. The whole operation is mainly depends upon the twiddle factors. The twiddle factor contains exponent of product of some values like N, m etc. where N represents the number of stages, m is the stage index. Also we calculate the twiddle factor by using the combination of sin and cosin with some products which are discussed already in above.

Fig 2 is the equivalent graph for fig1. In this paper, we implement the FFT sequence by using a radix-4 algorithm. The results are very fast, it occupies less area compare radix-2 algorithm. In this paper, we proposed 16 point FFT sequence, for this sequence if we use the radix-2 complexity is increased, to reduce complexity we use the radix-4.

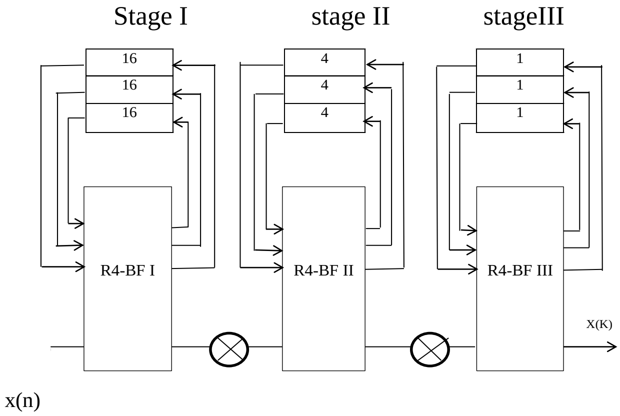


Fig 3 Block diagram for 16 points SDF

In Fig 3, we have 3 radix-4 butterflies. Here we consider a 16 point sequence, if we use the radix-2 algorithm the complexity will increase, for that reason we choose the radix-4 algorithm. The stages are found by using the 4^N, N represents the number of stages. For 16 point sequence we have used 3 radix-4 butterflies. Single path Delay Feedback (SDF), allows only a single bit at a time and remaining bits are feedback to the input. The main advantage is, there is no Intersymbol interference. The SDF is introduced to overcome the drawback present in the SDC. In SDC, there is no feedback due to this if the output has error we cannot change that. To overcome this drawback we introduce SDF. We also use multipliers; through this the output is sent to the next stage. At this multiplier the operations are performed.

The R4SDF is better than the R2SDF because, it operation performed highly and the results are out in fast manner. The R4SDF is not only used for small sequences, it also used for larges sequences. It is efficient technique compared to R2SDF. .

IV. RESULT AND DISCUSSION

A.Rtl Schematic:

The Fig 4 shows the RTL schematic for 16 point radix-4 SDF.

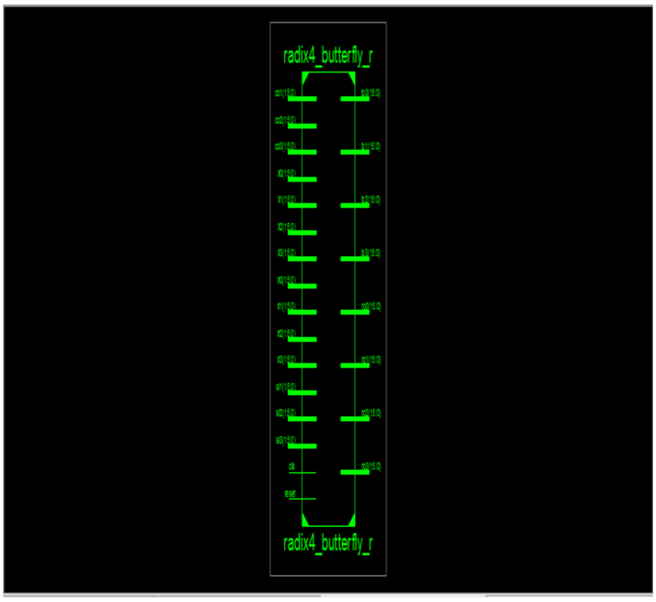
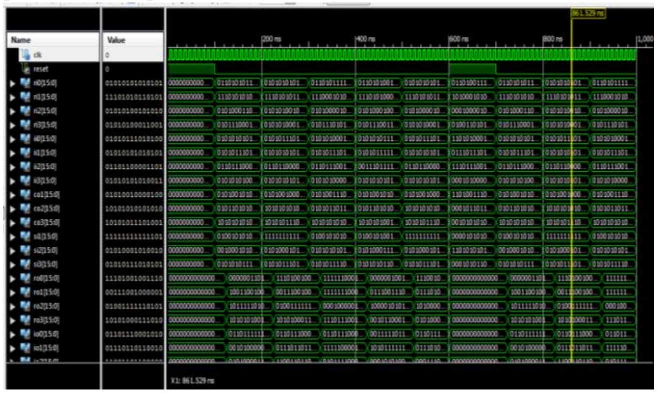


Fig 4 RTL Schematic for 16 points SDF FFT processor

B.Simulation Results:

The Fig 5 shows the simulation results for radix-4 16 point FFT sequence.



Name	Value
clk	0
reset	0
ri0[15:0]	0101010101010101
ri1[15:0]	1110101010110101
ri2[15:0]	0101010100101010
ri3[15:0]	0101010100011001
ii0[15:0]	0101011101010100
ii1[15:0]	0101010101010101
ii2[15:0]	0110110000001101
ii3[15:0]	0101010101010011
co1[15:0]	0101001000000100
co2[15:0]	1010101010101010
co3[15:0]	1010101110101001
si1[15:0]	1111111111111101
si2[15:0]	0101000101001010
si3[15:0]	0101011101010101
ro0[15:0]	1110100100111010
ro1[15:0]	0011100100000001
ro2[15:0]	0100111111110101
ro3[15:0]	1010100001110110
io0[15:0]	0110111000101010
io1[15:0]	0111011011001010

Fig 5 simulation results

C.Design Summary:

We utilize 768 registers along with 768 flipflops. For the synthesis we have to utilize the devices with the number of slices counts 1584 out of 165% and the number of flipflops is 848 out of 1920 with 44% and LUT's counts to 2392 out of 1920 with 124%. The I/O's we use 354 and bounded input-output will be 354 out of 66 with 536%. We use multi 18*18 input outputs 4 out of 4 with 100% and the generator clock is 1 out of 24 with 4%.

We require a 13.312ns clock period with a frequency of 75.119MHz and get the delay of 13.312ns with 31 levels of logic. The delay for logic is 6.531ns with 88.3% and 0.866ns with 11.7%. The total real-time to xst completion is 18.00s and the total CPU time to xst completion is 17.86s and the total memory usage is 251908Kb.

V. CONCLUSION

The proposed high-speed SDF architecture and memory scheduling are very much suitable for the FFT processor in multiple input multiple output OFDM system because the constant multipliers are used to store the twiddle factors, which uses less area and reduces the delay. Further we can improve this method by using mixed-radix we can reduce the computations and complexity and we will get the efficient results in the same as the radix-4.

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