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FPGA Implementation of Fault Tolerant Adder using Verilog for High Speed VLSI Architectures

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Abstract: ***The main objective is to detect and reduce the faults in full adder design using self checking and self repairing adder block. The rate of chip failure is directly proportional to chip density. This fault tolerant adder has high speed (Delay is 6.236ns) & implemented on FPGA Spartan 3 using XC3S50 device. The source code is written in verilog. In this design faults are identified and repaired using self checking and self repairing full adder methodologies.***

Index Terms**:** ***Fault Tolerance, VLSI, Full Adder, Self Checking, FPGA Spartan 3, Self Repairing, Xilinx ISE 14.7, Verilog.***

I. INTRODUCTION

Nowadays fault tolerant have been very crucial in the critical applications in which instant human action is not possible. These precarious applications popularly include defence surveillance, medical supervisory system space applications. These faults existence may lead to the failure of the functionality of such highly sensitive applications. As the technology is upgrading and developing, density of IC is also increasing which in turn minimizing the size of IC. The major effects that lead to transient faults in IC are cosmic rays, electromagnetic noises, power supply noise and cross talk. In addition to this technology scaling also holds major share in producing faults that may turn to be permanent faults too. Though the compact design is noble for minimizing, it will also lift up the chances of hardware failure in advanced processor

II. SELF CHECKING ADDER

The output for the carry & sum expressions of the full adder is shown in below

$$C_{out} = AB + BC_{in} + C_{in}A$$

$$Sum = A \oplus B \oplus C_{in}$$

The block diagram of self checking full adder is shown in fig.1. The faulty sum and carry both are different when the inputs all are equal to zero and all the inputs are equal to logic high. The both faulty sum and carry equal to one only when inputs A=0, B=1 and c=1. From the figure 1, if inputs A, B and C all zero, the outputs of each stage Sum=0, Cy=0, G1=0, G2=0, E0=1, Fc=0 and Fs=1. Similarly when all the inputs A, B and C are high or logic 1, Sum=1, Cy=1, G1=1, G2=1, E0=1, Fc=1 and Fs=0.

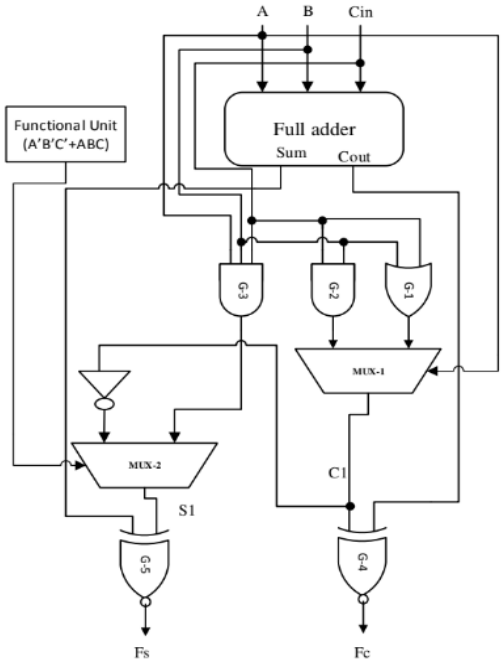

Fig.1 Self Checking Full Adder

A	B	C	SUM	CY	G1	G2	G3	EQ	FC	FS
0	0	0	0	0	0	0	0	1	0	1
0	0	1	1	0	1	0	0	0	1	0
0	1	0	1	0	1	0	0	0	1	0
0	1	1	0	1	1	1	0	0	1	1
1	0	0	1	0	0	0	0	0	1	0
1	0	1	0	1	1	0	0	0	0	1
1	1	0	0	1	1	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1	0

Table.1. Truth Table of Self checking full adder design

III. SELF REPAIRING FULL ADDER:

The block diagram of self repairing full adder is shown in figure 2. It consists of two 2:1 multiplexers, self checking adder.

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The control signals Carry fault and sum fault is connected to the multiplexers. In this design the stand by adder cells are not required. The operation is dependent on Fs and Fc given from the self checking full adder. Faults will not occurred in the sum, if Fs is equal to zero. If signal Fs is equal to one , it shows error or fault in the sum. If fault occurs in the sum, the inverter is used to remove the error or fault.

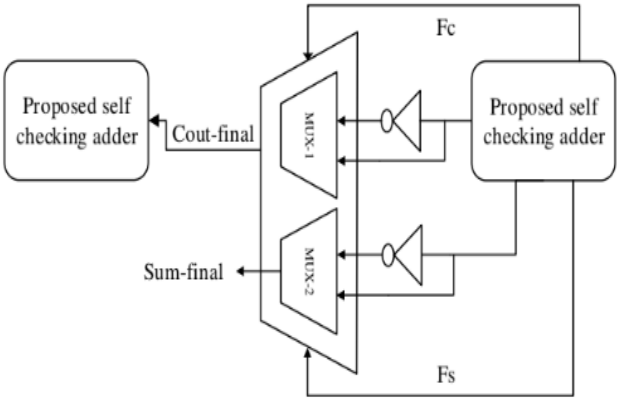

Fig 2. Self-repairing full adder

IV. SIMULATION & SYNTHESIS RESULTS

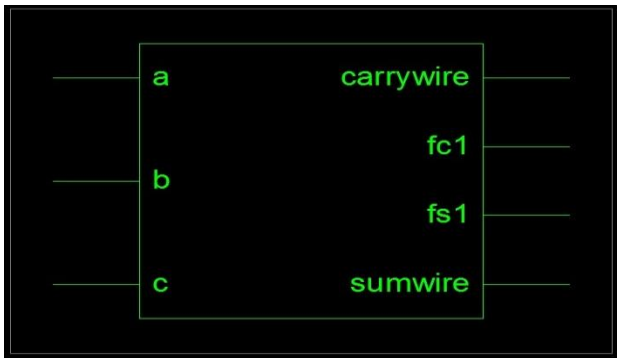

Fig 3. Top module of self checking Full Adder

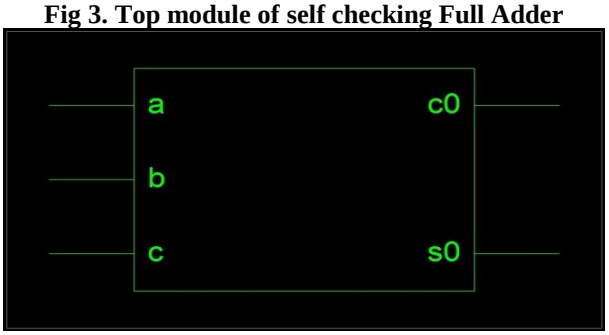

Fig4.Top module of self repairing Full Adder

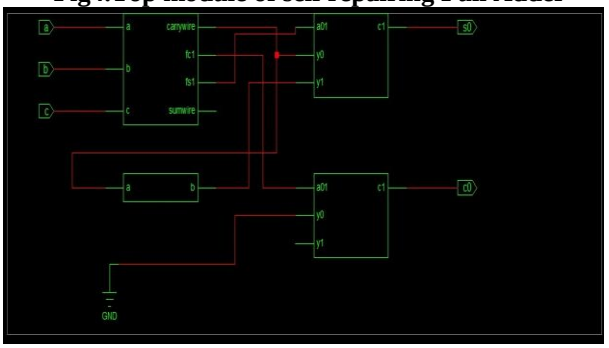

Fig 5. RTL Schematic Self checking Full Adder

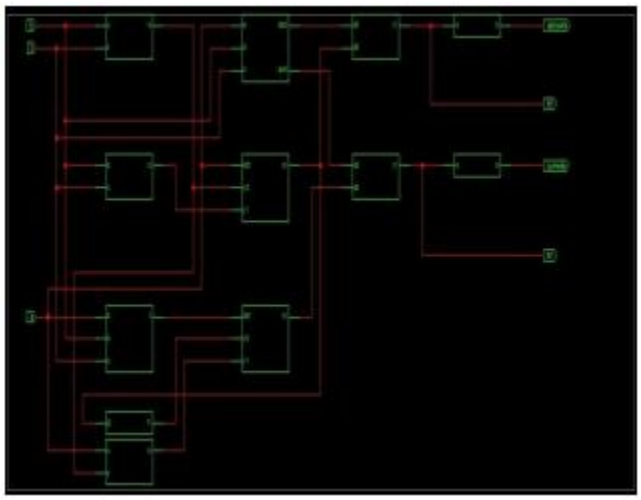

Fig 6.RTL Schematic of self repairing Full Adder

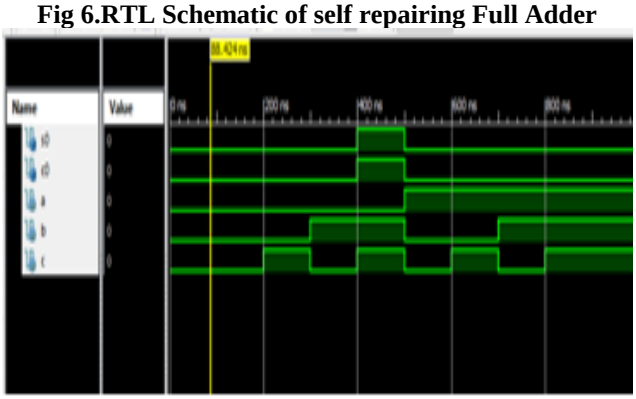

Fig 7. Simulation of Self Checking Full Adder

In the above fig. 7 the three inputs are A=0, B=0, C=0 and the output becomes Fs=1 and Fc=1.

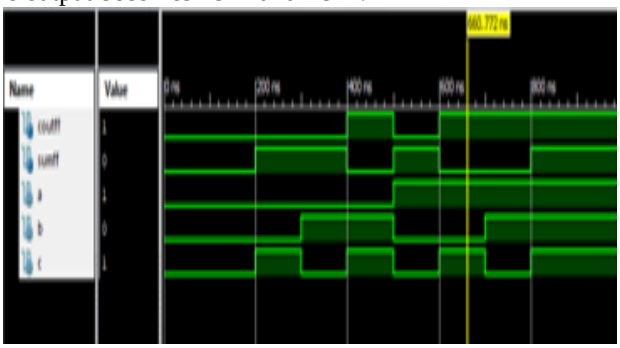

Fig 8. Simulation results of Self repairing

In the above fig. 8 the three inputs are A=1, C=1, B=0 and the output becomes sumff=0 and coutff=1.

Delay Analysis of Self Repairing:

Total Delay: 6.236ns (5.194ns logic, 1.042ns route)

The total delay is 6.236ns. The total delay is consists of 83.3% of logic delay and 16.7% of routing delay.

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V. IMPLEMENTATION RESULTS

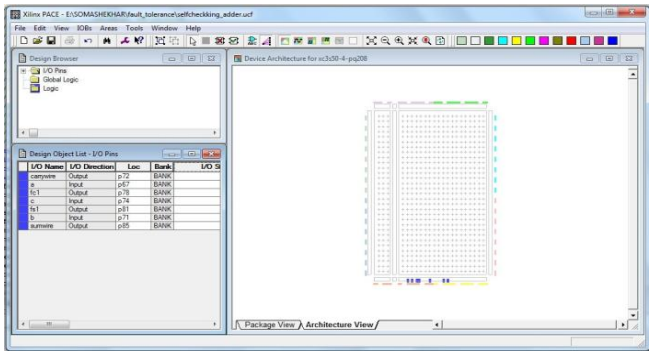

Fig 9. UCF file

In this fig.9 UCF is generated using 7 pins of XC3S50 device. 3 pins are used for inputs a, b and c and 4 pins are used for out pins Sumwire, carrywire, fc1 and fs1.

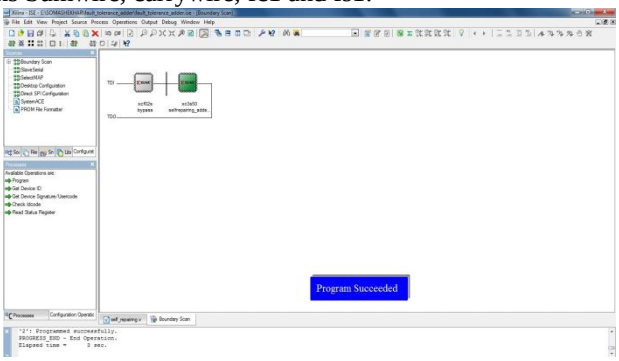

Fig 10. Boundary Scan checking

In this fig.10 boundary scan, the JTAG is used for boundary scan testing

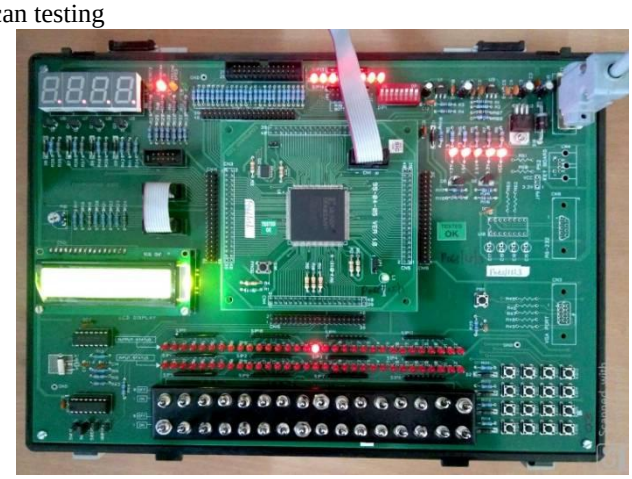

Fig 11. FPGA Implementation Results

Figure 11 shows the implementation of fault tolerant full adder on FPGA Spartan 3, XC3S50 device. It consists of 32 I/O pins.

VI. CONCLUSION

This fault tolerant adder has high speed (Delay is 6.236ns) & implemented on FPGA Spartan 3 using XC3S50 device. The source code is written in verilog. In this design faults are identified and repaired using self checking and self repairing full adder methodologies.

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