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VLSI Implementation of Digital Filter using Novel RTSD Adder and Booth Multiplier

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Abstract: ***Finite Impulse Response (FIR) filters are most important element in signal processing and communication. Area and speed optimization are the essential necessities of FIR filter design. This work looks at the design of Finite Impulse Response (FIR) filters from an arithmetic perspective. Since the fundamental arithmetic operations in the convolution equations are addition and multiplication, they are the objectives of the design analysis. For multiplication, Booth encoding is utilized in order to lessen the quantity of partial products. Consequently, considering carry-propagation free addition strategies should improve the addition operation of the filter. The redundant ternary signed-digit (RTSD) number framework is utilized to speedup addition in the filter. The redundant ternary representation utilizes more bits than required to denote the single binary digit because of which most numbers have several representations. This special behavior of RTSD allows the addition along with the absence of typical carry propagation. Xilinx ISE design suite 14.5 is used for the design and validation of proposed method. From the implementation result, the proposed design of FIR filter is compared with other conventional techniques to show the better performance by means of power, area and delay.***

Keywords: Finite Impulse Response (FIR) filters, Redundant Ternary Signed-Digit (RTSD) adder, Booth Multiplier, low power and delay.

I. INTRODUCTION

The digital filtering is considered as trustworthy and also the significant part of the DSP (Digital Signal Processing) which is created and linked to the domain of electrical engineering [1]. A filter is employed to drive out few portion of signal, so, on the contrary, the two terms are used more often [2]. The digital filter is basically a discrete time, discrete amplitude convolved [3]. The Essential Fourier transform hypothesis states that the linear convolution of two classes in the time field is as similar as the copying of two connecting ghost like progressions in the frequency field [4]. The digital filtering plans are used to enhance the signal in the selected frequency ranges, remove or restraint specific frequencies, stifle commotion, additional unusual actions and force bandwidth [5].

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For performing the digital filters, frequently, a method is applied in view of a subgroup of the impulse response of the filter [6]. The filter defined along these lines is called FIR filters [7]. The yield of a linear structure can be acquired by utilizing the arithmetical process as denoted by its stimulus reaction is the convolution [8].

Commonly, filtering is the growth of the signal range through the frequency area impulse response of the filter [9]. The digital filters are prepared into FIR(Finite Impulse Response) and Infinite Impulse Response (IIR) filters [10]. The finite impulse response digital filters contain the accurate linear stage response and the remarkable benchmark plan and undergo the harmful effects of the influences of the finite word length as compared and IIR digital filters [11]. The major portions of the FIR filter are latency, adder and multiplier [12]. Addition is considered as the basic mathematics doings for each arithmetical assignments such as division, multiplication, and square rooting. The carry propagation delay is a restraining changeable of the adder and the multiplier [13].

The emollient of the carry propagation link its adders is fundamental with a particular final objective to impact the FIR to filter performs addition quicker [14]. This can be attained by the two common methods such as the carry space addition and the marked digit addition [15]. The Marked digit number structure can do addition and subtraction with a restrained propagation of carry. This component prepares the adder's defer autonomous of the operand length which proposes less deferral [16]. The carry propagation can go parallel from one location to another part. The sign of the quantity is provably communicated in the digits and no distinctive depiction is needed for this cause [17].

The various quick circuits with the benchmark configures and the low power structure have been suggested with the recent progression in the novelty of the combined circuits [18]. For the arithmetic assignments, the circuits still suffers some concerns such as hardware complication, propagation time delay and the limited scope of the amount of bits. The adders and the multipliers are sketched out the propagation delay is reduced of the FIR filter considering additional number [19]. The RTSD (Redundant ternary sign digit) numbers is mainly enhancing much thought owing to the capability of carry free addition [20].

The rest of the paper is organized as follows, the below section 2 give the literature review and major contribution of proposed work. The next section 3 give the detail explanation of the planned work and the related results are deliberated subsequent part 4. Finally, the work is concluded in the last section of this paper.

II. RELATED WORK

Some of the recent work related to the redundant ternary sign digit arithmetic is listed here. For every arithmetic element, adders are necessary and also the significant element, especially quick parallel adder. The RTSD (Redundant ternary sign digit) adders are proposed to execute the quick arithmetic jobs. The RTSD (Redundant ternary sign digit) number structure brings free addition that diminishes the extra time of two binary numbers. The manual calculations are not supportive yet precious in planning quick arithmetic machines in the computational state. Smita Sharma et. al. [21] concentrated on the quantity structure to dispose of the obtained propagation chains that diminishes the computational time and improves the quickness of the machine. The illustration of numerous adders such as Wallace Tree Addition, Carry Select Adder, Carry Spare Addition are specified in this manuscript and also the circuit of rapid Redundant ternary sign digit adder cell is matched and the Carry Look Forward Adder.

The experts are convinced by the RTSD (Redundant ternary sign digit) number structure to plan the quick processing devices. Due to the surprise of the absence of carry evaluation and regulator precondition, the redundant ternary sign digit (RTSD) can execute the rapid totalling of two numbers. A new method to deal with the plan RTSD adder cell was introduced by Shukla, Vandana et al [22] by employing few necessary reversible logic gates, for instance, Peres gate, Feynman and BJN. This adder cell strategy is taken as the basic work for the low misfortune and, moreover, fast digital structures. Also, there is amount of additional streamlining of dissimilar implementation parameters to enhance the output of the planned adder circuit. This suggested plan is recreated by employing the Modelsim device and the combined for Xilinx Simple 3E with the Device XC3S500E with 200 MHz frequency.

On the whole, the limited products are diminished in the enhancement process in a high radix changed booth encrypting computation. A Redundant ternary (RT) depiction can be employed while planning the superior multipliers, owing to its great quantified value and carry-free addition, the current RB multiplier needs an extra RB Partial Product (RBPP) row, taking into account that an Error Correcting Word (ECW) is made by the radix-4 Modified Booth Encoding (MBE) and the RB encoding. For the Modified Booth Encoding multiplier, this carries an extra RB Partial Product collecting stage. An additional RB Modified Partial Product Generator (RBMPPG) was suggested by Ravichander, J and Gunde Mounika. A [23] to remove the extra Error Correcting Word and later, it spares one RBPP amassing stage. The suggested RB Modified Partial Product Generator (RBMPPG) makes fewer partial thing pushes than an average RB MBE multiplier in this method. The regeneration appears regarding to prove the suggested RBMPPG centred strategies pointedly to improve the area and power usage while the word length of all the operand in the multiplier is no less than 32 bits.

A. Major Contributions

A key contribution in this research is given as follows,

- VLSI implementation of a digital FIR filter for high speed application.
- Here, a carry propagation free addition (RTSD) technique is used for addition and a booth encoding technique is used for multiplication process.
- Simulate the proposed technique in Xilinx tool for low power and less delay.

III. PROPOSED METHODOLOGY

The proposed novel RTSD arithmetic has no separate sign bit as shown in figure 1. The number value is determined by the signed weighted value of the digit. Due to this the carry propagation will eliminate which is our important criteria for design of a digital filter. Area, delay and power are the three important design constraints for designing an embedded real-time digital signal processing systems. The area constraint is imposed primarily by considerations of cost. Area efficient implementation results in a smaller die size and hence becomes more cost effective. It also enables integrating more functionality on a single chip. The performance requirements of a system are driven by its data processing needs. For the requirement of high-speed and low-power applications, the development and implementation of high-speed FIR digital filters need both increased parallelism and reduced complexity in order to meet both sampling rate and power dissipation goals.

A. Proposed Novel RTSD Adder

The Redundant Ternary Representation (RTR) is a numeral system which utilizes more bits than needed to represent a single binary digit and hence each number have lot of representations. Negative values are available in RBR but there is no single sign bit to tell whether the particular number is positive or negative. The expression $\sum_{k=0}^{n-1} D_k 2^k$ is used to convert an integer from redundant ternary representation. In which, number of digits can be represented by n and the interpreted value of the k[th] digit can be denoted by D_k .Where, k start at 0 at the right most position [24]. The proposed redundant ternary sign digit (RTSD) adder perform the addition operation with the limited carry propagation to single digit position. This proposed RTSD also improve the speed of all arithmetic operations. In order to cope with the issue of carry propagation, an appropriate approach should be used for the elimination of carry propagation. If the addition of any representation does not require carry propagation, then it can be said as carry propagation free addition. Here, the addition process of all digits can be performed simultaneously.

$$A_i + B_i = 2x_i + y_i \quad (1)$$

The above equation is the basic formula for the RTSD arithmetic operation. Where, A_i & B_i are the two operands at which the transfer digit (x_i) and interior sum digit (y_i) can be calculated using the table 1.

$$S_i = x_i + y_i \quad (2)$$

The final sum digit (S_i) can be obtained through the addition of transfer digit and interior sum digit. There is no possibility for the generation of new transfer digit.

The sum of the operand is realized into three steps as:

- In first step the transfer digit is $|x_i| = 1$ only if $|A_i + B_i| \geq 1$

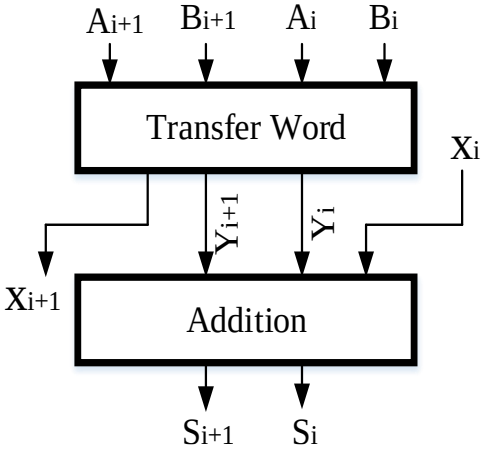


Fig. 1. Architecture of RTSD Representation

- In second step the transfer digit $|x_i| = 1$ only if $|x_i + y_i| = 2$ under these conditions both x_i & y_i cannot be 1.
- In third step the sum digits is obtained by carry free addition of x_i & y_i

The general block diagram of proposed RTSD adder is shown in figure 1. The inputs are A_i & B_i which are given to the transfer word block. Transfer digit (x_i) and interior sum digit (y_i) are the results of transfer word block. In the above diagram, the transfer digit X_{i+1} is transferred to the next addition block in order to stop the carry propagation process.

B. Algorithm and representation

The proposed algorithm for RTSD addition performed is given below:

$$2W_{2i+1} + W_{2i} = \left[2\left(X_{2i+1} + Y_{2i+1}\right) + \left(X_{2i} + Y_{2i}\right)\right] - 4t_{2i+2}$$
$$and \;\; S_i = \left(W_{2i+1} + W_{2i}\right) + t_{2i+2}$$

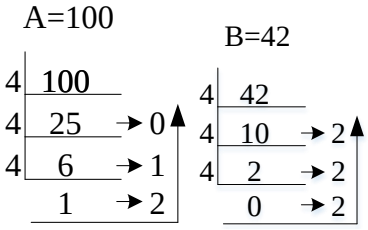
Where,

$$Z = 2W_{2i+1} + W_{2i}$$
$$and \; T = \left[2\left(X_{2i+1} + Y_{2i+1}\right) + \left(X_{2i} + Y_{2i}\right)\right]$$

Table- I: Calculation of Transfer Digit

Z	T	t_{2i+2}
1	-3	-1
0	-4	-1
-1	-5	-1
-2	-6	-1
-1	3	1
0	4	1
1	5	1
2	6	1

Example: [with reference to Table-I] Carry free RTSD addition of two numbers (100) & (-42) is given below.
Assume A= (100) and B= (- 42)
Step 1: Find the Ternary Signed Digit (TSD) representation of A & B.



$$A \Rightarrow 100 = (1210)$$
$$B \Rightarrow 42 \;\; = (0222)$$

The B value is negative so it's corresponding TSD representation will be $B \Rightarrow (-42) \; = (0 - 2 - 2 - 2)$
Step 2: Convert the TSD representation of A & B into binary numbers based on $(-2, +2, -1, +1)$ format.

	-2 +2 -1 +1	-2 +2 -1 +1	-2 +2 -1 +1	-2 +2 -1 +1
(1 2 1 0) →	0 0 0 1	0 1 0 0	0 0 0 1	0 0 0 0
(0-2-2-2) →	0 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0
	1	0	-1	-2

In the above addition of A & B, add the corresponding values from $(-2, +2, -1, +1)$ for the presence of 1 in the binary representation. If sum is above 2 or -2, then take carry, e.g. if sum is -3 then take -3=+1 - 4, so sum is +1 and carry to next MSB i.e. -1.
Step 3: Finally add the resultant values (1 0 -1 -2) as follows.

$$(1\;0\;-1\;-2) = (1\times 4^3) + (0\times 4^2) + (-1\times 4^1) + (-2\times 4^0)$$
$$= 64 + 0 - 4 - 2$$
$$= 58$$

After the completion of binary addition, the value will be converted into decimal value. Delay improvement, word length independency, carry free addition and high efficiency are some of the benefits of RTSD adder.

Table- II: Transfer Digit & Interior Sum for RTSD

	-2	2	-1	1	-2	2	-1	1	-2	2	-1	1	-4	4	
	X_4	X_3	X_2	X_1	Y_4	Y_3	Y_2	Y_1	Z_4	Z_3	Z_2	Z_1	C_2	C_1	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1
2	0	0	0	0	0	0	1	0	0	0	1	0	0	0	-1
3	0	0	0	0	0	0	1	1	-	-	-	-	-	-	-
4	0	0	0	0	0	1	0	0	0	1	0	0	0	0	2
5	0	0	0	0	0	1	0	1	0	0	1	0	0	1	3
6	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1
7	0	0	0	0	0	1	1	1	-	-	-	-	-	-	-
8	0	0	0	0	1	0	0	0	1	0	0	0	0	0	-2
9	0	0	0	0	1	0	0	1	0	0	0	0	0	0	-1
10	0	0	0	0	1	0	1	0	0	0	1	1	1	0	-3

C. Booth Multiplier

The parallel encoding scheme is adopted by the booth multipliers to produce the partial products for the implementation of large parallel multipliers. This type of encoding scheme reduces the number of additions and pipeline stages via the reduction of number of partial products. Here, three bits are recorded at a time which in turn speed up the multiplication process. In each cycle, large amount of bits can be reviewed and eliminated and hence the total number of cycle requirement get reduced. The number of bit inspection at the radix (r) can be denoted as,

$$Number of\ bits = 1 + \log_2 r \quad (3)$$

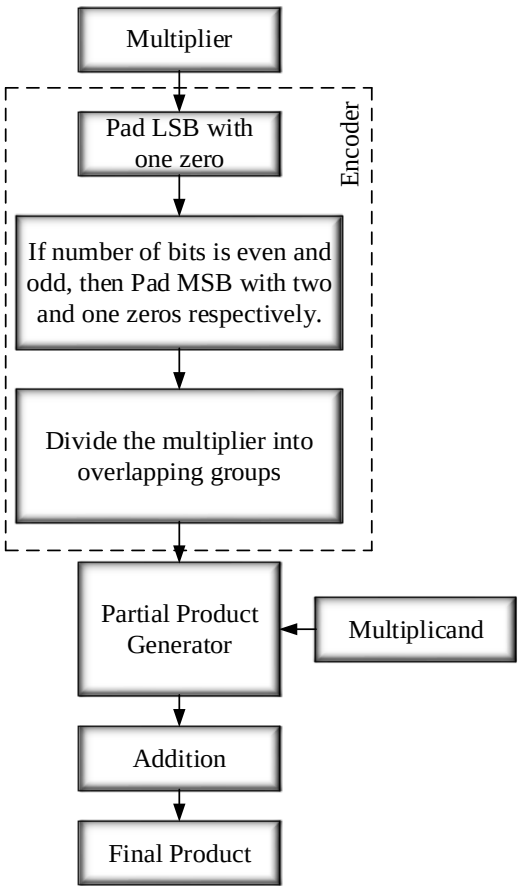


Fig. 2. Architecture of Booth Multiplier

The figure 2 shows the process flow of booth multiplication process with the main blocks. Normally, the basic blocs used in the booth multiplication process are encoder, adder and a partial product generator. The inputs like multiplier and multiplicand are given to the booth algorithm. The multiplier is directly given to the encoder block and get the encoded signal as the output. The partial products are obtained from the encoded signal and multiplicand at the partial product generator block side. The resultant partial products are added with the help of adder block in the final stage.

Consider the 8×8 bit multiplication, a normal multiplier produces eight partial product rows whereas the booth multiplier generates 3 rows only. Here, the number of bits are divided by 3 for the reduction of row. For example, consider two numbers for the multiplication like 25 as multiplier and 39 as multiplicand. Here, 011001 & 100111 are the corresponding binary representation of 25 & 39 respectively. Initially, four digits LSB of the multiplier with an appended zero is considered for the determination of first partial product. The resultant partial product is 1110 which means the multiplicand has to multiply by the value -1 by taking two's complement of the multiplicand. Therefore, 1100111 is resulted as the first partial product with seven-bit length. The next four bits of the multiplier is used for the finding of second partial product. In this case, multiplicand is multiplied by -3 by left shifting one bit of two's compliment of the multiplicand value with the resultant partial product value 10110101. The next four bits is utilized for the determination of third partial product i.e., multiply by 1. Here the partial product is 0011001 which is same as the multiplicand value. The addition of these, three partial products will be the final result i.e. 001111001111.

D. FIR Filter Design

Digital filtering plays a vital role in the field of electrical engineering due to the development and application of digital signal processing.

Digital filtering method is widely used for the noise suppression, signal enhancement in selected frequency range, specific frequency attenuation and other special operations [25].

Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) are the main two types of digital filter design.

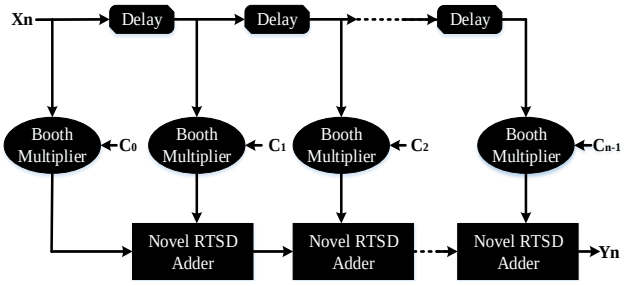


Fig. 3. Proposed FIR Filter

The proposed work focus on the design and implementation of FIR filter based on novel redundant ternary number systems. The structure of proposed FIR filter is shown in the figure 3. The main components of FIR filter are adder, multiplier and delay. The carry propagation delay is a limiting factor of the adder and multiplier. Based on redundant number, novel RTSD adder and booth multiplier are designed in such a way that the propagation delay is reduced of the FIR filter. In FIR filters, the subset of the filters impulse response can be considered for the implementation purpose.

$$Y[n] = \sum_{k=0}^{n} C[k]X[n-k] \qquad (4)$$

In expression, input and output of the FIR filter is denoted as x[n] & y[n] respectively. In figure 2, the delay denotes the inversion and shift in the input x[n].

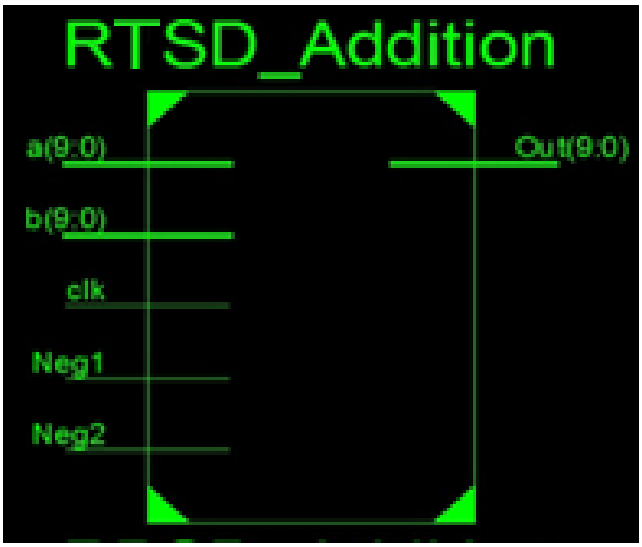
The constant coefficient value C is multiplied with the taps of delay block. The performance of the FIR filter is widely affected by the slow functioning of multiplier system. Hence, Booth multiplier is used in the proposed work which in turn reduces the area and speedup the performance. At each clock cycle, a new data sample and corresponding coefficients are given as inputs to the multiplier. This block performs the function of the Booth multiplier which is clearly explained in the section 3.2. The carry propagation should be stopped in order to speed up the FIR filter operation. After the completion of multiplier operation, the FIR filter needs to be assembled [26]. The proposed work uses the RTSD adder which adds the positive and negative parts of the signed digit number.

$$X = (X^+, X^-)_{n-1}(X^+, X^-)_{n-2}.....(X^+, X^-)_2(X^+, X^-)_1(X^+, X^-)_0 \qquad (5)$$

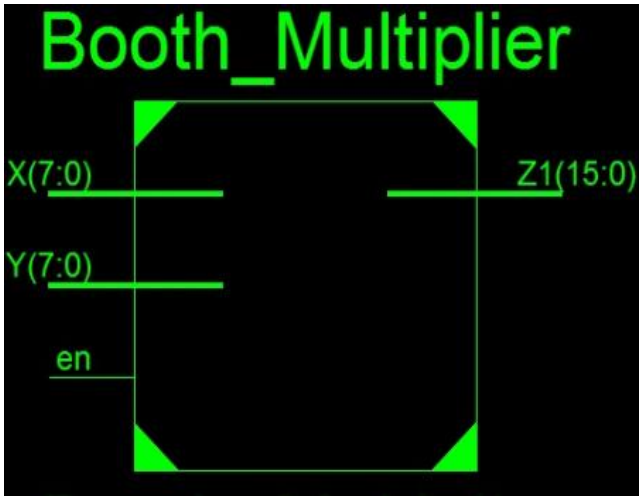
In expression 5, $X_P = X^+_{n-1}X^+_{n-2}.....X^+_2X^+_1X^+_0$ is the positive part and $X_N = X^-_{n-1}X^-_{n-2}.....X^-_2X^-_1X^-_0$ is the negative part. The corresponding 2's complement representation is $Y = X_P + X_N$. The RTSD adder perform the addition operation as explained in the section 3.1 as a final block. Therefore, final outcome of the FIR filter is delay free result with improved parallelism and less complexity.

IV. RESULTS & DISCUSSIONS

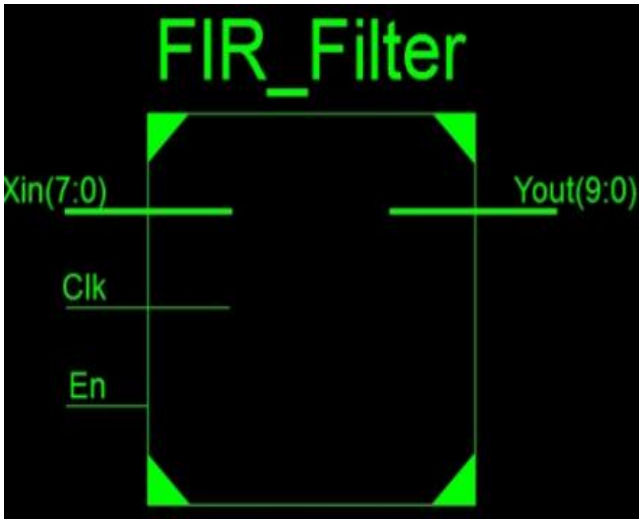
The implementation of proposed work is carried out in Verilog on structural Register Transfer Level (RTL) and its synthesis & simulation is performed with the help of Xilinx ISE design suite 14.5. The RTL view of the proposed work including novel RTSD adder, booth multiplier and proposed FIR filter is displayed in the figure 4 (a), (b) & (c) respectively. The positive and negative inputs are given to the RTSD adder. There is no carry generation at the output side due to the novel working procedure of RTSD adder. The simulation reports for the proposed adder, multiplier and filter design is represented in the figure 5.



(a) Novel RTSD Adder



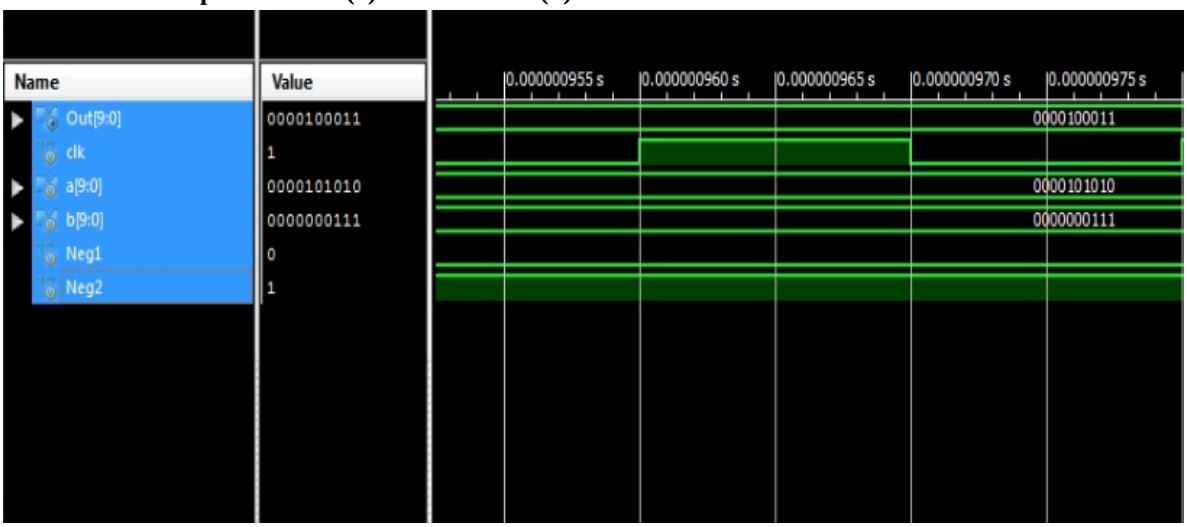
(b) Booth Multiplier



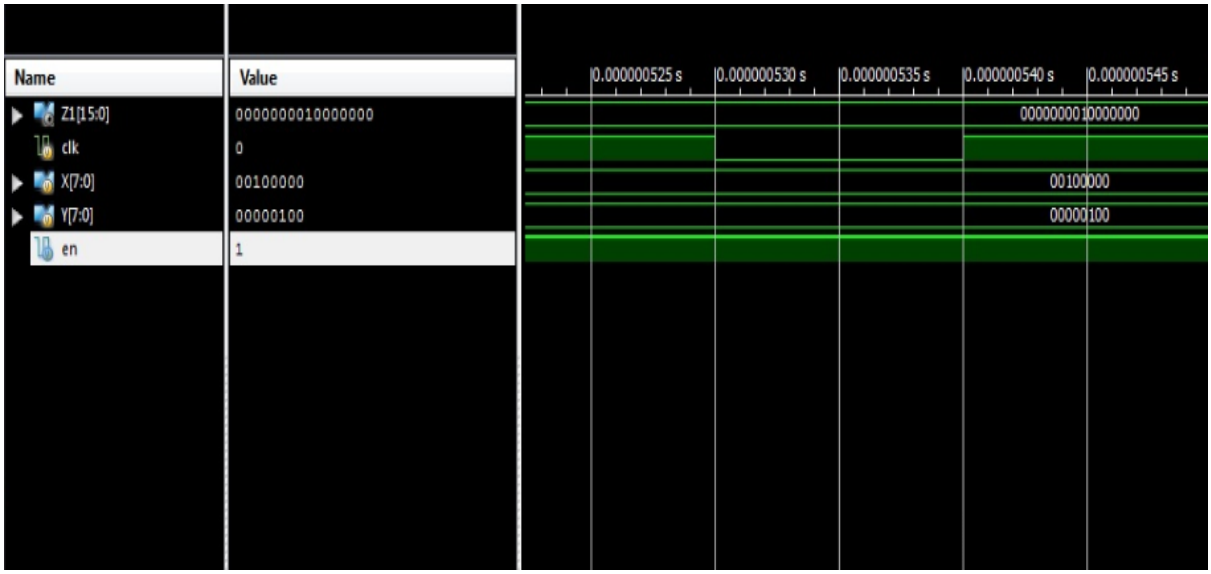
(c) Proposed FIR Filter

Fig. 4. RTL View of Proposed Work (a) RTSD Adder (b) Booth Multiplier (c) Proposed FIR Filter

The simulation results of the proposed work is given in the figure 5 for each blocks such as RTSD adder (5a), Booth multiplier (5b) and FIR filter (5c). Similarly, the design summary of the proposed work is taken through the Xilinx implementation of filter blocks. The two values like (42) & (-7) are taken for the implementation purpose of RTSD adder as an example. In figure (5a), the inputs are 0000101010 & 0000000111 and the corresponding carry free result will be 0000100011. Here, Neg 2 value is given as 1 to indicate the negative part of one of the inputs. In figure (5b), the values of 4 & 32 are taken for the implementation of booth multiplier. Likewise, the implementation of FIR filter is shown in the figure (5c).



(a) Novel RTSD Adder



(b) Booth Multiplier

(c) Proposed Filter

Fig. 5. Simulation Result of Proposed Work (a) Novel RTSD Adder (b) Booth Multiplier (c) Proposed Filter

Device Utilization Summary (estimated values)		
Logic Utilization	**Used**	**Available**
Number of Slice Registers	199	687360
Number of Slice LUTs	214	343680
Number of fully used LUT-FF pairs	162	251
Number of bonded IOBs	33	1200
Number of BUFG/BUFGCTRL/BUFHCEs	1	248

(a) Novel RTSD Adder

Device Utilization Summary (estimated values)		
Logic Utilization	**Used**	**Available**
Number of Slice LUTs	133	343680
Number of fully used LUT-FF pairs	0	133
Number of bonded IOBs	33	1200
Number of BUFG/BUFGCTRL/BUFHCEs	1	248

(b) Booth Multiplier

Device Utilization Summary (estimated values)		
Logic Utilization	**Used**	**Available**
Number of Slice Registers	496	687360
Number of Slice LUTs	474	343680
Number of fully used LUT-FF pairs	343	627
Number of bonded IOBs	19	1200
Number of BUFG/BUFGCTRL/BUFHCEs	1	248

(c) Proposed Filter

Fig. 6. Design Summary of Proposed Work a) Novel RTSD Adder (b) Booth Multiplier (c) Proposed Filter

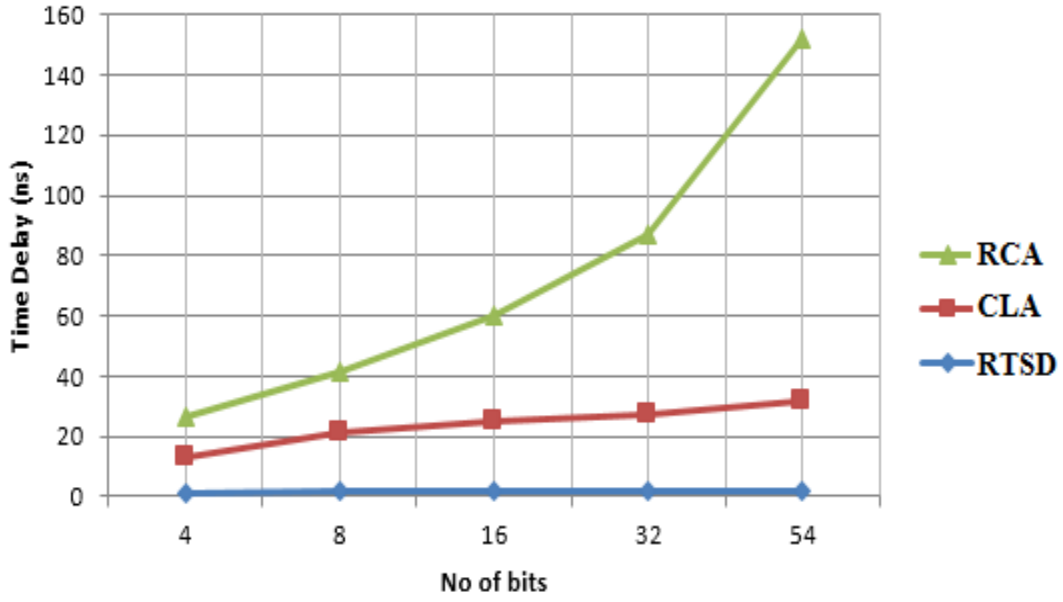


Fig. 7. Delay Comparison

Table III: Area & Power Comparison of Proposed Work with Existing Techniques

Parameters	FIR Filter with RCA	FIR Filter with CLA	FIR Filter with Proposed RTSD
Target Device	XC3s50-5pq208	XC3s50-5pq208	XC6VLX550T2
Number of LUTs	918	1065	474
Number of slices	510	582	496
Number of IOBs	86	86	19
Power (mW)	68.33	68.33	26.02

The figure 6 (a), (b) and (c) shows the design summery of RTSD, booth multiplier & FIR filter is given in the following representations. Logic device utilization of Xilinx implementation is considered as the design summary. The following tabular representation shows the comparison of components utilization from the available components. Number of registers, look up tables, flip-flops, slices and input/output components are present in the device utilization table.

The delay comparison is performed among FIR filter design with Ripple Carry Adder (RCA), Carry Look ahead Adder (CLA) & proposed adder. The delay comparison is diagrammatically represented in the figure 7. In the proposed work, the delay is 1.177ns (4 bit), 1.547ns (8 bit), 2.033ns (16 bit),2.033ns (32 bit) & 2.033ns (54 bit). The delay of the proposed work is lower than the existing works which are taken for the comparison.

The area and power comparison of proposed work is given in the below table 2. Actually, FIR filter design with RCA and CLA is considered as the existing works for the comparison purpose. The number of LUT is 918, 1065 & 475 for RCA, CLA &RTSD respectively. The number of IOBs are same for RCA & CLA which is 86 and the proposed work has 19 IOBs. The power consumption of the proposed work is 26.02 mW which is lower than the existing methods i.e, 68.33 mW for both RCA & CLA.

V. CONCLUSION

In this work, VLSL design and implementation of FIR filter have been approached from the arithmetic perspective. From the adder design using RTSD number system, there is no carry propagation after second stage of addition. So it will reduce the addition time by reducing the length of the maximum carry propagation chain. Since number of stages for completion of addition in this method is less than the previous one, hence power dissipation will be less. Along with the RTSD adder, booth multiplier is also used for the filter design to raise the speed of operation. The proposed digital filter design is simulated in Xilinx tool and compared the outcomes with existing works in terms of power (26.02mW), area and delay (2.033ns). Further, various types of digital filters can also be designed using the proposed adder in future.

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