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Heterogeneous Logic: a High Performance and Low Power Non-CMOS 4-1 Multiplexer

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Abstract*: A novel non-CMOS 4-1 multiplexer using heterogeneous logic style is presented in this brief. The heterogeneous logic design uses the combination of three basic logic styles such as Dual Value Logic (DVL), Transmission Gate Logic (TGL) and Simple Pass Transistor Logic (SPTL). The design uses only two stacking transistors in between the supply rails. Only 16 transistors are required for the actual logic function in the proposed state-of-the-art design. Number of transistors is reduced by distinctly choosing DVL and TGL in the first stage as per the input combination. Later stage of the multiplexer is constructed using SPTL. A required logic style is chosen at first and second stage in accordance with input bit combination to minimize the number of transistors, enhance the speed of logic transition and reduce the average power dissipation. The design and simulation analysis of proposed circuit is carried out at 22nm technology using Pyxis Schematic and Pyxis Simulator. Comparison of wide-ranging simulated results of proposed design, CMOS tree multiplexer and CMOS NOR multiplexer at various supply voltages and frequencies on same technology node manifests that the performance of proposed heterogeneous multiplexer is better in terms of speed and power dissipation. At minimum possible supply voltage of 0.8V and at moderate frequency of 1GHz, the proposed multiplexer achieves, reduced power dissipation of 17.3% and reduced in delay of 9.14%. The count of transistors including inverters is also less compared to CMOS tree type and CMOS NOR type multiplexers. However, robustness of mixed logic style designs is to be improved compared to CMOS designs.

Keywords: Logic Styles, VLSI, Multiplexers, CMOS, Heterogeneous Logic.

I. INTRODUCTION

Performance of digital components would consistently relies on logic styles that are being used at the gate level. Multiplexer is one of the most widely used circuit and has mushrooming applications. Few of the applications are Data Acquisition (DAQ) instruments, telephone network, computer memory and communication systems etc., in which only one signal is to select among many signals. CMOS logic styles are being used widely in the digital circuits. During last few decades, CMOS logic style is applied pointedly for designing and implementing multiplexers as it exhibits low static power dissipation, robustness to supply voltage variations and high degree of compactness in layout. There is time to time improvement in the performance of CMOS multiplexers which are designed by researchers as described in [9], [10] and [11]. But few of the conventional and non-CMOS logic styles such as Pass transistor Dual Value Logic [3], Transmission Gate Logic [4] and Simple Pass Transistor Logic may also be used to satisfy the specifications of certain applications. Therefore, conglomerating few logic styles for a single IC, the performance of some digital circuits could be improved. The source of motivation for the mixed logic design of the proposed multiplexer model is the significant work in [2]. To target the reduction in power dissipation, propagation delay and area Heterogeneous Logic (HL) may be used. Non-CMOS circuits can also compete with CMOS for some of the digital circuits as per previous non-CMOS associated works such as [2], [3] and [8]. However, CMOS circuits are more robust compared to mixed logic style designs but an attempt can be made to attain such requirement. As per the number of transistors, Non-CMOS circuits are better [13].

The proposed design, static CMOS multiplexer, DVL design of only the required expression, TGL design and circuit architecture of proposed multiplexer are detailed in Section II. The implementation of designs and discussion on the obtained results are included in Section III. Section IV comprises concluding points, future scope and extension of the brief.

II. PROPOSED DESIGN

With minimum possible number of MOSFETs, a 4-1 Heterogeneous Logic Multiplexer (HLM) is designed . The design of 4-1 HLM is categorized in to two stages. First stage comprises the active high output decoder using Heterogeneous Logic (HL) and the second stage consists four input OR logic which is cascaded to the outputs of the decoder. The work of [2] is extended by adding SPTL OR gate to design novel HLM. The new multiplexer is designed with low power and high performance decoder [2], using minimum number of transistors in the first stage followed by Simple Pass Transistor Logic (SPTL) AND gates in second stage. The decoder [2] is implemented with DVL and TGL for reducing the number of complemented variables and to restrict number of MOSFETs to 12 only. The second stage of 4-1 HLM is realized using SPTL. This OR logic in the second stage allows providing actual inputs of HLM directly to source or drain terminals of MOSFETs, instead of giving inputs to first stage [9-11].

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By distinctly choosing SPTL, inputs are directly fed to second stage for reducing the
signal propagation delay. Therefore, the root cause of choosing SPTL in spite of its disadvantages is to reduce input signal propagation delay.
Moreover the input signal is traversed through only single MOSFET; which results in signal degradation maximum of threshold voltage of the device. An utmost care is also taken for boosting the output voltage level to the maximum extent. The design and explanation for constructing the proposed circuit is as follows. The HLM requires only two stacking transistors between the supply rails even though size of the multiplexer is increased.

A. Complementary MOS

The most popular, with least static power dissipation and high compact layout logic style is CMOS[4]. This logic style is also more robust to supply voltage changes [5]. To compete with this logic a novel HLM circuit is designed and it is compared with CMOS circuit on same technology node. Therefore, a 4-1 CMOS Multiplexer is constructed using equal number of nMOSFETs and pMOSFETs. The pull-up network is designed using p-type devices connected in parallel and pull-down network with n-type devices connected in series [13]. The developed circuit of CMOS 4-1 tree type Multilexer (CT) is shown in Fig.1. But CT is not best suited for the comparison with proposed HLM. Therefore to bring out a fair comparison of CMOS logic and heterogeneous logic, a CMOS 4-1 Multiplexer using NOR gates (CN) is considered as shown in Fig.2.

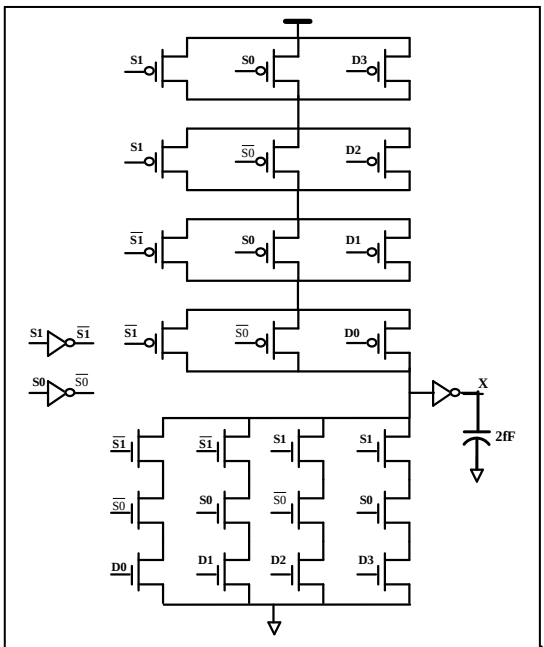

Fig.1 CMOS 4-1 Tree type Multiplexer (CMOSTM).

The selection inputs are S1 (MSB) and S0 (LSB) and the data inputs of CMOS Multiplexers are considered as D3, D2, D1 and D0. The logical expression of output X is stated below.

$$X = (S1.S0.D3) + (S1.\overline{S0}.D2) + (\overline{S1}.S0.D1) + (\overline{S1}.\overline{S0}.D0) \quad (1)$$

The logical expression of output X described by (1), is simple and straight forward but to mitigate the signal propagation delay, it is required to intensively look for number of complemented variables. Focusing on CN shown in Fig.\ref{fig:2}, selection inputs S1 and S0, both are to be complemented to get their inverted form.

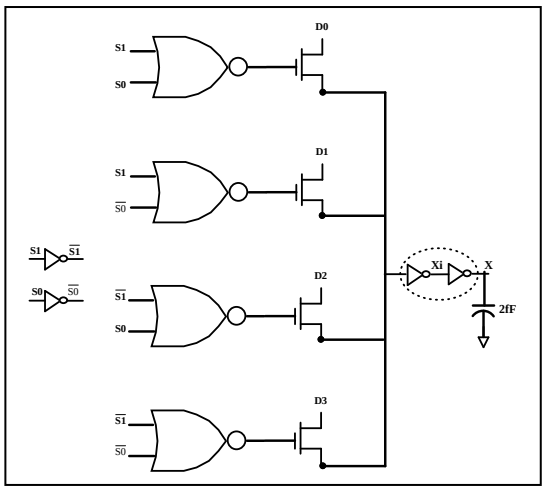

Fig.2 CMOS 4-1 NOR based Multiplexer (CMOSNM).

Moreover, every NOT gate has to drive two pMOSFETs and two nMOSFETS, in total of four devices for a single 4-1 CMOSM. But as the resolution of CT and CN increases to 16-1, 32-1 and so on, such load on NOT gate may be a hazardous in case of propagation delay. Even though the CMOS is ratio-less logic, the aspect ratio of pMOSFET in NOT gate should be high to produce high output current, through which NOT gate can drive overall gate capacitances of four MOSFETs.

At the same time CMOS logic always produces complemented output, an additional NOT gate is mandatory specifically in case of multiplexer, as it should produce one of inputs among D3, D2, D1 and D0 in their original form but not in complemented form. As per the literature survey, based on the circuit analysis of CMOSM the following conclusions were drawn,

- Total number of MOSFETs required for 4-1 CMOSM are 30 (including NOT gates) and can be minimized to improve the performance.
- Number of complemented variables can be reduced to eliminate redundant NOT gates.
- Loading effect on NOT gate can be decreased to enhance the speed of circuit.

B. Dual Value Logic (DVL)

The main objective of introducing DVL is for reducing the number of devices by eliminating the redundant devices [14]. It produces full voltage swing at output with lower transistor count [15]. DVL has some merits like by merely arranging the input signals to reduce the complimented variables for some digital circuits; redundant branches could be eliminated to minimize layout area. Also duality and complementary form of output function can be easily designed. Considering these advantages, DVL is used in the first stage of proposed design. This logic is utilized to generate two product/minterms, as denoted by following equations.

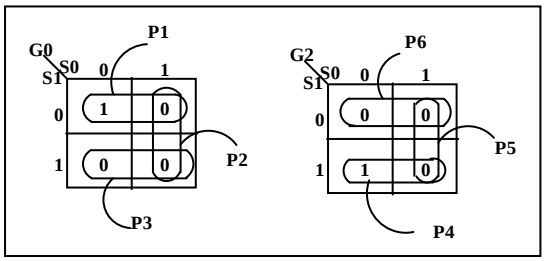

Fig.3 Karnaugh map notation for G0 and G2.

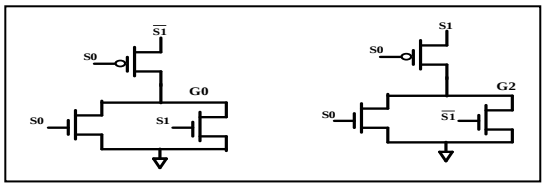

Fig.4 Circuit realization for G0 and G2 using DVL.

To realize the G0 expression, P1 combination in Fig.3 is implemented using single pMOS device, P2 and P3 combinations are realized using two nMOS devices whose source terminals are connected to ground. Previous work [2], to realize (2), used CMOS logic which requires 3 transistors. Now the same DVL circuit is used, limiting the number of transistors to 3 by maintaining the good logic swing at output node. The DVL circuit shown in Fig.4 is embedded in the proposed design. In similar fashion, to realize the expression of G2, P4 combination is implemented by a single pMOS transistor and two nMOS transistors are connected in parallel to realize P5 and P6 combinations. Since DVL is ratioed logic, more emphasis has to be put on aspect ratios of single pull up transistor and two pull down transistors for acquiring full logic swing, equal charging and discharging times. As the complexity of design is extended, the count of transistors would be limited. Therefore, it also targets the layout area to attain compactness of system.

C. Transmission Gate Logic (TGL)

A dual version of TGL is introduced [12]. TGL is a basic and simple logic style to overcome the drawbacks of simple pass transistor logic SPTL[13]. As the number of series stacking transistors increases in SPTL the output voltage is degraded, which results in poor switching of the transistors. This disadvantage is eliminated in TGL by connecting nMOS and pMOS transistors in parallel. TGL has an ability to produce full logic swing. Transition times from 0 ->1 and 1 -> 0 should be very less and has to be taken care of. Additional transistor is used for faster discharging from logic 1 to 0, to increase the switching speed of TGL. Either pMOS or nMOS transistor can be used as additional transistor. Transmission Gate is a combination of nMOS and pMOS transistors connected in parallel. Complimented signals are given to gate terminals of nMOS and pMOS transistors.In the proposed design, TGL is used to realize two output expressions of decoder. The equations are as shown below. The corresponding circuit realizations based on (4) and (5) are designed in TGL \cite{bal} and shown in Fig.5.

$$G1=S1'.S0 \quad (4)$$

$$G3= S1.S0 \quad (5)$$

Both circuits are incorporated with additional nMOS device to pull down the output voltage from logic ‘1’ to logic ‘0’ at faster rate. Actual logic is obtained by using single transmission gate in both Fig.5 but additional transistor is only to fasten the discharging process. The function tables of the corresponding to TGL circuits shown in Fig.5 are shown in Table I and Table II respectively.

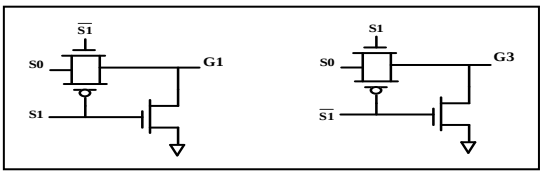

Fig.5 Circuit realization for G1 and G3 using TGL.

Table I. Function table of Fig.5 (a)

S1	S0	TG	nMOS	G1
0	0	ON	OFF	0
0	1	ON	OFF	1
1	0	OFF	ON	0
1	1	OFF	ON	0

Table II. Function table of Fig.5 (b)

S1	S0	TG	nMOS	G1
0	0	OFF	ON	0
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	OFF	1

D. Proposed novel Heterogeneous Logic Multiplexer (HLM)

Conglomeration of three different logic styles such as DVL, TGL and Simple PTL, resulted in the novel design of HLM. From previous research findings, the advantages of these logic styles are considered to design the state-of-the-art HLM. The three different logic styles are chosen appropriately according to input combination to enhance the speed of logical transition, to target the area and for reducing the power dissipation. The proposed design shown in Fig. 6 uses less number of transistors compared to previous designs without much degradation in performance. The source of motivation for the proposed design is from work done in [2]. This is modified and extended to get HLM. The first stage is fed up with selection lines of HLM and is designed using DVL and TGL using reduced transistor count. Only one of the outputs would be logic ‘1’ at an instant and remaining all outputs would be logic ‘0’. The choosing of logic style and the way of giving selection inputs is done distinctly to target the complemented variables reduction.

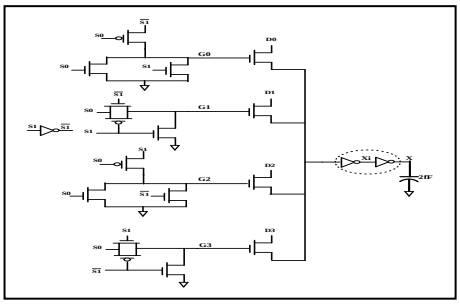

Fig.6 Proposed circuit of 4-1 HLM with minimum transistor count.

Among the two selection lines S1 and S0, only complement of S1 is needed. Previous designs used two complemented variables for same size of multiplexer. Therefore, the designer gets flexibility to select S1 as most significant signal (since it has to traverse through NOT gate) which has less number of transitions compared to S0. The design of first stage and generation of G0, G1, G2 and G3 outputs using DVL and TGL is already elaborated in previous sections. The second stage is constructed with SPTL, as it uses few transistors. One reason for choosing such obsolete logic style in spite of its shortcomings is actual inputs of HLM could be directly fed to second stage by skipping signal traversing through first stage. This would be one of the key factors for reducing the signal delay. However, there would be threshold drop of only single MOSFET and output voltage would diminished by Vth i.e. threshold voltage of nMOSFET. Another reason for selecting SPTL at second stage is actual inputs D0, D1, D2 and D3 are transmitted through single pass transistor with maximum drop of threshold voltage. Therefore, the actual input is transmitted through a single transistor. At the output side, signal boosting is done using two inverters. The inverted output Xi can also obtained if an application demands. This output would be complimented form of actual input signals. The function table of the novel HLM is shown in Table III. The outputs D0b, D1b, D2b and D3b shown in table are complemented signals.

Table III. Function table of novel 4-1 HLM.

Selection inputs		Outputs of first stage				Outputs	
S1	**S0**	**G0**	**G1**	**G2**	**G3**	**Xi**	**X**
0	0	1	0	0	0	D0b	D0
0	1	0	1	0	0	D1b	D1
1	0	0	0	1	0	D2b	D2
1	1	0	0	0	1	D3b	D3

III. EXPERIMENTATION AND RESULTS

The circuits and sub-blocks such as Inverter (INV), buffer (BUF), CMOS NOR decoder (CD), Heterogeneous Logic Decoder (HLD), CMOS tree type multiplexer (CT), CMOS NOR multiplexer (CN) and proposed HLM are designed and extensively simulated using mentor graphics SPICE tools at 22nm technology. For the best comparative analysis NOR based 4-1 Multiplexer is considered instead of CMOSTM which has more number of stacking transistors in between supply and ground. However the comparative analysis is done from first stage i.e. 2-4 CMOS Decoder using NOR gates (CD) and Heterogeneous Logic Decoder (HLD). The SPICE based simulation tool is used for analysis and comparison of designs. The Predictive Technology Model (PTM) 22nm Metal Gate/ High-K/ Strained-Si model files of nMOS and pMOS are used for simulation [7]. All the simulations are carried out on software like Pyxis schematic and Analog and Mixed signal simulator of Mentor Graphics HEP1: IC Nano Meter design by following steps [6]. All the simulations are carried out with temperature range (in degree centigrade) of -50 to +50 and no violations are detected.

Both designs are functionally verified and compared for same input pattern combinations with varied supply voltages and at various input frequencies with a 2fF of load capacitance. The dynamic power dissipation is proportional to square of the supply voltage and to know the performance of the circuits, both circuits are analyzed at four different voltages i.e. 0.8V, 1V and 1.2V. To analyze the speed metric all the circuits are simulated at 1 GHz frequency such for each value of supply voltage. Exhaustive simulations are done for the qualitative comparison of their performances and few worst case simulations are selectively chosen i.e. 63 simulations for power dissipation analysis as shown in Table V, power delay products of designs are shown in Table VI and 21 simulations for propagation delay analysis as shown in Table IV. To analyze the prorogation delay the circuits are stimulated with input pattern in such a way that output follows the most significant selection input of multiplexers. This technique is to compare input and output in terms of jitter delay. The implemented circuit of CT, CN and proposed HLM is shown in Fig.7, Fig.8 and Fig.9 respectively. A sample power dissipation comparison waveform is shown in shown in Fig.10. Based on the result analysis the novel and proposed HLM exhibits less power dissipation and propagation delay in comparison with static CMOS multiplexer. At every specified supply voltage and frequency HLM shows improvement in performance metrics. It is observed that percentage of power dissipation reduced at different voltages; 0.8V- 14.8%, 1V- 14.7% and 1.2V-14.6%.

For worst case assumption, minimum percentage reduction at respective voltage is considered for estimation of power dissipation and propagation delay. CT exhibited less propagation delay than CN. Therefore the propagation delay analysis the results of CT and HLM are compared. Propagation delay result analysis reveals that, it has been reduced at different voltages as; 0.8V- 9.14%, 1V- 17.8% and 1.2V-32.3%. By considering the results of power dissipation and propagation delay at lowest possible supply (0.8V) and highest frequency (4 GHz); 19.7% of power dissipation is reduced; propagation delay is diminished by 9.14. The comparison of power dissipation, propagation delays and power delay product of HLM, CN and CT are shown in Fig.11, Fig.12 and Fig.13 respectively. More over CN design is 28T circuit including 6 transistors for inverters but HLM design requires only 22 transistors. Therefore the count of transistors is lowered by 8.

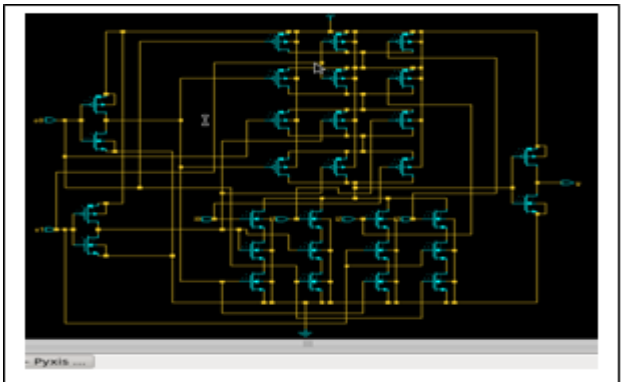

Fig. 7. Implemented circuit of 4-1 CMOSTM.

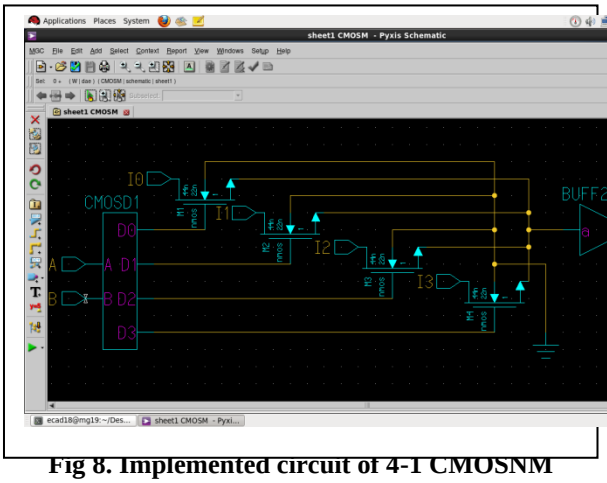

Fig 8. Implemented circuit of 4-1 CMOSNM

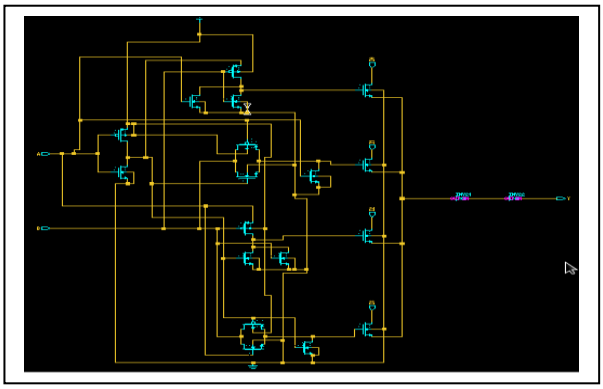

Fig. 9. Implemented circuit of 4-1 HLM.

Table 4. Propagation Delay (in Picoseconds) Results and Comparison.

Propagation Delay	0.8V	1.0V	1.2V
INV	0.514	0.405	0.336
BUF	1.944	1.724	1.627
CD	0.655	0.568	0.482
HLD	0.653	0.566	0.482
CT	7.512	6.709	6.485
CN	14.668	10.186	8.460
HLM	6.825	5.513	4.386

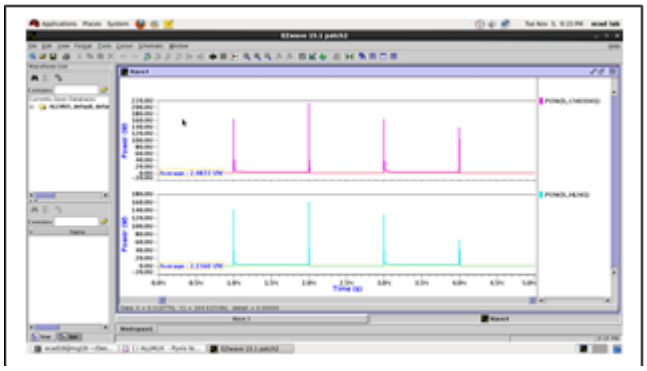

Fig. 10. Sample wave: Power dissipation comparison of CMOSNM and HLM for 1.0V at 1GHz

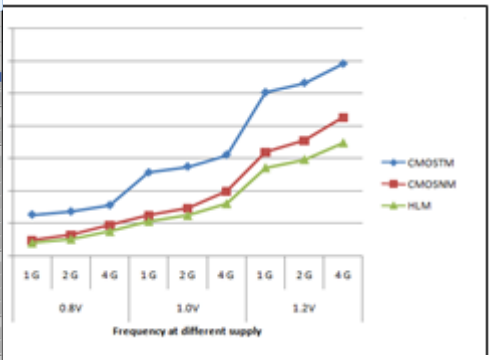

Fig. 11. Power dissipation comparison

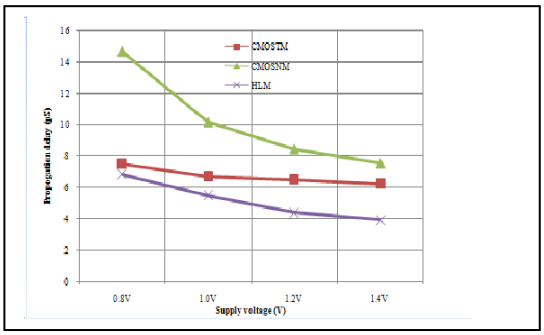

Fig.12. Propagation delay comparison

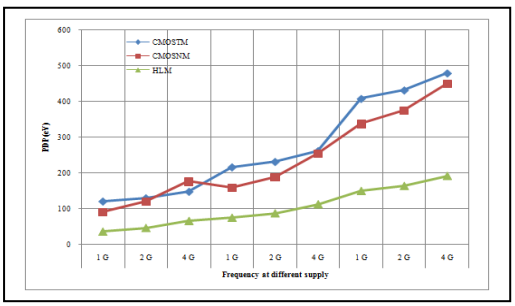

Fig. 13. PDP results comparison

Table-IV. Power dissipation (in Nanowatts) Results and Comparison.

Power Dissipation	0.8V			1.0V			1.2V		
	1G	2 G	4 G	1 G	2 G	4 G	1 G	2 G	4 G
INV	40	60	105	90	123	195	293	339	443
BUF	97	149	252	216	302	485	633	769	1052
CD	311	460	758	699	948	1656	2080	2452	3209
HLD	171	242	388	398	507	817	1262	1431	1786
CT	2546	2741	3131	5145	5507	6234	10071	10656	11837
CN	978	1299	1912	2483	2958	3988	6390	7094	8521
HLM	833	1074	1535	2156	2521	3250	5454	5958	6978

Table-V. Power delay Product (in Electronvolts) Results and Comparison.

Power Dissipation	0.8V			1.0V			1.2V		
	1 G	2 G	4 G	1 G	2 G	4 G	1 G	2 G	4 G
INV	0.128	0.193	0.337	0.228	0.311	0.493	0.615	0.711	0.929
BUF	1.177	1.808	3.058	2.324	3.250	5.219	6.429	7.810	10.684
CD	1.272	1.881	3.099	2.478	3.361	5.871	6.258	7.377	9.655
HLD	0.697	0.986	1.582	1.406	1.791	2.887	3.797	4.306	5.374
CT	119.3	128.5	146.8	215.4	230.6	261.0	407.6	431.3	479.1
CN	89.56	118.9	175.1	157.8	188.0	253.5	337.4	374.6	449.9
HLM	35.48	45.75	65.39	74.19	86.75	111.8	149.3	163.1	191.0

VI. CONCLUSION

This paper has introduced a novel, low power and high performance HLM by conglomerating DVL, TGL and SPTL. Considering the advantages and simplicity of the logic styles, they are chosen according to input combination. The design is best suited for low supply voltages and high frequencies compared to CN. As the lowest possible supply is the criteria, the proposed HLM achieves higher speed with an average reduction of 19.7% in delay; average reduction of 17.2% in power dissipation at minimum possible supply voltage and high frequency. The design achieves a greater reduction in delay compared to its reduction in power dissipation. The novel HLM is compact; requires fewer transistors than CN design. Therefore in all principle aspects of VLSI such as speed and power dissipation the proposed HLM design is better compared to static CMOS Multiplexer. At first stage the number of stacking transistors in HLM is only two between the supply rails. The design can be extended and used to develop key combinational circuits in arithmetic logic units. To make the design as library cell and full custom, it could be further extended to layout design.

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