

Low Power FPGA Implementation of Multi-View Video Coding with Hybrid Compression and Decompression Algorithm



Shaik Rahimunnisha, Ghanta Sudhavani

Abstract: The video is one of the most useful and most appealing medium to represent some information. More usage of digital multi-media via communications media, wireless communications, intranet, internet and cellular mobile leads to the uncontrollable growth of data in media. The video compression technique is used in this research work to improve the processing speed of the entire system. In this work, Low Cost - Multi Video Coding - Hybrid Compression and Decompression (LC-MVC-HCD) method is used to reduce computation complexity. The combinational of Discrete Wavelet Transform (DWT) and Discrete Cosine Transform (DCT) algorithms are denoted as hybrid algorithm. Based on this hybrid algorithm, the compression process is performing which improves the video coding efficiency of MVC. The LC-MVC-HCD method was implemented in the Matlab, Xilinx and Cadence tool. In Application Specific Integrated Circuit (ASIC) implementation, the area, power, and delay minimized by using the cadence encounter tool with 180nm and 45nm technology. In Field Programmable Gate Array (FPGA) implementation, the number of Lookup Tables (LUTs), slice, and flip-flop are minimized based on two different kinds of Virtex devices such as Virtex -6 and Virtex-7. In Matlab, Peak Signal to Noise Ratio (PSNR), computational time and bit error rate were analyzed for the LC-MVC-HCD method. The experimental outcome showed that the proposed methodology has improved performance ASIC and FPGA up to 2-3% compared to existing methods like Direct mode decision MVC and LC-MVC-DWT.

Keywords: Hybrid Compression and Decompression, Multi Video Coding, Two Dimensional Discrete Wavelet Transform, Discrete Cosine Transform.

I. INTRODUCTION

Multi-view Video (MVV) offers a sense of complete scene perception by sending different views to the receivers simultaneously. A 3D video transmission system adopts

Multi-view representation with efficient design, which enable by MV Coding (MVC). An efficient Statistical Direct Mode Early Termination (SDMET) has been introduced in MVC to speed up the computational complexity and the rate-distortion also adjusted by the cost threshold [1]. The integer motion algorithm introduced by motion estimator and it used for effective video compression in video coding [2]. The H.264/Advanced Video Coding (AVC) standard targeted by multiple reference frame motion estimation. In this system the data reuse method used for reducing the memory access. The process of MVC operation has reduced by temporal and inter-view predictions and also achieved better compression by the Rate Distortion Optimization (RDO) [3]. The coding of MV plus depth formats used for stereoscopic and auto stereoscopic MV displays. This is an extension of High-Efficiency Video Coding (HEVC) [4]. Less computational difficulties have been provided in the HEVC using 8-point DCT approximation, because it requires only 14 additions without multiplications. For an effective compression, a low complexity orthogonal 8-point Discrete Tchebichef Transform (DTT) has been introduced while processing the video, and this DTT used in both forward and near inverse transformations [5].

A Distributed MVC (DMVC) method introduced for encoding the MV video. The wavelet domain DMVC framework introduced for reducing the complexity of DMVC, which has large gap among the DMVC to the traditional MVC. In MV plus depth (MVD) based 3D video encoding, a rate control technique has been introduced for utilizing the image stitching technique at first, then the joint rate control has been developed for improving the video coding [6]. The motion and disparity estimation (ME & DE) architecture involved in the MVC and the data reuse techniques used for reducing the off-chip memory. The real-time processing requires 274 and 385 MHz for 6 views in a worst scenario. In MVC encoding, a multilevel pipelined parallel architecture developed for ME and DE and also four levels of parallelism exploited by pipeline scheduling. The full potential of the 3D neighborhood correlation of temporal, spatial and disparity domains were not exploited by the fast ME/ DE algorithms [7]. So, in this paper, the quality of the video is improved by using 2-Dimensional DWT and DCT. The quality of the video compression technique mainly depends on compression standard and motion estimation. The visual quality can be increased by using DCT technique that improve PSNR, Bit rate and computation time.

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This paper is composed as follows, section 2 explained the survey papers based on video compression. In the section-3, clearly described the LC-MVC-HCD method by employing 2-DWT and DCT combination. The section 4 explains the results and discussion of proposed LC-MVC-HCD and conventional methods: Direct Mode Decision-MVC, LC-MVC-DWT. The conclusion of this work is detailed in the section-5.

II. RELATED WORK

Jianjun Lei et al. [8] presented the bit allocation strategy for MVC, and bit allocation strategy depended on the multilevel Region of Interest (ROI). From the depth information of a video sequence, the Macro Block (MB) saliency was derived. This MB saliency was used for multilevel ROI segmentation. Coding efficiency for multilevel ROI and also the visual quality of video sequence was improved. The effective gain was achieved only when the bit rate was more than 2000 kbps.

Xin-Xian Huang et al. [9] solved the computational difficulties of MVC by introducing the fast mode decision algorithm that creates an early detection mode partition in MVC. In the current view, the complexity of MB was determined by utilizing the best modes of reference views. The computation time for the TZ search was reduced and the system was more efficient when the temporal and disparity estimation are considered in the fast decision algorithm.

HodaRoodaki et al [10] introduced the view level Rate-Distortion (RD) model and it considers the MV/ 3D video characteristics. The RD model parameters are discovered by using a statistical dependency within the MV frames. Because, this statistical dependency has disparity between views and motion for temporally successive frames. The proposed method has achieved high precision and low estimation error of 12%. This view level RD model is adjusted easily for wide range of MV/3D video applications. Prediction process is affected by the disparity between the views and motion.

Amara Berkhouf et al. [11] presented faster view random access to different views by using an inter-view prediction structure. For non-anchor B-pictures, the Prediction Structure without Inter-View Prediction method was introduced, which was named as PS-WOPB. The better trade-off among the view random access and bit rate were carried by PS-WOPB. Due to this, random access was developed up to 33.5%. It attains less PSNR ratio of 38 dB.

Yusuf Aksehir et al. [12] introduced a full search ME method to minimizing the number of computations performed by temporal and inter-view predictions in H.264 MVC. The temporal and inter-view predictions were introduced by low energy adaptive H.264 MVC ME. H.264 MVC ME consumed less energy. In TZ search, the PSNR loss and decrement of bit rate were obtained.

To overcome above mentioned problems, the LC-MVC-HCD method is implemented and their performances are analyzed in the Xilinx and Cadence tool, which achieves better FPGA and ASIC performances compared to existing methods.

III. LOW COST- MULTI VIDEO CODING HYBRID COMPRESSION AND DECOMPRESSION METHODOLOGY

The LC-MVC-HCD method compresses the video with a high rate of compression ratio. LC-MVC-HCD method comprises of Motion Estimation, Motion Compensation, and hybrid Compression systems that is combination of DCT and 2D-DWT, and the entropy coding. The process of MVC compression is explained in below steps:

- In the initial stage, one input image frame can be view at different viewpoints, it denotes $v_0, v_1, v_2, \dots, v_n$, which is present in the figure.1.Perspectives multiplexer figures every single distinctive view and multiplexer is proceeded as a few contributions with one output switch. The following info outline is given to the movement estimation process just as subtract activity process.
- The motion estimation is a significant process in video compression technique that reduces the temporal redundancy from video data. The hybrid compression system improves the data compression of video.
- The Fig. 1 shows the block diagram of the proposed LC-MVC-HCD method. To improve the picture grouping, it is required to assess the movement of the picture succession. The motion compensation takes the picture from the movement estimation of the picture compression process. Next, an info esteems and movement remuneration esteems are subtracted, later single casing is moved to the 2D-DWT.
- In this exploration work, the real picture size is 256x256, which is separated into 16x16. Here, each 16x16 frames are again disintegrated with the assistance of 2D-DWT.
- The LL, and HH frequency components are perform the DCT compression which output is connected to the Genetic algorithm.
- The main low-frequency co-efficient is moved to the following stage utilizing precise low frequency part, where the high frequency co-productive can be disposed.
- A low-frequency coefficient is moved to the IDWT and IDCT, which is utilized to reproduce the frequency modules.
- So, once the entire compression process is done, finally the LC-MVC-HCD method gets the compressed output. A brief description about the LC-MVC-HCD method is presented in the following section.

3.1. MOTION ESTIMATION AND MOTION COMPENSATION

The ME and Motion compensation are the fundamental procedure in the video compression plot, which creates better PSNR esteem and lessen framework multifaceted nature. The significant point of the movement estimation is to extricate the coordinating items from the picture outline. After the ME process the articles are forward to the Motion compensation. This procedure processes the quick edge to perceive the square when movement vectors are put away in the squares. The combination of video compression process with ME is known as inter frame coding.As, the PSNR value improves and the multifaceted nature of picture become less. The motion compensation process use as a prescient procedure.

In the event that a picture arrangement shows the moving items, at that point their movement inside the scene can be registered and data is used to frames the substance of edges later in the succession.

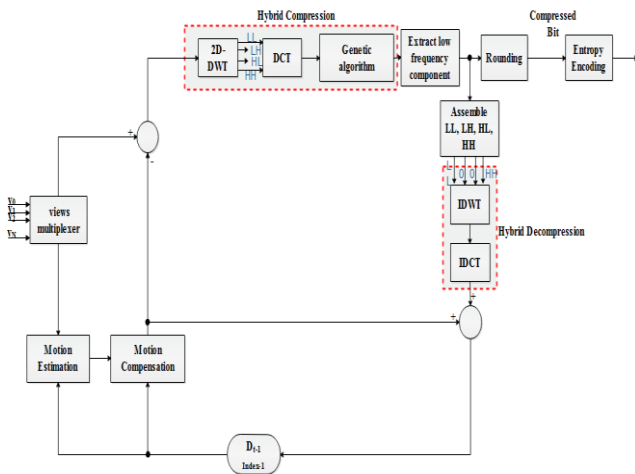


Figure.1. Block diagram for an LC-MVC-HCD methodology

The motion compensation technique communicates the change of a reference frame to the present frame. A reference edge might be taken later. At the point when the present frames can be synthesized from past transmitted edges, the compression effectiveness can be improved by utilizing the movement pay method.

3.2. . TWO-DIMENSIONAL DISCRETE WAVELET TRANSFORM

The DWT is a decimated wavelet transform, where the size of the image reduces by half at each scale. The significant advantage of the wavelet transform is to convert the spatial domain inputs into the frequency domain. High pass and low pass coefficient series are obtained from the input series y_0, y_1, \dots, y_n . The high pass and low pass coefficients are represented by using the following two equations (1) and (2).

$$H_i = \sum_{n=0}^{l-1} Y(2j - n) \cdot s_n(z) \quad (1)$$

$$L_i = \sum_{n=0}^{l-1} Y(2j - n) \cdot t_n(z) \quad (2)$$

Where, the wavelet filters are represented as $s_n(z)$ and $t(z)$, length of the filter is denoted as l and $j = 0, \dots, [n/2] - 1$. The spatial domain DWT is applied in two directions. First, 1D-DWT is applied on the horizontal axis and that results are applied to the vertical axis of 1D-DWT. There are four parts named as LL, LH, HL and HH obtained from the 2D-DWT.

The two-dimensional DWT is applied to all rows and columns of an image.

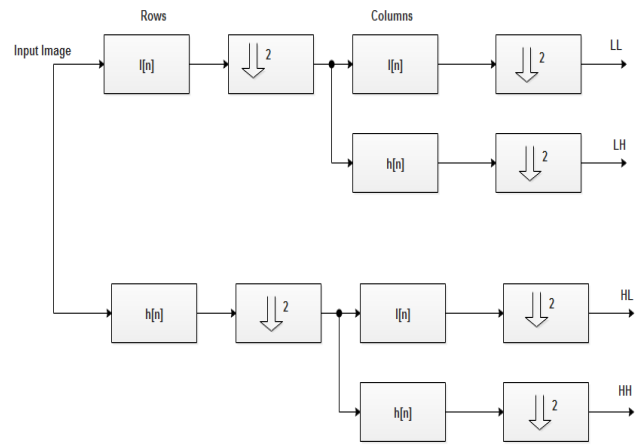


Figure.2. Discrete wavelet transform

If the input image is of size $2^k \times 2^k$ pixels at level L then after decomposition at level $L+1$ its size will be $2^{k/2} \times 2^{k/2}$ pixels. The different sorts of decomposition strategies use in wavelets over a picture. The DWT is applied to the info picture, which is separated into four sub picture. These sub pictures are named as sub groups. The LL sub band is the coarse level sub picture, HH, LH, and HL are the diagonal, vertical and horizontal segments of the picture separately. Finally, the input image is decomposed into four major components that is shown in Fig. 2. A high level 2D-DWT is developed by LL frequency and low pass components for multi resolution analysis.

3.3. DISCRETE COSINE TRANSFORM

After performing MC and ME, the information about the video is transmitted to the DCT. DCT is a video compression technique, and it transforms the data from time or spatial domain to the frequency domain. High compression rates of video processing achieve by the JPEG image compression standard. By using DCT, the information is converted into the frequency domain. The DCT output sets the higher amplitudes in the low spatial frequencies as a neighborhood pixel in an image which has a large likelihood of presenting minor differences in color. From those results, the high spatial frequencies are canceled, and it provides better compression rate and a small perceptible loss in the image quality. The following equation (3) defines the forward DCT.

$$Y = A \times X \quad (3)$$

$$F(u, v) = 1/4 C(u)C(v) \sum_{x=0}^7 \sum_{y=0}^7 f \quad (4)$$

$u, v, x, y = 0, 1, 2, \dots, 7$

$$c(j) = \frac{1}{\sqrt{2}}, j = 0$$

$$c(j) = 1, j = 1, 2, \dots, 7$$

$$F(x, y) = 1/4 \sum_{u=0}^7 \sum_{v=0}^7 C(u), C(v) F(u, v) \cos((2x + 1)u\pi/16) \cos((2y + 1)v\pi/16) \quad (5)$$

Where, the matrix of coefficients and sample are represented as A and X respectively, then the $N \times N$ transform matrix is denoted as A . Normally, the majority of the energy is focused on the upper left corner.



Subsequent to quantizing the changed grid, the majority of the information in this network are zero, at that point utilizing a zig-zag order to scan and run length coding, a higher compression proportion is accomplished. Reverse two-measurement 8x8 DCT change is appeared in condition (5).

3.1.1. QUANTIZATION AND ZIG-ZAG SCAN

The Quantization of the DCT coefficients is a key procedure, in light of the fact that the mix of quantization and run-length coding is zero which is the most positive state of the compression. The MPEG-1 uses a matrix called quantize (Q[i,j]). Every time when a pixel’s matrix (X[i,j]) has the same size Q[i,j], used to divide X[i,j] to get quantized value matrix X_q[i,j]. The example for quantization is shown in the Fig. 4.

$$\text{Quantization Eq}^n: X_q[i, j] = \text{Round} \quad (6)$$

$$\text{Inverse Quantization Eq}^n: X'[i, j] = X_q[i, j] * Q[i, j] \quad (7)$$

Inverse Quantization (DE-quantize) is utilized to reproduce the first value. Yet, quantization utilizes round capacity to get the closest number value, with the goal that the recreated value won't be equivalent to the first value. The distinction between genuine value and reproduced estimation of the quantized value is called as quantization error. In general, if Q[i,j] is carefully designed, visual quality will not be affected. After DCT and quantization process, all the AC values will be zero. By using a zigzag scan, a more consecutive zero will be obtained. The zigzag output is converted into the rational number, which is given to the input of the GA optimization process to select a low frequency portion.

3.4. GENETIC ALGORITHM

The GA calculation is an inquiry methodology dependent on the mechanics of common determination and genetic qualities of crossover, mutation and reversal. The determination administrator is select chromosome in the population. Every single chromosome comprises of qualities (bit). The crossover trades subparts of the at least two chromosomes. The mutation randomly changes the genetic estimation of comparable locale in the chromosome, which is displayed in the figure. 3. In the GA procedure, each person in search area is coded as a chromosome, it contains the characters: zero and one. To begin with, select arbitrarily a lot of chromosome to establish the essential population. Next, each chromosome is figured dependent on fitness work, which characterize the optimality.

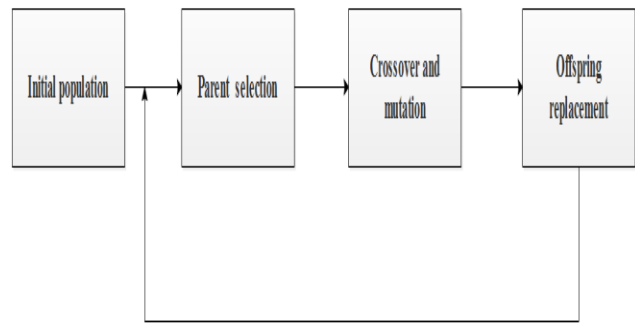


Figure.3. Phase of the Genetic Algorithm

Next, a lot of major activity is applied to the number of inhabitants in chromosomes. Determination is one of the significant activities in the GA procedure, which chooses the chromosomes as indicated by their fitness value. In this way, if a chromosome has a higher fitness value that will have a high opportunity to deliver off-springs into following generation. The chose parents are crossed to make another chromosome by trading qualities among parents in the crossover operation. The mutation is the last activity, which changes the quality of certain chromosomes. The GA stages are repeated until an optimal result is found. The GA output is given to the input of the Inverse DWT (IDWT) process. The reverse process of DWT is named as Inverse DWT (IDWT) that converts the frequency domain into the spatial domain. The output values of high pass and low pass filters are considered as approximate coefficients. That coefficients are less significant, so these values are neglected in a video reconstruction, and get the original video with less loss. The IDCT process is the reverse process of DCT, and this IDCT process reconstructs a sequence from its DCT coefficients. The IDCT function is the inverse of DCT function. $x = IDCT(y)$ that returns the inverse discrete cosine transform of y . The equation (8) describes the IDCT function.

$$X = A^T \times Y \quad (8)$$

Where, the transpose of the $N \times N$ matrix is denoted as A^T . An entropy encoding algorithm is applied to the IDCT output, which is described in the following section.

IV. RESULT AND DISCUSSION

The LC-MVC-HCD method was implemented in the three different types of tools such as Matlab, Xilinx and cadence tool. The performance of the FPGA has been analyzed for different Virtex devices analyzed with various families: Virtex-6-xc6vcx240t, Virtex-6- xc6vlx75t and Virtex-7-xc7vx330t in Xilinx ISE tool. The performance of the ASIC has analyzed based on 180nm and 45nm library technology.

Table.1. Experimental results comparison of FPGA Performance for existing and LC-MVC-HCD method.

Target FPGA	Methodology	LUT	Flip-flop	Slice	Number of DSP	Frequency (MHz)
	Direct Mode Decision-MVC [13]	548/150720	81/674	212/301440	34/768	108.2

Virtex6 xc6vcx240t	LC-MVC-DWT [14]	543/150720	76/674	207/301440	30/768	110.81
	LC-MVC-HCD	521/150720	73/674	199/301440	30/768	110.81
Virtex6 xc6vlx75t	Direct Mode Decision-MVC [13]	545/46560	79/674	209/93120	32/768	75.32
	LC-MVC-DWT[14]	543/46560	76/674	207/93120	30/768	80.921
	LC-MVC-HCD	521/46560	73/674	199/93120	30/768	110.812
Virtex7 xc7vx330t	Direct Mode Decision-MVC [13]	549/204000	77/674	216/408000	36/1120	110.35
	LC-MVC-DWT[14]	542/204000	75/674	207/408000	30/1120	127.905
	LC-MVC-HCD	521/204000	70/674	199/408000	30/768	127.905

Table.2. Experimental results comparison of FPGA Performance for existing and LC-MVC-HCD method.

Technology	Method	Area (um2)	Power (nW)	Delay (ps)	APP (um2 * nW)	ADP (um2 * ps)
180nm	Direct Mode Decision-MVC [13]	1249575	138764512	98.2	173396665082400	122708265
	LC-MVC-DWT[14]	1046188	107733257	96.8	112709240674316	101270998
	LC-MVC-HCD	1034152	106801008	96.8	110448476025216	100105913
45nm	Direct Mode Decision-MVC [13]	145615	15254311	275.3	2221256496265	40087809
	LC-MVC-DWT[14]	127180	13507326	273.8	1717861720680	34821884
	LC-MVC-HCD	126186	13420013	272.8	1693417760418	34423540

4.1. VERILOG PERFORMANCE ANALYSIS

Several numbers of devices are available in the FPGA platform, but this research work has selected only higher devices: Virtex-6 and Virtex-7, which achieves better performance compared to lower kind of Virtex devices: Virtex-4, Virtex-5 and so on. As well as in ASIC platform several library technologies are available, although this research work selected 180nm and 45nm technology, which improve the results compared to existing methods; Direct Mode Decision-MVC and LC-MVC-HCD. Comparison results between existing and LC-MVC-HCD method of the performance of FPGA are shown in table 1.

The proposed LC-MVC-HCD method has reduced the value of the FPGA performance parameters such as LUT, flip-flop, slice, DSP and increases the frequency compared to the existing methods. Both existing and LC-MVC-HCD methods were implemented in the Xilinx tool using the Verilog code and the outputs are tabulated in table 1. The proposed LC-MVC-HCD method has achieved less area by minimizing the hardware utilization. The figure. 4, 5 and 6 show a comparison graph of virtex-6 and virtex-7 for Direct Mode Decision-MVC[13], LC-MVC-DWT[14] and LC-MVC-HCD methods. In this research work, hybrid

compression and decompression technique used in the MVC for video compression that has achieved better FPGA results

compared to the Direct Mode Decision-MVC[13], LC-MVC-DWT[14] methods.

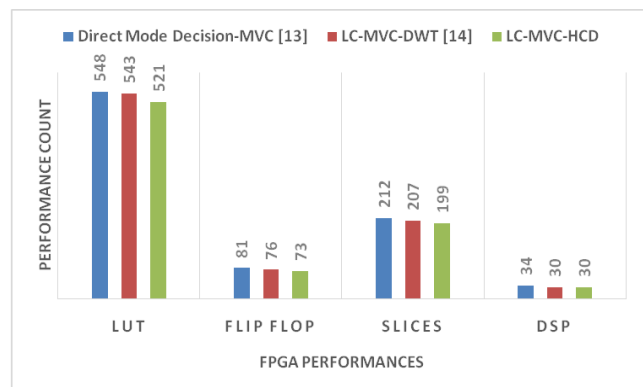


Figure.4. Virtex-6- xc6vcx240t performance of the exiting and LC-MVC-HCD methods.



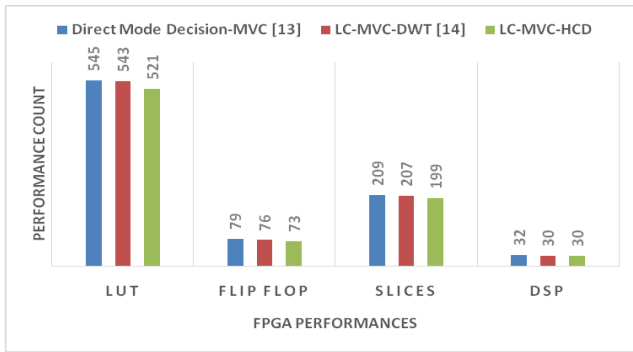


Figure.5. Virtex-6- xc6vlx75t performance of the existing and LC-MVC-HCD methods

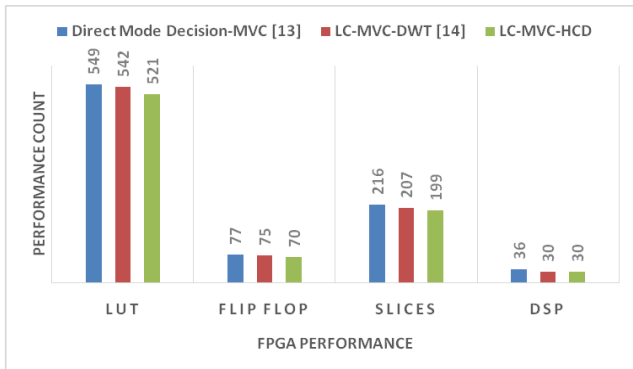


Figure.6. Virtex-7- xc7vx330t performance of the existing and LC-MVC-HCD methods

In this paper, the LC-MVC-HCD method was implemented in the Cadence tool of 180nm and 45nm technologies and that results are tabulated in table 1. In the existing methods, the direct decision mode and DWT techniques are used in the MVC to achieve the time reduction by skipping follow up time-consuming Motion Estimation technique, but this method required more area. Area, power, delay, APP and ADP are reduced in the LC-MVC-HCD compared to Direct Mode Decision-MVC and LC-MVC-DWT method. Fig. 6, 7, and 8 shows the comparison of the area, power, delay, APP and ADP.

Table 2 presents the reduced percentage of area, power and delay in the LC-MVC-HCD method. In 180nm technology, 1.15% of the area, 0.86% of power, 2.06 % of delay has been reduced by using LC-MVC-HCD method. In 45nm technology, 0.78% of area, 0.64% of power, 0.36 % of delay are reduced by using LC-MVC-HCD method than the conventional methods. The figure. 7, 8, and 9 shows the comparison graph of the performance parameter of the ASIC.

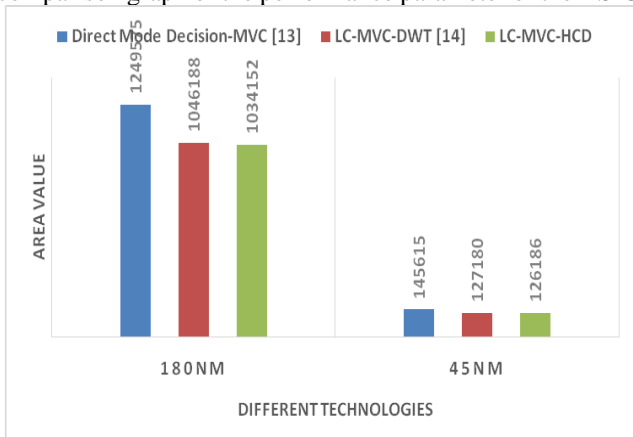


Figure.7. Area performance of the existing and LC-MVC-HCD methods for different technologies

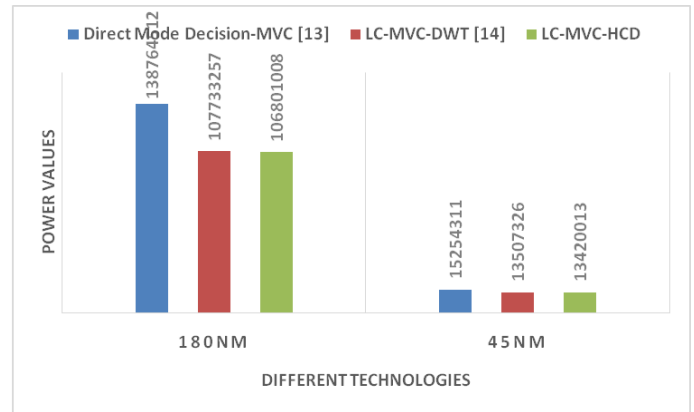


Figure.8. Power performance of the existing and LC-MVC-HCD methods for different technologies

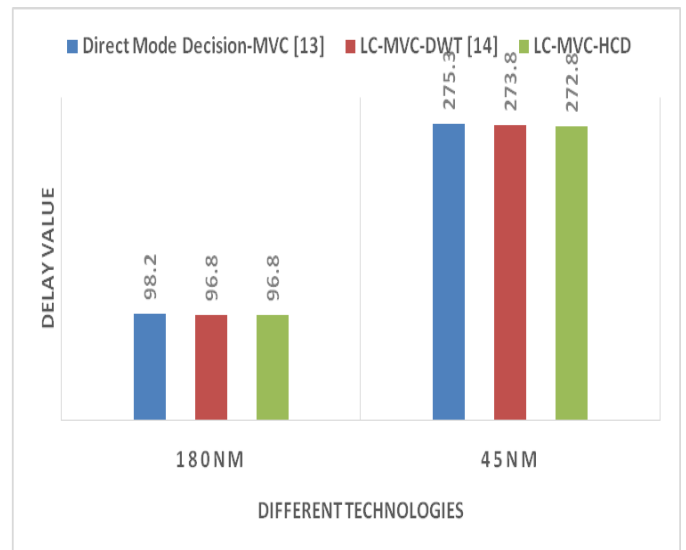


Figure.9. Delay performance of the existing and LC-MVC-HCD methods for different technologies

Figure.10 shows the Register Transfer Level (RTL) schematic top module of LC-MVC-HCD method includes encoder and decoder module, which is taken from the Cadence tool. The number of the output bits depends on the number of input bits. The LC-MVC-HCD is designed based of 8bit input and 8 bitoutput. The RTL schematic of encoder design is shown in fig.11 and RTL schematic of decoder design is shown in fig.12.The synthesis is a process by an abstract form of designed circuit RTL has been converted into a design implementation. The synthesis of Verilog code has carried out by cadence tool. The top-level RTL schematic for the background subtraction algorithm designed and implemented on ASIC platform. This is a schematic representation of the pre-optimized design shown at RTL.

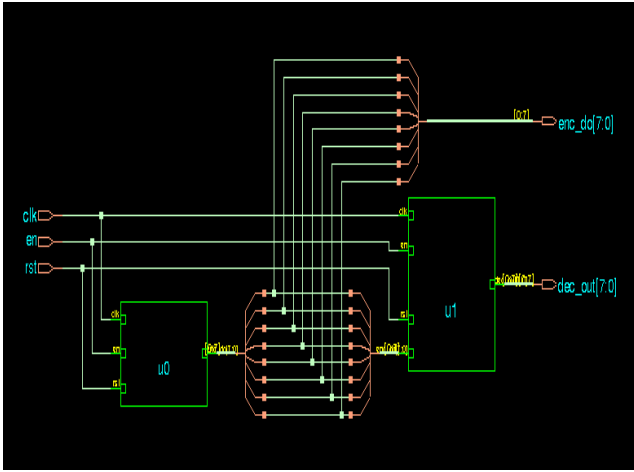


Figure.10. RTL view top module of the LC-MVC-HCD method

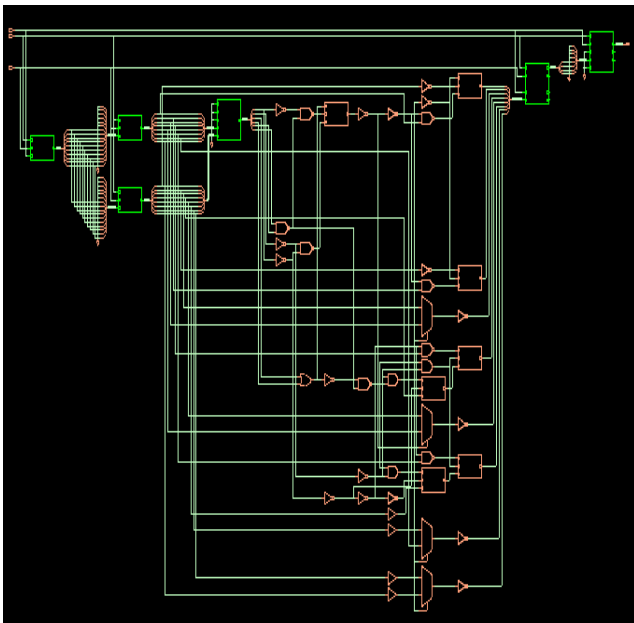


Figure.11. RTL schematic of encoder design

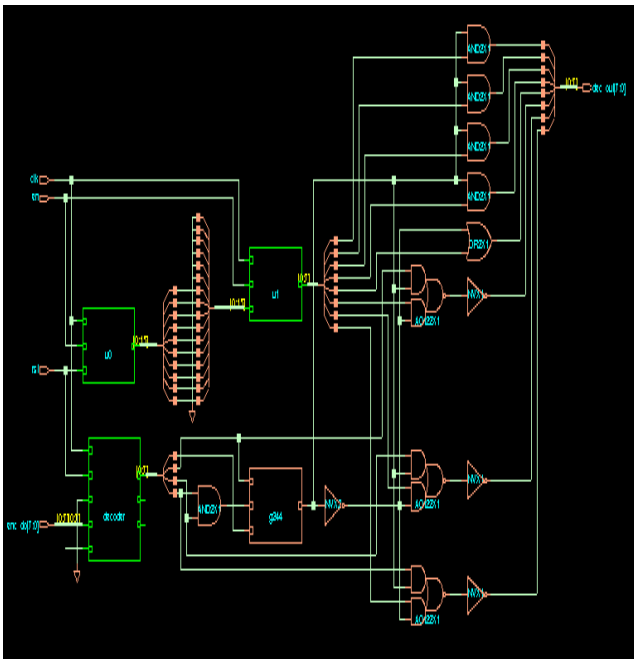


Figure.12. RTL schematic of decoder design

4.2. MATLAB PERFORMANCE ANALYSIS

The performance LC-MVC-HCD method was evaluated in MATLAB (Version 2018a) on Personal Computer (PC) with the 64-bit operating system. PSNR and computational times has been analysed of LC-MVC-HCD method.

4.2.1. PEAK SIGNAL TO NOISE RATIO

The pixel difference between 2-images are represent as PNSR. The PSNR is defined in Eq. (9)

$$PSNR = 10 \log \frac{S^2}{MSE} \quad (9)$$

Here, $S = 255$ is used for an 8-bit image.

4.2.2. COMPUTATIONAL TIME

It is a time required to process the entire operation with effective manner. Generally, the computation time is directly proportional to the applications of number of rule. The PSNR (dB) and computation time (s) of the LC-MVC-DWT and LC-MVC-HCD method computed in the MATLAB tool. In this paper three different types of the camera frames are taken for PSNR and computational time analyzed such as camera 1, camera 2 and camera 3. From the table 3, it is clear that the PSNR and computational time have been improved in the LC-MVC-HCD due to the proposed method using HCD techniques. Figure.13 shows comparison graph of the RD cost performance for existing and with GA and without GA of LC-MVC-HDC method. In this experiment, the PSNR and bit rate are computed for the original and output frame. Here, the RD cost is computed based on the PSNR (dB) and bit rate (kpbs). Performance of the RD and encoding time are improved in the H.264/AVC by using the best supporting mode. Figure.13 shows that proposed method obtains an excellent coding performance in terms of the RD performance and encoding time saving. In experimental, the RD cost is computed for three different types of the video coding technique such as LC-MVC-DWT[14], LC-MVC-HCD method based on with and without genetic algorithm.

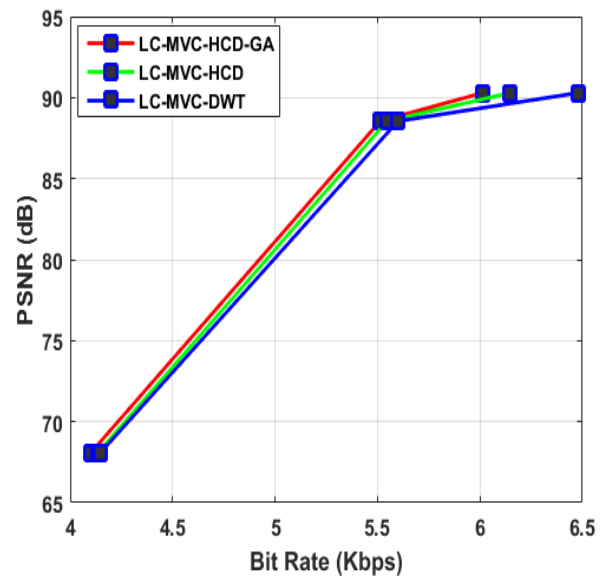


Figure.13. Comparison graph of the RD cost performance for existing and with GA and without GA of LC-MVC-HDC method

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Compared to RD cost performance of three methods, the LC-MVC-HCD- with GA method was achieved better RD cost compared to the other two methods such as LC-MVC-DWT, LC-MVC-HCD without GA. A RD model used for inter predictions, which models as the rate as linear combination of the non-zero quantized transform coefficients and sum of absolute values of the all non-zero coefficients separated by quantization step size. With a better RD estimation, the original residual encoding process: inverse and forward transform, entropy encoding, quantization and an image reconstruction is not required in the mode decision after inter or intra computation in the H.264/AVC encoding operation

V.CONCLUSION

In this paper, HCD based LC-MVC video compression technique have implemented and results obtained for different videos. This research work has achieved low computational time, improved bit rate and PSNR value due to

the usage of DCT and DWT hybrid compression algorithm. After decompression algorithm, RD cost has been evaluated to verify the compression quality of the algorithm. The same compression algorithm has been implemented in FPGA platform to evaluate the hardware utilization. The performance of the FPGA and ASIC have been improved in research work by using LC-MVC-HCD method. Additionally, this method was achieved less computational time and increases bit rate, these performance metrics were computed in Matlab for different frames. In 180nm technology, 1.15% of area, 0.86% of power, 2.06 % of delay reduced using LC-MVC-DWT[14]. In 45nm technology, 0.78% of area, 0.64% of power, 0.36 % of delay were reduced using LC-MVC-DWT[14] method than the conventional methods. In future work, efficient wavelet transform technique can be used to further improve the video quality.

Table.3. Performance of PSNR and Computation time for the LC-MVC-DWT[14] and LC-MVC-HCD method.

Methodology	Cam No	Background image	Current frame	PSNR,(dB)	Computational time (seconds)
LC-MVC-DWT[14]	Cam1			74.2194	4.7628
	Cam2			75.5677	1.1988
	Cam3			74.1342	1.1945
LC-MVC-HCD	Cam1			68.0561	2.7769
	Cam2			88.5449	0.7802
	Cam3			90.2895	0.8498

REFERENCES

1. Zhang, Y., Kwong, S., Jiang, G., Wang, X. and Yu, M., 2012. Statistical early termination model for fast mode decision and reference frame selection in multiview video coding. *IEEE Transactions on Broadcasting*, 58(1), pp.10-23.
2. Elhamzi, W., Dubois, J., Miteran, J. and Atri, M., 2014. An efficient low-cost FPGA implementation of a configurable motion estimation for H. 264 video coding. *Journal of real-time image processing*, 9(1), pp.19-30.
3. Grellert, M., Sampaio, F., Hecktheuer, B., de Mattos, J.C. and Agostini, L., 2010, December. Memory-aware multiple reference frame motion estimation for the H. 264/AVC standard. In *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on* (pp. 575-578). IEEE.
4. Müller, K., Schwarz, H., Marpe, D., Bartnik, C., Bosse, S., Brust, H., Hinz, T., Lakshman, H., Merkle, P., Rhee, F.H. and Tech, G., 2013. 3D high-efficiency video coding for multi-view video and depth data. *IEEE Transactions on Image Processing*, 22(9), pp.3366-3378.
5. Oliveira, P.A., Cintra, R.J., Bayer, F.M., Kulasekera, S. and Madanayake, A., 2017. Low-complexity image and video coding based on an approximate discrete tchebichef transform. *IEEE Transactions on Circuits and Systems for Video Technology*, 27(5), pp.1066-1076.
6. Liu, Y., Huang, Q., Ma, S., Zhao, D., Gao, W., Ci, S. and Tang, H., 2011. A novel rate control technique for multiview video plus depth based 3D video coding. *IEEE Transactions on Broadcasting*, 57(2), pp.562-571.
7. Zatt, B., Shafique, M., Bampi, S. and Henkel, J., 2011, March. Multi-level pipelined parallel hardware architecture for high throughput motion and disparity estimation in multiview video coding. In *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011* (pp. 1-6). IEEE.
8. Lei, J., Wu, M., Feng, K., Hu, C. and Hou, C., 2014. Multilevel region of interest guided bit allocation for multiview video coding. *Optik-International Journal for Light and Electron Optics*, 125(1), pp.39-43.
9. Huang, X.X., Chen, M.J., Yeh, C.H., Chi, H.W. and Chen, C.Y., 2014. Efficient multi-view video coding using inter-view information. *Signal Processing: Image Communication*, 29(6), pp.667-677.
10. Roodaki, H., Irvani, Z., Hashemi, M.R. and Shirmohammadi, S., 2016. A View-Level Rate Distortion Model for Multi-View/3D Video. *IEEE Transactions on Multimedia*, 18(1), pp.14-24.
11. Bekhouch, A., Bouchrika, I. and Doghmane, N., 2016. Improving view random access via increasing hierarchical levels for multi-view video coding. *IEEE Transactions on Consumer Electronics*, 62(4), pp.437-445.
12. Aksehir, Y., Erdayandi, K., Ozcan, T.Z. and Hamzaoglu, I., 2012, October. A low energy adaptive motion estimation hardware for H. 264 multiview video coding. In *Design and Architectures for Signal and Image Processing (DASIP), 2012 Conference on* (pp. 1-6). IEEE.
13. Wang, Fengsui, Huanqiang Zeng, QinghongShen, and Sidan Du. "Efficient early direct mode decision for multi-view video coding." *Signal Processing: Image Communication* 28, no. 7 (2013): 736-744.
14. ShaikRahimunnisha, GhantaSudhavani, "Efficient Implementation of Multi-View Video Compression for High Performance Application", ShaikRahimunnisha, GhantaSudhavani, "Efficient Implementation of Multi-View Video Compression for High Performance Application", Received: June 1, 2017.