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Sense Amplifier Half Buffer Based Ripple Carry Adder for IEEE 754 Standards

Venkata Jeevitha Rongali, Sudhakar Jyothula

Abstract: ***Addition is a specifically used indispensable computation used for most of the applications including digital systems and control systems. Adder is a primitive constituent used in the construction of digital IC; also it is an essential part of signal processing applications like DSP. The speed of an adder circuit holds a considerable influence on the total performance of digital circuits. The prime objective of this research is to design ripple carry adder using different asynchronous logics like Multi-threshold null convention logic (MTNCL), Multi-threshold dual spacer dual rail delay insensitive logic (MTD^{3}L) and proposed Sense amplifier half buffer logic (SAHB). SAHB is an asynchronous Quasi-Delay -Insensitive (QDI) method used to achieve significant functional speed of the circuit. The standard library cells (2-input AND/NAND, 2-input OR/NOR, 2-input XOR/XNOR) are designed using proposed SAHB logic to design an 8- bit Ripple Carry Adder circuit. The proposed SAHB logic design provides the solution of minimum delay with improved speed compared to the existing logic design techniques. The asynchronous logics are designed using mentor graphics tool with 130nm technology. Various performances attributes like power dissipation, delay and energy are tabulated and compared with existing logics.***

Key words— ripple carry adder, QDI, DSP, MTNCL, MTD^{3}L and SAHB.

I. INTRODUCTION

Earlier days, the principle challenge of VLSI designer is to reduce the area of chip [1, 2]. Later years, the enormous advancement in technology allows the designer to aim for low power, portable and high speed digital circuits [3, 4, 9]. Consequently, in recent VLSI systems the energy consumption becomes the most crucial attribute of performance. Arithmetic unit is the fundamental block in digital systems. The performance of digital system depends upon speed and accuracy of an adder circuit. Arithmetic logic unit (ALU) requires an adder circuit for the purpose of addition and multiplication. Adders happen to be a vital hardware unit for the dynamic realization of ALU. They are widely used in various arithmetic and other kinds of applications especially in some parts of processor. Adder is a fundamental circuit used in digital arithmetic to perform addition of two N bit numbers.

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* Correspondence Author
Venkata Jeevitha Rongali, Electronics & Communication Engineering Department, Vignan's Institute of Engineering for Women college, JNTUK, Visakhapatnam, Andhra Pradesh, India.
rvjeevitha21@gmail.com, s
Sudhakar Jyothula, Electronics & Communication Engineering Department, Vignan's Institute of Engineering for Women college, JNTUK Visakhapatnam, Andhra Pradesh, India. udhakar.jyo@gmail.com

It is designed with the help of asynchronous (clock less) techniques due to its major advantages like less power consumption, lower interference due to Electro-Magnetic radiation (EMI) and high robustness correlated to the synchronous (clocked) design. This paper deals with three asynchronous logic design techniques which are, multi-threshold null convention logic (MTNCL), multi-threshold dual spacer dual rail delay insensitive logic (MTD^{3}L) and proposed sense amplifier half buffer logic (SAHB).

This presented paper is segmented into six sections. Section two describes two asynchronous logics MTNCL and MTD^{3}L with neat diagrams. Section three presents the proposed asynchronous logic known as "sense amplifier half-buffer", with neat diagrams. Section four delineates implementation of "8-bit Ripple carry adder" using SAHB logic. Section five presents the waveforms of SAHB logic and results are evaluated and tabulated. Ultimately, this paper is concluded in section six.

II. VARIOUS ASYNCHRONOUS LOGICS

A. Multi-Threshold NULL Convention Logic (MTNCL):

Multi-Threshold NULL Convention Logic (MTNCL) is a Sleep Convention Logic (SCL) designed with the combination of Multi-Threshold CMOS (MTCMOS) [5, 10] and NULL Convention Logic (NCL) circuits [11, 14]. MTCMOS circuit is an efficient leakage control technique in idle (standby) mode that utilizes both NMOS and PMOS transistors with two dissimilar threshold voltages [8, 10]. By means of high and low V_{th} transistors used in the design of MTCMOS circuit, it effectively eliminates the leakage problem and improves the performance of the circuit. The basic Null Convention Logic design enables robust, self timed asynchronous circuit comprising of SET, RESET, Hold0 and Hold1 blocks as shown in Fig.1 [7, 11, 12]. Employing multi-threshold to NCL [11, 13] technique results with the reduced transistor count in less circuit area and reduced power consumption. The MTNCL circuit design with a little high threshold voltage (V_{th}) transistor is presented in Fig. 2.

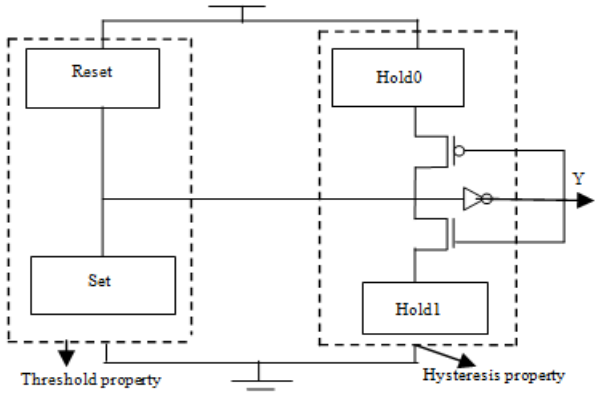

Fig. 1. Architecture of Static-CMOS NCL threshold gate

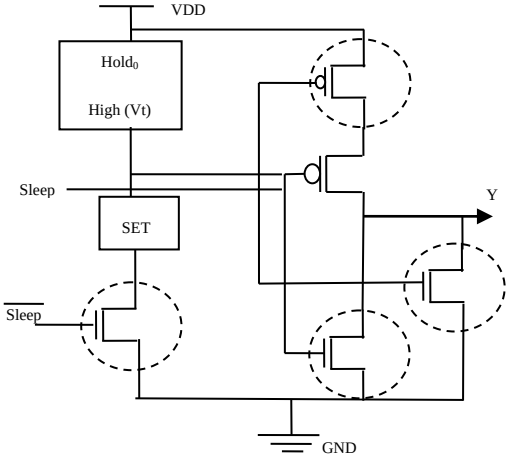

Fig. 2. MTNCL gate structure

B. Multi-Threshold Dual Spacer Dual Rail Delay Insensitive Logic (MTD^{3}L):

The circuit design of MTD^{3}L [15] is alike to MTNCL logic with a requirement of two extra sleep signals (Sleep-0, Sleep-1) as shown in Fig. 3. Depending on the two sleep signals state (S0=S1=0) and the applied input signal the MTD^{3}L circuit functions normal as presented in Table I. In case, if the sleep (S0) is signalized to high state (logic 1) then the design sleeps to zero and similarly if sleep (S1) is transitioned to high state then the design sleeps to one. When the pair of sleep signals is simultaneously set high, then the function of the design will be invalid.

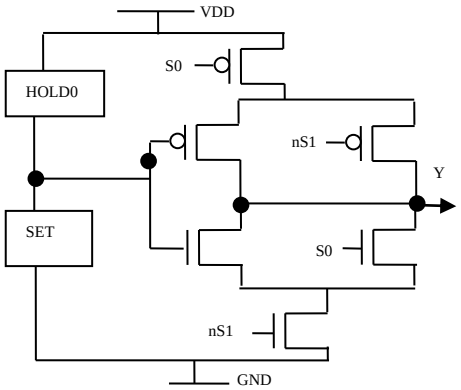

Fig. 3. MTD^{3}L gate structure

TABLE I: MTD^{3}L FUNCTION WITH SLEEP SIGNALS

Sleep Signals		
S0	S1	Output (Y)
Low	Low	Normal
Low	High	All-One Spacer
High	Low	All-Zero Spacer
High	High	Invalid

III. SENSE-AMPLIFIER-HALF-BUFFER (SAHB) LOGIC

SAHB is one of the asynchronous (clock-less) logics with quasi-delay-insensitive (QDI) cell design approach used to attain high performance in terms of speed. SAHB [6, 16] cell makes use of a standard 4-phase handshake protocol. The cell design comprises of evaluation and sense amplifier (SA) blocks which are coupled together to diminish the switching nodes resulting enhanced functioning in terms of less power dissipation. The circuit design of XOR/XNOR cell is shown in Fig. 4 and the design of AND/NAND, OR/NOR cells are shown in Fig. 5. For the cell initialization, the N-type transistor represented in green color with RST is considered to be optional. In the cell design Rack is known as evaluation flow control signal and nRack is reset flow control signal.

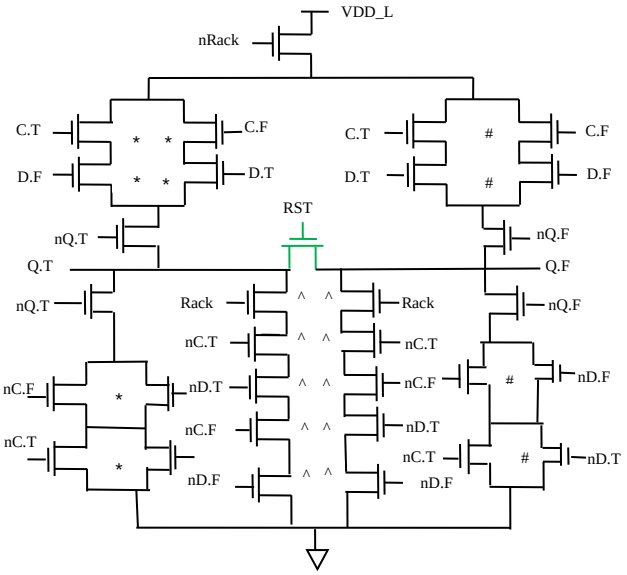

Fig. 4. Circuit schematic for the Evaluation block of 2-input XOR/XNOR

Initially the cell is subjugated to reset condition with all the inputs and their corresponding complementary signals are set to high. For an instance, assume the evaluation phase with D.F=1 (nD.F=0) resulting the N-type pull-up network to charge partially with the voltage at Q.F to VDD_L and Q.T remains 0. As soon as the input to the cell becomes valid, the sense amplifier block as shown in Fig. 6 with cross-coupled latch switches ON due to the direct connection of VDD_v to VDD and magnifies the false rail of output (Q.F) to 1. Accordingly, the false rail of output is clamped and nQ.F results with 0. The efficacy of output (dual-rail) is indicated with the asserted Lack signal to 1 (nLack =0). Similarly, the dual-rail outputs in the reset phase becomes empty with the applied inputs (nC.T and nC.F are 1) and Lack is asserted with 0. Therefore, the new operation of SA [17] block can be performed.

Lastly, the evaluation block and SA block are mutually joined to reduce the number of switching nodes. Thereby, the speed gets improved and leakage current gets reduced.

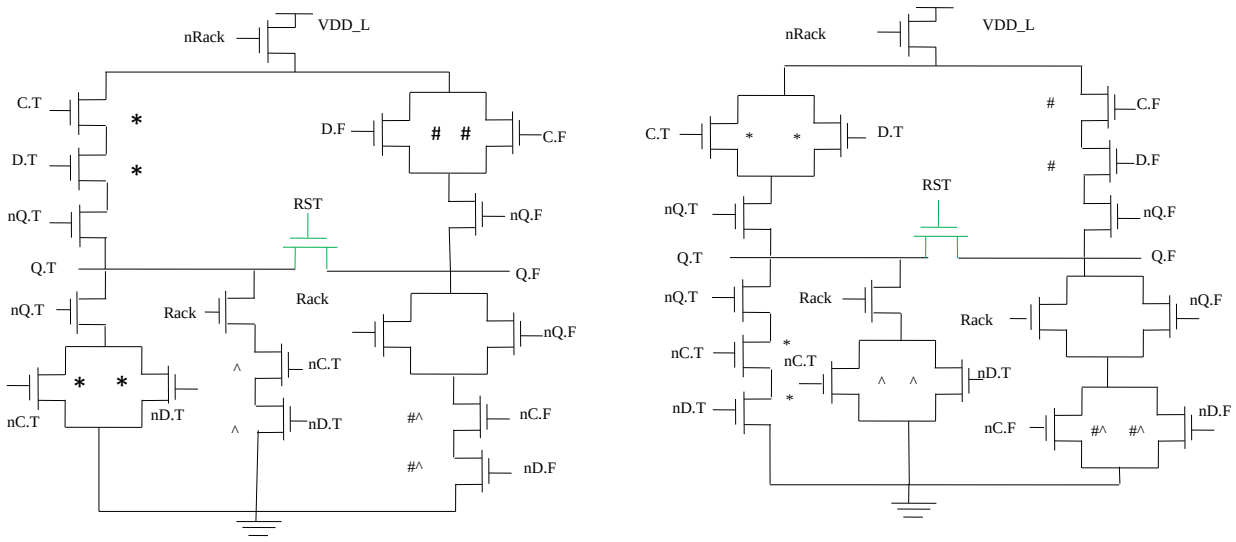

Fig. 5. Circuit schematic for the Evaluation block of 2-input AND/NAND, OR/NOR cells

*, # Series-Parallel Pair ; ^ Input-completeness

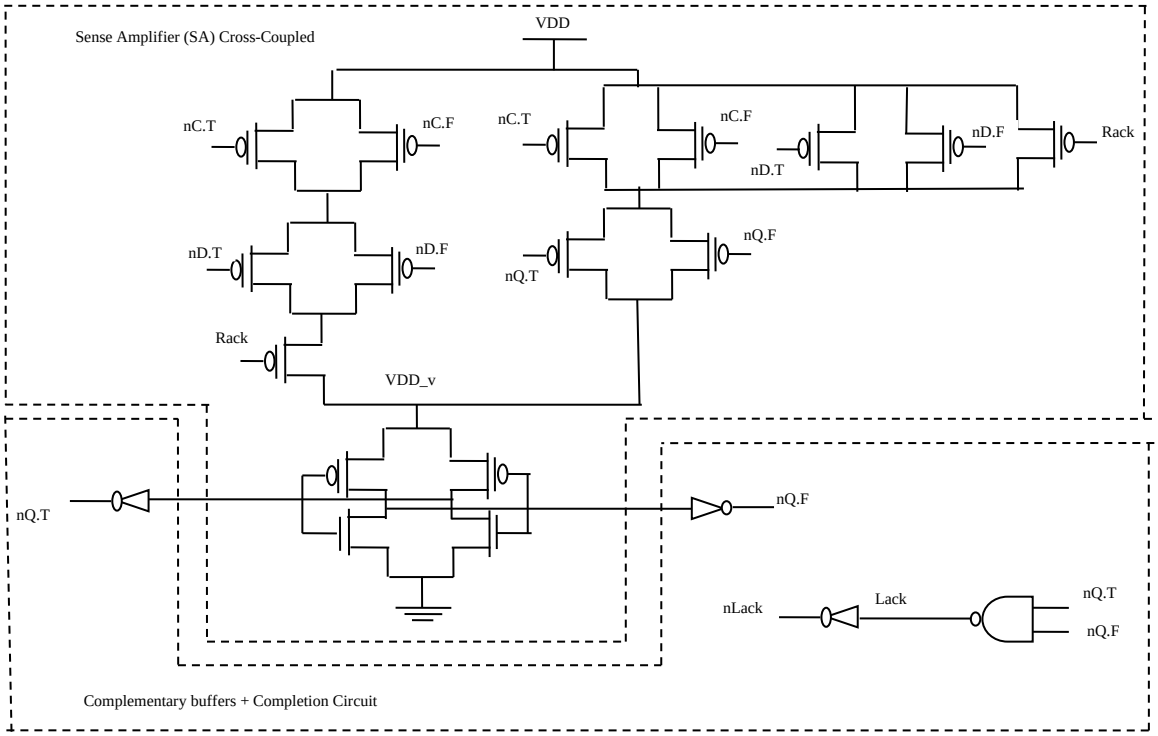

Fig. 6. Circuit schematic for the SA block of AND/NAND, OR/NOR and XOR/XNOR cells includes cross coupled network, complementary buffers and completion circuit.

IV. 8-BIT RIPPLE CARRY ADDER

A ripple carry adder [18, 19] is a logic circuit which is constructed in a cascaded structure using a series of full adder blocks as shown in Fig. 7. The resultant carry that is rippled from one adder is given as input to subsequent full adder. The schematic of full adder using SAHB logic is presented in Fig. 8. The circuit pattern of 8- bit ripple carry adder is done in the series arrangement using 7 full adder blocks and 1 half adder block that performs the addition of two 8-bit binary inputs is shown in Fig. 9. Since an output carry gets rippled towards the next succeeding phase of full adder it is termed as ripple carry adder.

In digital electronics, ripple carry adder is an essential logic circuit used for numerous applications. It is used for the calculation purpose of adding two binary numbers of N-bit by rippling a carry bit in each stage. At last, the result concludes with N bits plus a carry out.

V. RESULTS AND DISCUSSION

This work has been carried out with Mentor Graphics Electronic Design Automation (EDA) tools using 130nm technology. The simulation of the ripple carry adder results the output waveforms of a single rail using SAHB asynchronous logic is shown in Fig. 10. The comparison of three asynchronous techniques MTNCL, MTD^{3}L and SAHB with the performance attributes like power dissipation, delay and energy are presented in Table II.

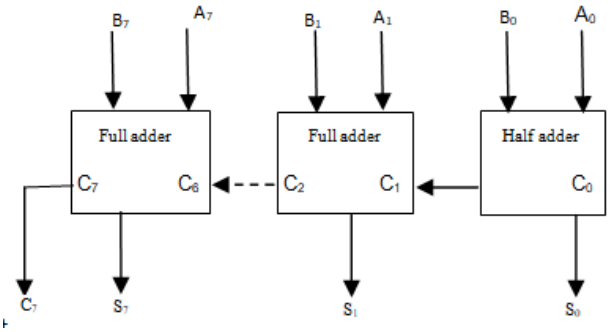

Fig. 7. Architecture of 8- bit Ripple Carry Adder

The equations representing full adder are described by (1):

$$C_{out}^{0} = A^{0}B^{0} + C_{in}^{0}A^{0} + C_{in}^{0}B^{0}$$
$$C_{out}^{1} = A^{1}B^{1} + C_{in}^{1}A^{1} + C_{in}^{1}B^{1}$$
$$S^{0} = C_{out}^{1}A^{0} + C_{out}^{1}B^{0} + C_{out}^{1}C_{in}^{0} + A^{0}B^{0}C_{in}^{0}$$
$$S^{1} = C_{out}^{0}A^{1} + C_{out}^{0}B^{1} + C_{out}^{0}C_{in}^{1} + A^{1}B^{1}C_{in}^{1} \quad (1)$$

The equations representing half adder are described by (2):

$$C_{out}^{1} = A^{1}B^{1}$$
$$C_{out}^{0} = A^{0} + B^{0}$$
$$S^{0} = C_{out}^{1} + A^{0}B^{0}$$
$$S^{1} = C_{out}^{0}A^{1} + C_{out}^{0}B^{1} \quad (2)$$

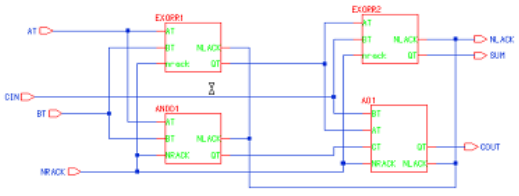

Fig. 8. Full adder schematic using SAHB logic

a) Power Dissipation (PD) : PD in any device is defined as the conversion of source energy in the form of heat. The lifetime and reliability of the circuit decrease with an increase in power dissipation. Due to its switching activity, asynchronous logics have low power dissipation.

The average PD of the static CMOS circuit is:

$$P_{total} = P_{static} + P_{dynamic}$$
$$P_{static} = V_{CC} * I_{CC}$$
$$P_{dynamic} = \alpha * C_L * V_{DD}^{2} * F$$

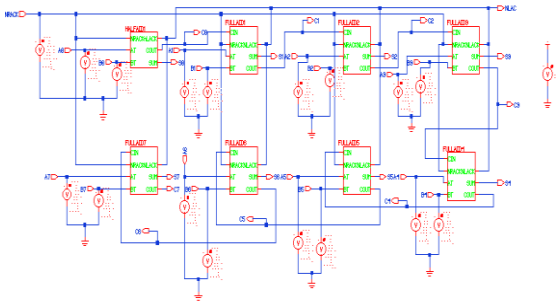

Fig. 9. Ripple carry adder schematic using SAHB logic

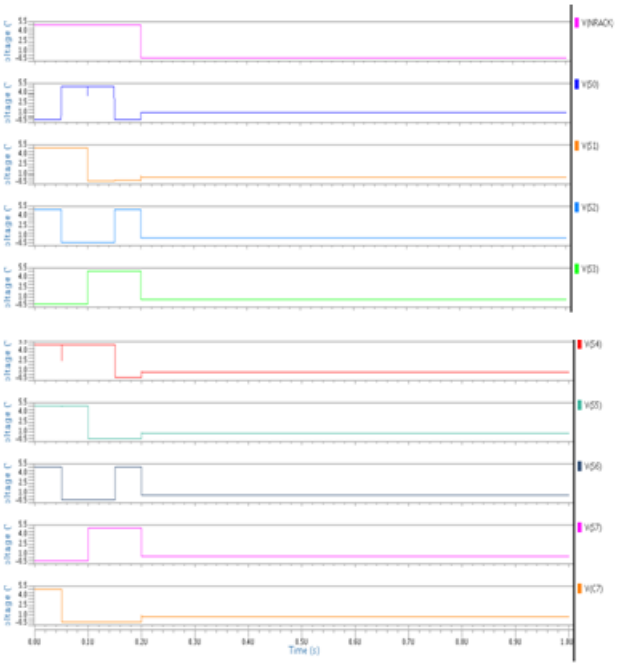

Fig. 10. Waveforms of an 8-bit Ripple carry adder

Where, the entire average power is denoted by "P_{avg}", static power dissipation is known as "P_{Static}" and the dynamic power dissipation of the circuit is denoted by "$P_{Dynamic}$".

b) Delay : In any circuit, propagation or gate delay is delineated as the total time occupied for transmission of an input voltage signal to the output voltage signal of the circuit. Delay is abated to an immense measure in the suggested SAHB asynchronous logic correlated to existing MTNCL and MTD^{3}L logics. The reduction in delay will steadily increase the performance of the circuit.

Energy : In a circuit, energy is exemplified as the product of executing duration and power dissipation. The performance of the design can be measured from the power-delay product. The result of high energy indicates that all leakages are minimized in the circuit. Energy parameter is given by

*Energy = Power * delay*

TABLE II: COMPARISON OF PERFORMANCE ATTRIBUTES FOR VARIOUS ASYNCHRONOUS LOGICS

Parameters	MTNCL	MTD^{3}L	SAHB
Power dissipation (u Watts)	0.202	0.857	2.666
Delay (n Seconds)	299.88	0.175	0.0667
Energy (p Joules)	60.78	1.505	1.78

VI. CONCLUSION

In this research article, a Ripple Carry Adder (RCA) which is of 8-bit has been produced by using different asynchronous logics such as MTNCL, MTD^{3}L and SAHB. As shown in Table II the proposed SAHB logic outcomes with improved performance in terms of speed than the traditional methods. SAHB logic is designed by effectively combining the evaluation and SA blocks to abate the amount of switching nodes ensuing better performance in terms of speed of the circuit with less leakages. Upon comparison, the proposed SAHB method achieves 61.8% of minimum propagation delay and improves the performance of the circuit with speed. Continuing to drive a well-diversified research, to accomplish high performance, there is a scope to expand the circuit design with low power and low leakage techniques like GAELOR and LECTOR that explores solutions to the existing issues in the traditional approaches.

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REFERENCES

1. Kiat Seng Yeo, Kaushik Roy, Low Voltage, Low Power VLSI Subsystems, Tata McGraw Hill, 2005.
2. Pal, Ajit, Low-Power VLSI Circuits and Systems, Springer
3. Sivakumar, R., Jothi, D.: Recent trends in low power VLSI design. IJCEE 6, 869 (2014).
4. N. N. Tan, D. Li, and Z. Wang, Ultra-low power integrated circuit design. Springer, 2014, vol. 1801466741.
5. Hematha S , Dhawan A and Kar H , "Multithreshold CMOS Design for low power digital circuits" TENCON 2008-2008 IEEE Region 10 Conference,pp.1-5,2008.
6. Multi Objective Analysis of Standard Cells Using Sense Amplifier Based QDI Approach S. Jhansi Rani 1 , Dr. J. Sudhakar2 ,IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 13, Issue 4, Ver. I (Jul.-Aug. 2018).
7. Lars S.Nielsen, CeesNiessen, Jens Sparso, and Kees van Berkel, "Low-Power Operation Using Self-Timed Circuits and Adaptive Scaling of the Supply Voltage", IEEE Transactions on Very Large Scale Integration (Vlsi) Systems, Vol. 2, No. 4, December 1994.
8. Shin'ichiro Mutoh, TakakuniDouseki, Yasuyuki Matsuya, Takahko Aoki, Satoshi Shigematsu, and Junzo Yamada, "I-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS", IEEE Journal of Solid-State Circuits, Vol. 30, No. 8, August.1995
9. Alice Wang , Benton H. Calhoun, Anantha P. Chandrakasan, "subthreshold Design for Ultra LowPower Systems", Springers US, 2006.
10. B.H. Calhoun, F. A. Honore, A. p. Chandrakasan , "A leakage reduction methodology for distributed MTCMOS", IEEE Journal of Solid-State Circuits ISSUE 5, May 2004, pp.818-826.
11. S. C. Smith, R. F. DeMara, J. S. Yuan, D. Ferguson, and D. Lamb, "Optimization of NULL Convention Self-Timed Circuits," Elsevier's Integration, the VLSI Journal, Vol. 37/3, pp. 135 165, August 2004.
12. J.Sudhakar, A.Mallikarjuna Prasad and Ajit Kumar Panda, "Behavior of Self Timed Null Convention Logic Circuits with Threshold Variations", international Journal of Emerging Trends in Engineering Research (IJETER), Vol. 3 No.6, Pages : 173-179 (2015)
13. Liang Zhou, Ravi Parameswaran, Farhad A. Parsan, Scott C. Smith, Jia Di, "Multi-Threshold NULL Convention Logic (MTNCL): An UltraLow Power Asynchronous Circuit Design Methodology", J. Low Power Electron. Appl. 2015, 5, 81-100; doi:10.3390/jlpea5020081.
14. Farhad. A. Parsan and Scott. C. Smith, "CMOS Implementation Comparison of NCL Gates," IEEE Int. Midwest Sym. on Circuits and Systems (MWSCAS), Aug. 2012.
15. Michael Linder; Jia Di; Scott C. Smith. "Multi-Threshold Dual Spacer Dual Rail Delay Insensitive Logic: A Low Overhead Secure IC Design Methodology". J. Low Power electron. Appl. 2013, 3, 300-336.
16. Kwen-Siong Chong, Weng-Geng Ho, Bah-HweeGwee, Tong Lin, and Joseph S. Chang, "Sense Amplifier Half-Buffer: Low-Power High-Performance Asynchronous Logic QDI Cell Template, IEEE Transactions on VLSI Systems 1063-8210 c 2016
17. K.-S. Yeo, W.–L. Goh, Z.–H. Kong, Q-X.Zhang and W.–G. Yeo IEEE, Svst. „High-performance low-power current sense amplifier using a cross-coupled current-mirror-configuration" Proc.–Circuits DeGice.7, 2002.
18. Saraswat R., Akashe S., Babu S. (2013) Analysis and Simulation of Full Adder Design Using MTCMOS Technique. In: Bansal J., Singh P., Deep K., Pant M., Nagar A. (eds) Proceedings of Seventh International Conference on Bio-Inspired Computing: Theories and Applications (BIC-TA 2012). Advances in Intelligent Systems and Computing, vol 202. Springer, India.
19. Balasubramanian, P. & Yamashita, Area/latency optimized early output asynchronous full adders and relative-timed ripple carry adders S. SpringerPlus (2016) 5: 440. https://doi.org/10.1186/s40064-016-2074-z.