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An Efficient Architecture of Vedic Multiplier using FinFet Based Pass Transistor Logic

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Abstract: ***Multiplies is an important component in Digital Signal Processing (DSP) and communication systems. It is utilized in signal and image processing applications including convolution, Fast Fourier Transform (FFT) and correlation. Therefore, it is necessary to develop a multiplier with power efficient and speed to reduce the cost of the system. Vedic multiplier has been introduced to solve the problems of existing multiplier. It is based on 16 algorithms. These algorithms use algebra, arithmetic operations and geometry. Urdhva Tiryabhyam is widely employed formula which provides high speed and efficient. Vedic multiplies generates partial sums and products in single step. It has been designed using pass transistor logic which reduces the number of components utilized to build logic gates by removing unwanted transistors. This paper design a vedic multiplier with FinFET based pass transistor logic. The developed multiplies provides better performance and suitable for high speed applications. 2x2 and 4x4 vedic multipliers are developed and executed 180nm approach with Tanner EDA Tool 3.0.***

Index Terms: ***Vedic Multiplier, FinFET based Pass Transistor, High performance, Low power optimized circuit.***

I. INTRODUCTION

CMOS technology dominates VLSI and other logic families. But, this technology has some drawbacks which have been solved. For an instance, the process technology has reduced the size from 180nm in 1999 to 60nm in 2008. Now it is reduced to 45nm. Several attempt being made to reduce it 32nm. However, die area shrunk during 2008 now is increasing due to the more number of transistors and its features. A multiplier is an important parameter which is utilized in various electronic systems like DSP. Filtering, ALU, Image Processing and etc. High speed and low power multiplier has been in an increasing demand day-by-day. Multiplier like Array multiplier, Booth multiplier, Bit serial multiplier, Carry Save multiplier and etc. are used for as source of the algorithms. Vedic multiplies with different architecture is designed using carry save adder and ripple carry adder. Performances are compared and their merits and demerits are identified with respect to speed and area focused in [2],[3]. Adiabatic logic is utilized to minimize power consumption of Vedic multiplier and its performance is estimated by comparing it with traditional MOS design. Vedic multiplier with adiabatic logic consumes less power than Vedic multiplier without adiabatic logic analysed in [6],[7].

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Power consumption is a crucial factor than efficacy the Fin-type field-effect transistors (FinFETs) are good candidate for bulk CMOS at the Nano scale in composed in [4],[10],13].FinFET implies Fin Field Effect Transistor.The power and zone productive plan of full adder with 6 transistors utilizing proposed 2 transistors XOR gate has been displayed in [4],[10].The pass transistor is used to decrease the transistor count for any implementation logics utilizing privacy input to drive gate terminals, source and drain terminals. The main advantage is the use of FinFET which provide numerous profits and advantages over the bulk CMOS [1][8][9][14].

II. VEDIC MULTIPLIER

Sri Bharti Krishna Fhirthaji (1884-1960) was the person to discover the 16 sutra (algorithm) after the intense research on Arthira Sutra. An ancient Vedic mathematical algorithms are employed to solve various types of Mathematical operations like additions, subtractions, multiplications, divisions, fabrications etc. This mathematic is used to speed up the computation by cutting down the process complexity [2][3]. Two Sutrasout of sixteen are utilized to perform multiplication namely UrdhvaTiryabhyam Sutra and NikhilamNavatashcaramamDashatah Sutra. UrdhvaTriyabhyamvedic multiplier sutra is used in this paper.

A.Urdhva Triyabhyam

Urdhva Tiryabhyam was derived from a Sanskrit word. It means vertically and crosswise**.** This multiplication achieves high speed by computing partial sums and products in a step. The main advantage is that this sutra is simple and saves time while solving the problem. It can be utilized multiplications of 2*2, 3*3 and B*B upto N*N bit [5][6][14].

B.Pass Transistor Logic

The pass transistor logic is used to decrease the transistor count in any logic or in CMOS logic inputs are used to drive gate terminals, source and gate terminals [1]. In this paper, the circuits are driven with the help of the primary input itself by design AND gate and other design.

C.FinFET Technology

The main use of this technology is to get an advantage than bulk CMOS such as higher drive current for a given transistor footprint and lower leakage [4]. There are two working modes of FinFET, they are as follows.

1. Shorted Gate (SG)

In this gate, front and back gates are shorted whereas is SG FinFET, the gates are isolated in the below Fig1.

(a). These both isolated gates are jointly employed to control the electrostatic of the channel. Thus, SG FinFET's give higher on and off current compared to these of IG FinFETs [10][11][13]. The work functions of both the front and back gates of a FinFET are the source.

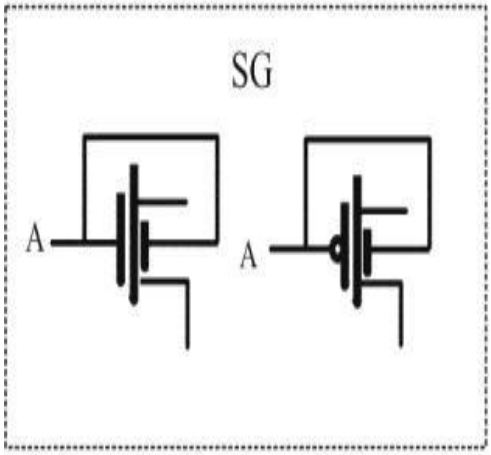


Fig 1.(a)Structure of SG – FinFET

2. Independent Gate (IG)

In this mode, the upper part of the gate is eliminated and then 2 independent gates are formed. The front and back gate are to two different inputs. It forms 4 terminals. IG produces the flexibility of adopting various signal to their 2 inputs which allows to utilized back gate bias to simulate front gate (V_{TH}) linearity [10][11][13]. Fig.1(b) shows the structure of 1G FinFet.

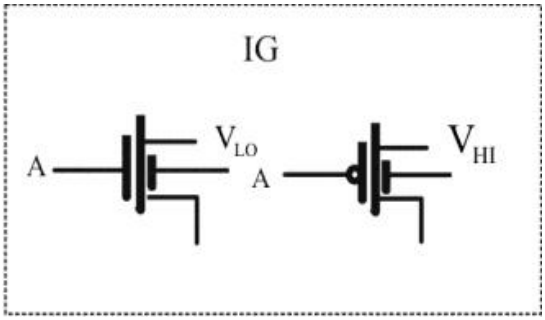


Fig 1.(b) Structure of SG – FinFET

III. CIRCUIT DESCRIPTION

Half adder, full adder and AND gate are used to implement Urdhva Tiryabhyam. In the following section, details of the above mentioned components are discussed.

A.AND Gate

AND is an operation where the outputs becomes high / true when all the inputs are true and this AND gate can be a two input or multiple inputs based on the requirements. AND gate can be called as Sequential check gate i.e., if we want to check a condition in which two sequential signals should be true these the two input signals can be connected to AND gateand output of AND gate can be takes as controlling command.

Fig.2. (a) depicts the structure of developed 3T AND gate. In optimized 3T AND gate, first NMOS gate is joined to second NMOS source and vice versa. The inputs are fed to both the NMOS and output is observed via drain. PMOS terminals, gate and source are connected to ground. An optimized AND gate can be designed using FinFETTechnology. The simulated output for 3T AND gate is presented in Fig 2.(b)

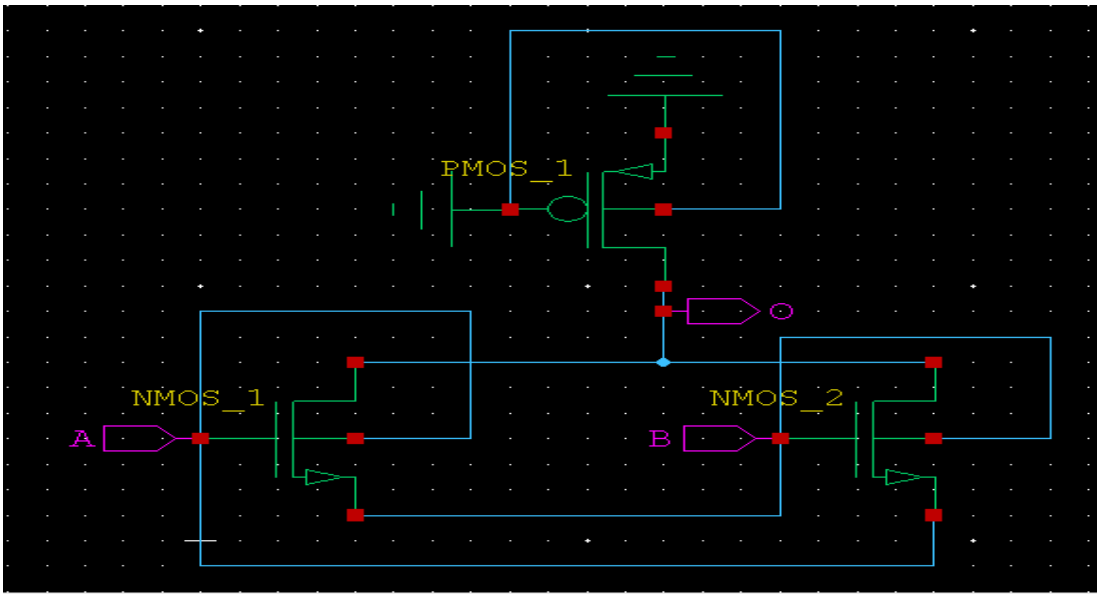


Fig 2. (a).The Proposed design of 3T-AND gate using SG-FinFET.

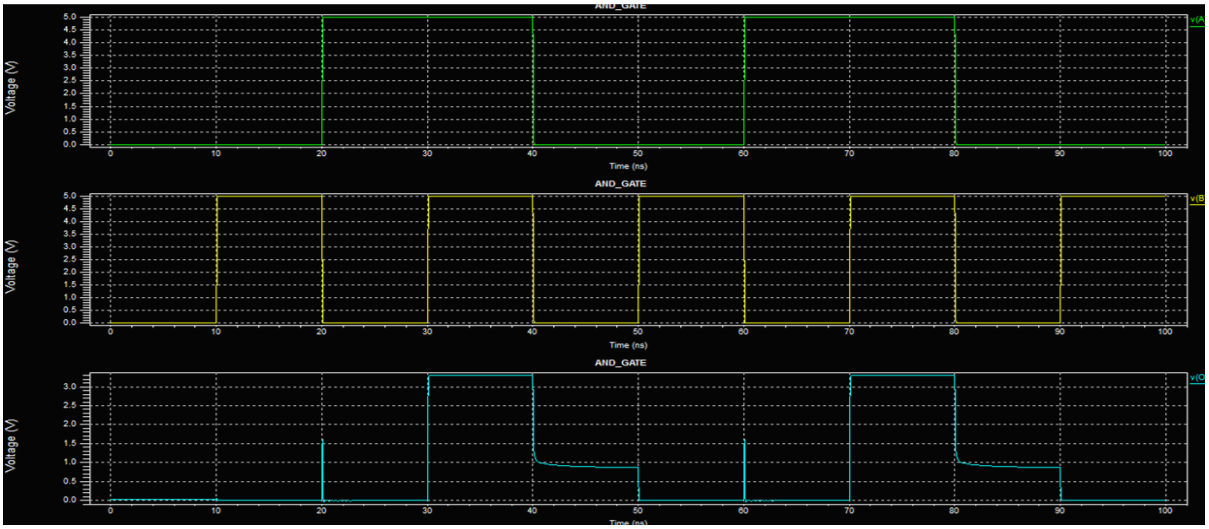


Fig 2. (b).Stimulated Output Waveform for 3T-AND gate

B.Half Adder

Half adder designed by combination of logic gates, It is simple and developed untilizing and XOR and a multiplexer in which XOR produces the sum and the multiplexer produces the carry. 10 transistor full adder designed with fusion of several XOR and modules.

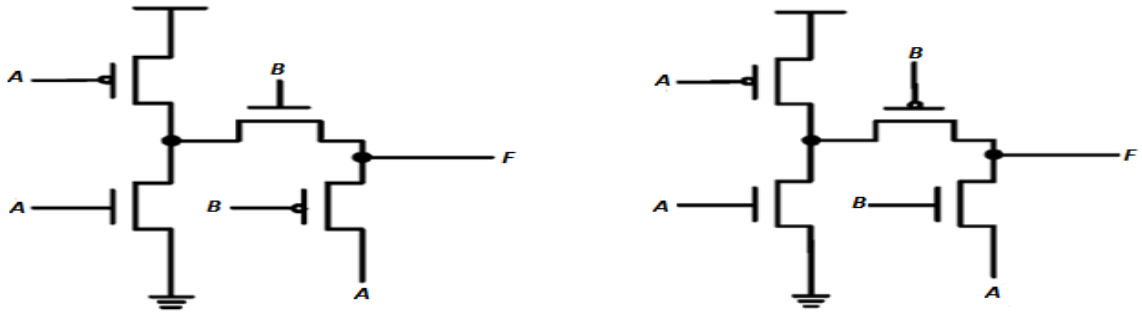


Fig 3.(a).Schematic Diagram for 4T XOR gate

The XOR circuit with four transistor is presented in Fig 3.(a) and this when connected with multiplexer gives an half adder circuit. A schematic of 6T half adder where 4T XOR gate is to generate carry. 4T XOR gate is used to act as inverter whenever input B is at logic high then output of XOR is inverted form of A and whenever input B is at logic low PMOS turnsON and NMOS turns OFF so output carry is equal to A.When sum is high, then PMOS turns OFF and NMOS turns ON so output carry gives low (ground).The proposed design of 6T half adder design and stimulated output as shown in Fig 3.(b) and Fig 3.(c).

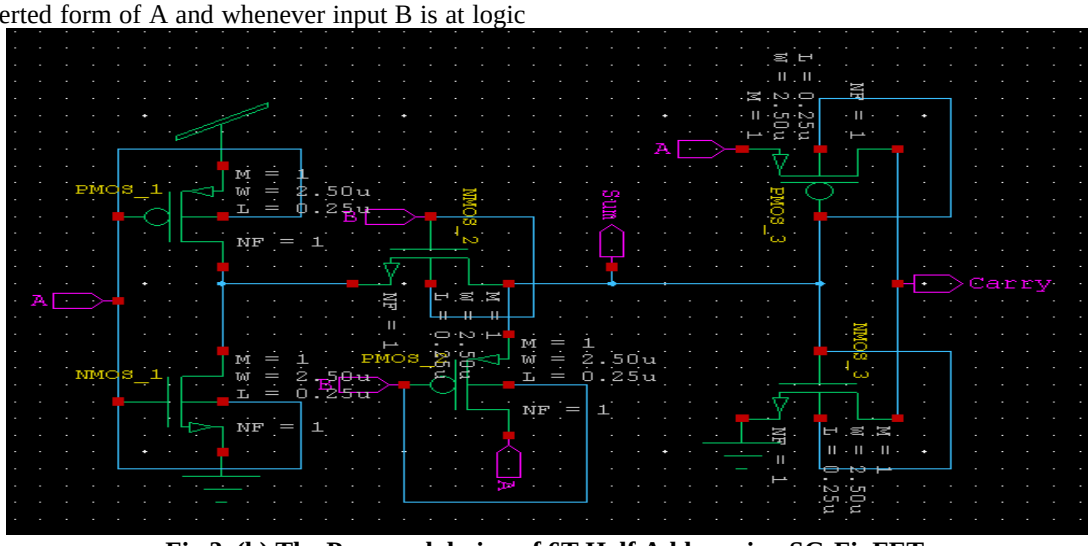


Fig 3. (b).The Proposed design of 6T Half Adder using SG-FinFET

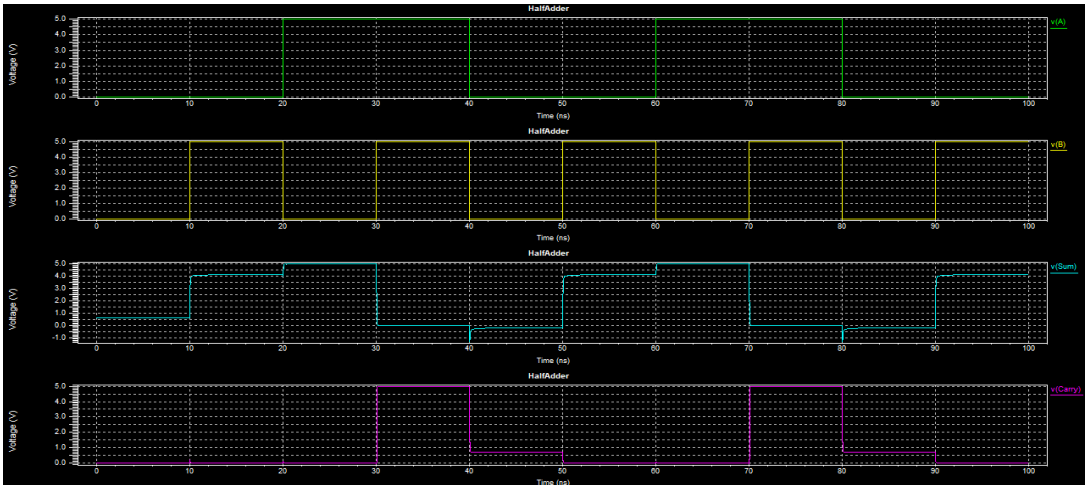


Fig 3. (c).Stimulated graph for 10T Half Adder

C. Full Adder

Full adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as Cin. The output carry is designated as Cout and the normal output is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another.

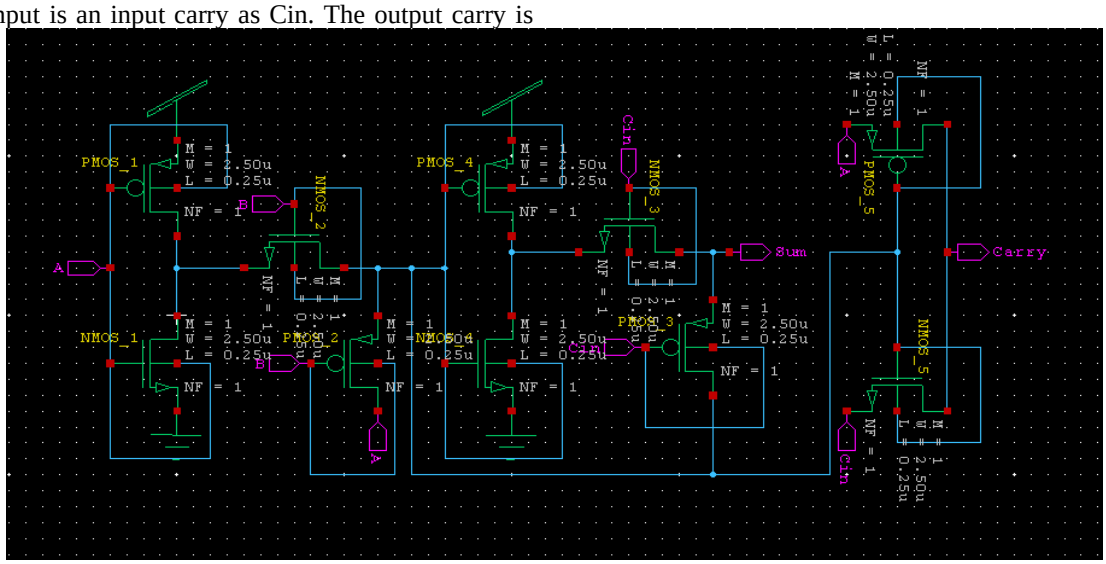


Fig 4.(a).The Proposed design of 10T Full Adder using SG-FinFET

The above diagram shows the 10T full adder while 2 3T XOR gates are utilized which would produce sum and one 2T MUX is used which is controlled by the first two inputs which in return produce the carry. It operates as such than whenever inputs A and B are same then sum is equal to third input Cin and carry is equal to A. Whenever inputs A and B are different sum will be equal to inverted form of Cin and carry is equal to Cin. The stimulated output as shown in Fig 4.(b).

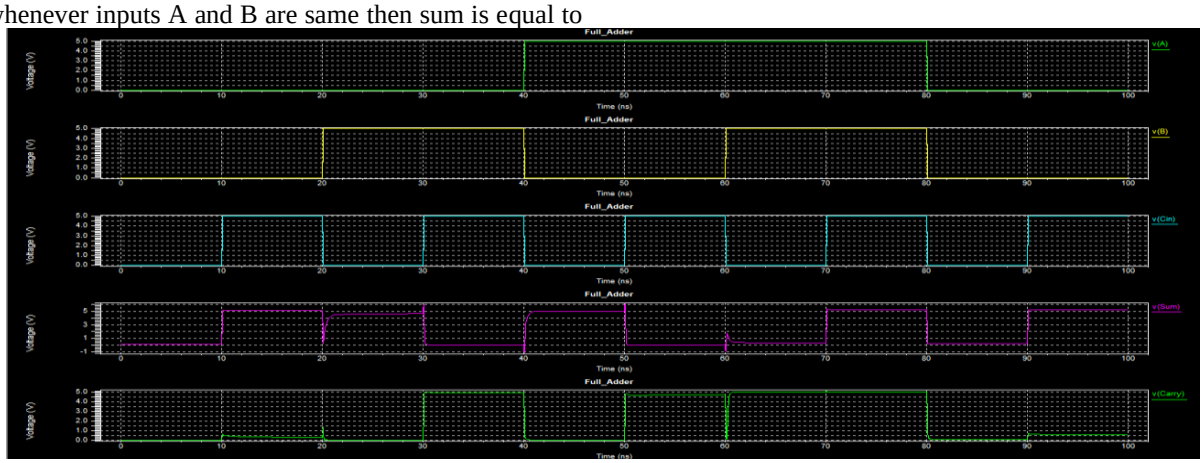
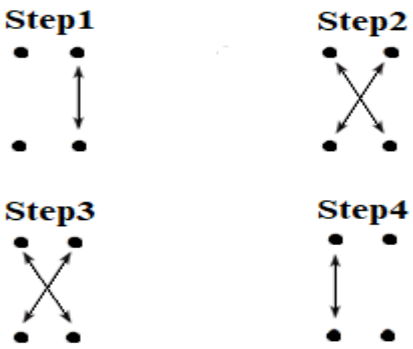


Fig 4.(b).Stimulated Output for 10T Full Adder

D.2X2 Vedic Multiplier

Urdhva Tiryabhyam sutra's refers vertically and crosswise multiplication is demonstrated in Fig 5.(a). First the LSB bit of both the inputs are multiplied vertically using the AND gate then the centrepairs of bits are crosswise multiplied and lastly the last pair of MSB bits of both inputs are multiplied vertically [14][15]. Finally all the products are connected to half adder as shown Fig 5.(b).



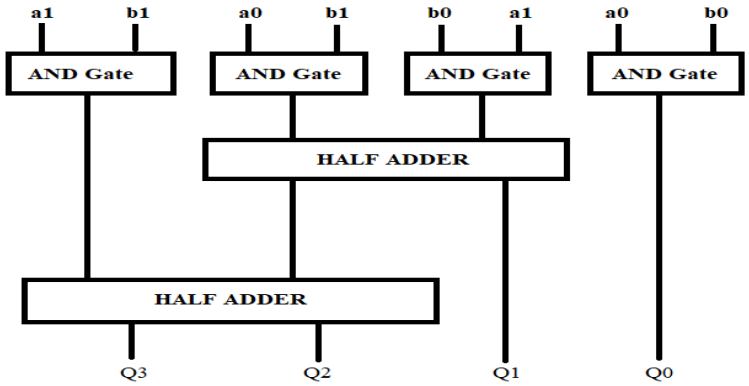


Fig 5.(a) Urdhva Tiryagbhyam Using 2-Digits Number Fig 5.(b) 2X2 Vedic Multiplier

The above diagram of 2x2 Vedic multiplier shows which consists the AND gate for 2-bit multiplication with 2 half adder for addition. The output produced is of 4 bits with one as carry is demonstrated in Fig 5.(c).

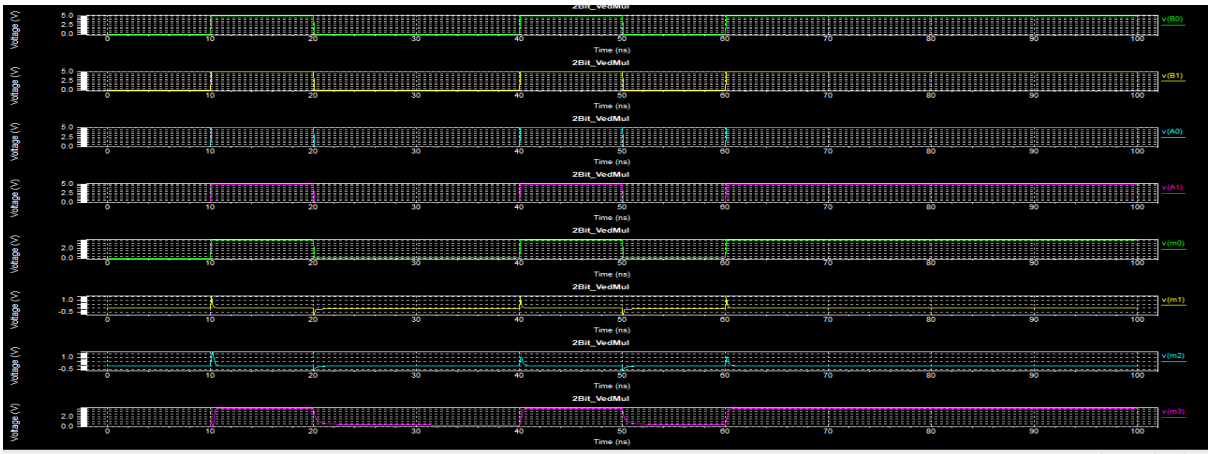


Fig 5.(c) Stimulated Output for 2x2 Vedic multiplier

E.4X4 Vedic Multiplier

2X2 Vedic multiplier is utilized to design 4X4 Vedic multiplication. It is a crucial part of the designed multiplier. Consider 4 bit numbers such as $A_0A_1A_2A_3$ and $B_0B_1B_2B_3$ as described in the formula as in Fig 6. (a). In this sutra, bits are grouped as a two bit pair and first step is of multiplying the LSB bits and similarly with the MSB bits. The centre two pairs are multiplied crosswise [6][8][9]. The 4x4 Vedic multiplier structure presented in Fig 6.(b) and the stimulated outputs are as illustrated in Fig 6.(c) and Fig 6.(d).

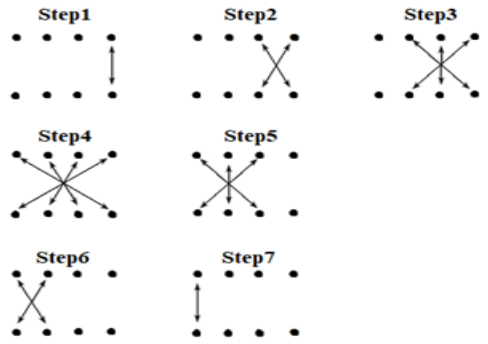


Fig 6.(a). Urdhva Tiryagbhyam Using 4-Digits Number

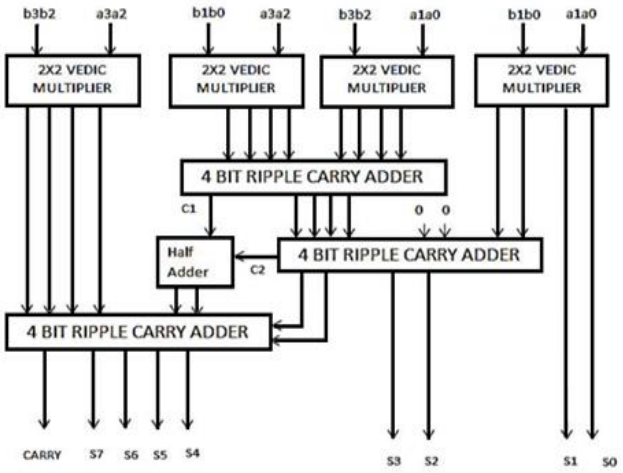


Fig 6.(c). Proposed design of Adiabatic 4x4 Bit Vedic multiplier

The simulated output graph of the four Bit Vedic Multiplier is as demonstrated below.In Figure, the output is checked with a sample input of taking all the inputs as 1's and getting the Output as 10000111.

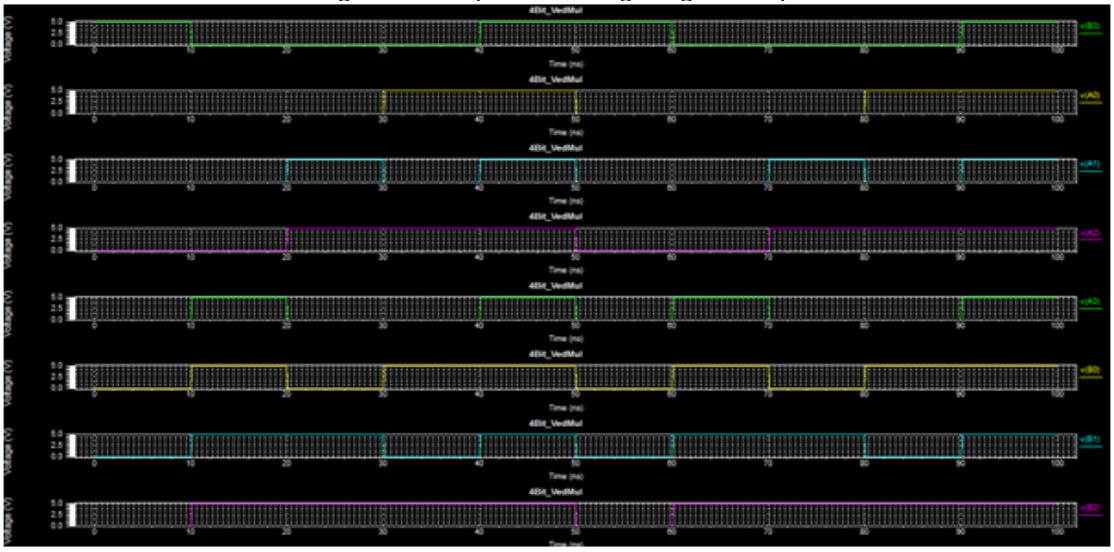


Fig6.(d) shows the output waveform for the inputs given in 4X4 bit Vedic Multiplier.

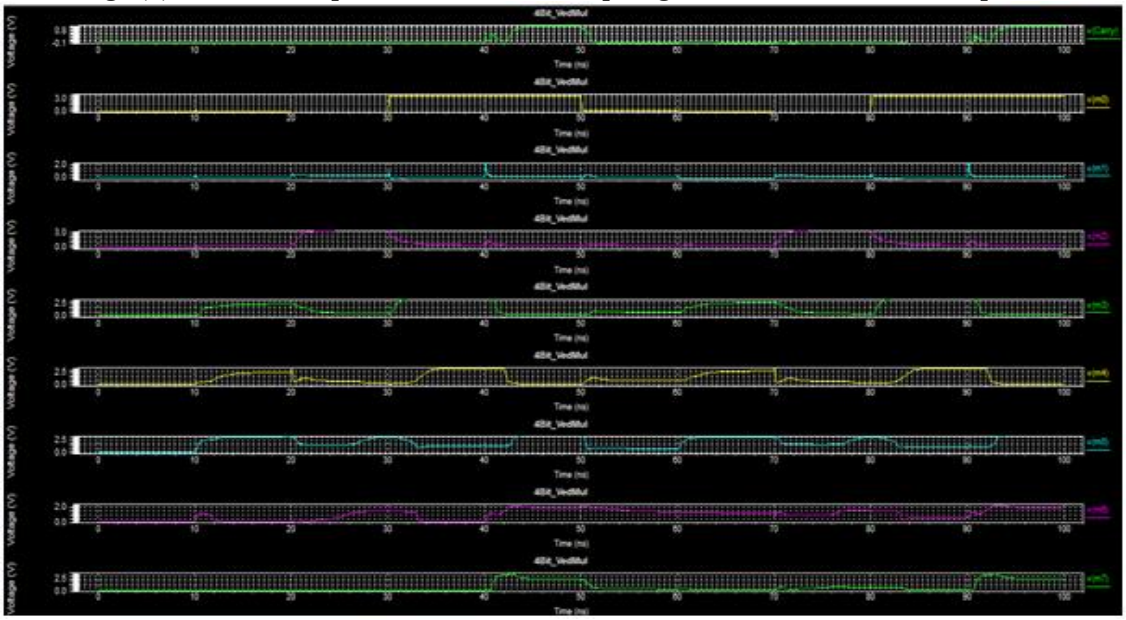


Fig6.(e). Output Waveform of 4-Bit Vedic Multiplier

To obtain overall output (S7 S6 S5 S4 S3 S2 S1 S0), 4 2x2 bit Vedic multiplier and 3 4-bit Ripple-Carry. From the results, it is found that the proposed multiplier has the potential to reduce the delay. In literature, most of the Vedic multiplier has the structure of array. This paper presented architecture. The proposed architecture is efficient with respect to speed.

The proposed Vedic multiplier can be used to reduce delay. Early literature speaks about Vedic multipliers based on array multiplier structures. On the other hand, we proposed a new architecture, which is efficient in terms of speed.

IV. RESULT AND CONCLUSION

The proposed multiplier is implemented on ISIM. The proposed architecture of Vedic multiplier is verified by software Tanner EDA Tool V13.0.Performance of the proposed Vedic multiplier is validated and its operations are tested by observing experimental results. From the results, it is observed that the combinational delay is minimized with a trade off related to area.

Comparison and Power Analysis

Power dissipation is one of the most important constraints during the design of any circuit. The mobile device consumer requires advanced features and long lasting battery at low price. But, modern technology needs more power. In both logic and memory, static power is increases rapidly and dynamic power is rises which resulted in increased total power. However, still research is going on to reduce power dissipation and meet the requirements of customer. Optimization of power can be done at different abstract levels and one such optimization of power is done in this proposed project work.

Table 1. Comparison of Power of Vedic Multiplier

Circuit Design	Existing methodology(CMOS logic)(W)	Proposed Methodology(Fin FET Logic)(W)
2X2 Bit Multiplier	3.52962 x e-003	2.182973 x e-003
4X4 Bit Multiplier	24.6211 x e-003	14.080295 x e-003

The power is compared between existing methodology which was read as 3.52e-003 in 2 bit and 24.62e-003 in 4 bit and that proposed methodology's circuit design is 2.182e-003 and 14.0802e-003 respectively. The power consumption has been reduced to about 38% and 42% in two bit and four bit Vedic multipliers respectively. Change in power dissipation has been drastically reduced and this shows the success of this proposed design.

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