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Performance Analysis of Three Phase Multilevel Inverter with SPWM Techniques used in Railway System

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Abstract: ***The medium voltage & high power converters are used in electrical railway system because of its high efficiency. Due to the use of heavy load in the railway system, conventional inverters causes power quality issues such as harmonic distortion, low power factor, etc. In this paper, new cascaded multilevel inverter (MLI) using cascaded H-bridge is introduced. The advantage of the proposed method is to mitigate power semiconductor switches in number which reduces the cost of the circuit as well as the complexity. The analysis and evaluation of various Sinusoidal Pulse Width Modulation (SPWM) Methods with different levels of an inverter has been modeled and simulated by using MATLAB/Simulink.***

Keywords: Induction Motor, LC filter, Three-phase inverter, SPWM techniques.

I. INTRODUCTION

A railway system has a main application in the transportation of goods and people all over the world. Traction system means the use of electricity to drive a railway known as the locomotive system instead of conventional railways which use fossil fuels. This advantage is to reduce the greenhouse gases, provide a clean eco-friendly environment and ease of control. Power electronic converters have found wide application in the railway system due to medium as well as high power and frequency control [1]. In a railway system, the use of Induction motor is more preferred because of steep speed-torque characteristics and regenerative ability [2].

Considering three-phase induction motor for electrical railway traction over DC motor because of absence of commutator and brushes. Hence the system becomes more efficient, more reliable and reduces the maintenance cost. It is also robust in construction, less expensive and has high overload capabilities [3]. 3-Ø inverters for railway system are the important power handling component between the DC line & electric motor. Generally, to design traction inverters it requires: high reliability, high efficiency, economical and higher power density [4].In two-level pulse width modulation (PWM) main disadvantages are low efficiency at the higher switching frequency, maximum voltage stress across switches, a higher harmonic distortion which leads to additional auxiliary resonant circuitry. To overcome these limitations Multi-Level Inverter (MLI) is introduced for medium voltage & high power railway system. The MLI is an advantage in the electric railway system, which is capable of operating in higher switching frequency with minimum Electro-Magnetic Interference (EMI) level [5]. MLI converts sine wave into a stepped waveform having a large no. of steps. MLI has multi input DC voltage sources. The output voltage from an inverter is a different combination of these input voltage sources. Therefore the output waveform is in a stepped form which is reaching to a sinusoidal waveform. These steps represent different levels of the multilevel inverter. MLI topologies such as DCMLI, FCMLI & CSMLI are discussed and represented in research papers [6-7].The main disadvantage of conventional MLI is when we increase the no. of steps in output voltage, makes it complicated. A new topology of Cascaded H-bridge inverter is introduced by researchers to reduce the number of components [8-9].

Considering the above problems, in this paper a new multilevel inverter topology is introduced. This new MLI topology is modeled and simulated in MATLAB/Simulink. Different modulation methods are used to analyze the performance of the new multilevel inverter.

II. DEVELOPED MULTILEVEL INVERTER

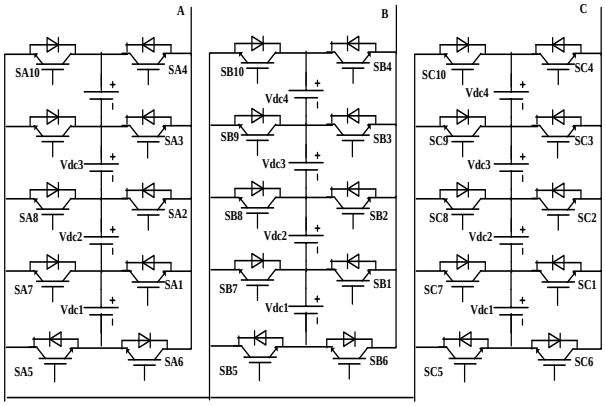

Fig. 1.Three-Phase Nine Level Inverter topology

The proposed topology is a modification of traditional H-bridge MLI. The number of stages increased by stacking, requires specific arrangement of switches & voltage sources.

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Switches S4, S5, S6 & S10 represent H-bridge & S1, S2, S3, S7, S8 & S9 are adjoined to increase the number of levels

The relationship between the number of output level & the number of components are situated in table 1. It is illustrated that this topology is more suitable for the odd number of output level.

Table- I: Components Required for MLI Topology.

Sr. No.	No. of Level (N)	No. of Switches $(m+1)$	No. of Sources $\frac{(m-1)}{2}$
1	3	4	1
2	5	6	2
3	7	8	3
4	9	10	4

Where 'm' is the level of (line to line) output voltage. The table 1 shows Multilevel topology design for a 9-level, it requires (9+1=10) switches and (9-1/2=4) voltage sources for single phase. In general, traditional single-phase MLI requires 16 switches.

III. OPERATION OFDEVELOPED MLI

To implement a 9 level staircase output voltage, consider any one phase of the three-phase inverter. The switching modes and respective levels of the output voltage is shown below

A. Positive staircase voltage level:

- When all switches are OFF, the o/p voltage is at a zero level.
- When switch S1 & S5 is ON then the o/p voltage of level +Vdc1is generated.
- .When switch S2 & S5 is ON, the o/p voltage of level Vdc1+Vdc2 is generated.
- When switch S3 & S5 is ON, the o/p voltage of level Vdc1+Vdc2+Vdc3 is generated.
- When switch S4 & S5 is ON, the o/p voltage of level Vdc1+Vdc2+Vdc3+Vdc4 is generated.

B. Negative staircase voltage level:

- When switch S7 and S6 is ON then the o/p voltage of level -Vdc1 is generated
- When switch S8 and S6 is ON, the o/p voltage of level –Vdc1-Vdc2 is generated.
- When switch S9 and S6 is ON, the o/p voltage of level -Vdc1-Vdc2-Vdc3 is generated.
- When switch S10 and S6 is ON, the o/p voltage of level -Vdc1-Vdc2-Vdc3-Vdc4 is generated.

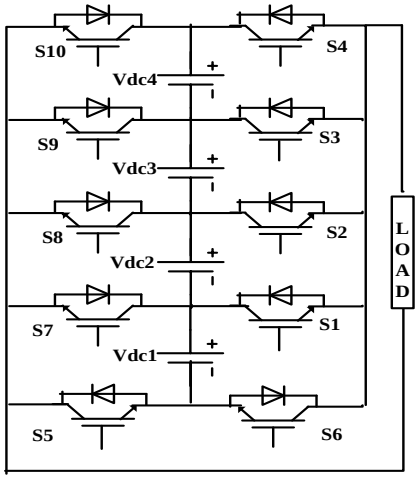

Fig. 2. Single Phase Nine Level Multilevel Inverter topology.

Table II shows the Switching stages of 9 level inverter. Where, Condition 1 means the switch is in 'ON' state & Condition 0 means the switch is in 'OFF' state

IV. MODULATION TECHNIQUES FOR MLI

This paper uses multi carrier SPWM method [10].In order to get the triggering pulse for switches, the reference waveform (*i.e.* sinusoidal wave) and carrier waveform (i.e. triangular wave) is compared. The N-level inverter has required $(m-1)$ carrier waves with the same amplitude & frequency. The level shifting SPWM techniques are further categorised as:

- Phase Disposition (PD)
- Phase Opposition Disposition (POD)
- Alternative Phase Opposition Disposition (APOD)

Table II: Switching Table for 9 Level Inverter

Voltage levels	Switching Stage									
	S1	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	*S9*	*S10*
$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$	0	0	0	1	1	0	0	0	0	0
$V_{dc1}+V_{dc2}+V_{dc3}$	0	0	1	0	1	0	0	0	0	0
$V_{dc1}+V_{dc2}$	0	1	0	0	1	0	0	0	0	0
V_{dc1}	1	0	0	0	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0
$-V_{dc1}$	0	0	0	0	0	1	1	0	0	0
$-V_{dc1}-V_{dc2}$	0	0	0	0	0	1	0	1	0	0
$-V_{dc1}-V_{dc2}-V_{dc3}$	0	0	0	0	0	1	0	0	1	0
$-V_{dc1}-V_{dc2}-V_{dc3}-V_{dc4}$	0	0	0	0	0	1	0	0	0	1

$$m_f = \frac{f_{cc}}{f_m} \quad (1)$$

$$m_a = \frac{A_m}{(m-1)*A_c} \quad (2)$$

For Carrier wave frequency (f_{cr}) = 5 kHz, Reference wave frequency (f_m) = 50Hz.

The Frequency Modulation Index (m_f) = 100 and Amplitude Modulation Index (m_a) = 0.6

- Phase Disposition (PD)

In PD method, all carrier waves are selected with same phase.

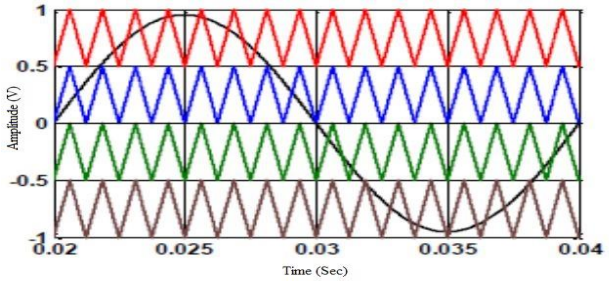

Fig. 3. PD Modulation Method

- Phase Opposition Disposition (POD)

In POD technique, the whole carrier wave above the zero axis is out of phase with below zero axis by 180^0.

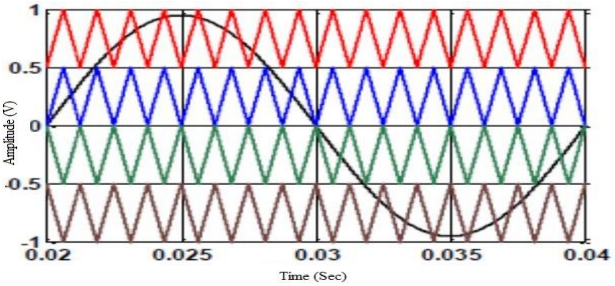

Fig. 4. POD Modulation Method

- Alternative Phase Opposition Disposition (APOD)

In APOD, each carrier wave is phase shifted by 180^0 from its neighbouring wave.

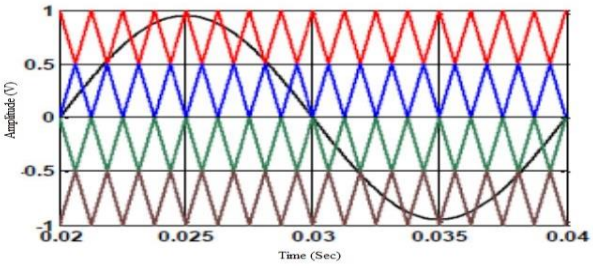

Fig. 5. APOD Modulation Method

V. SIMULATION & RESULT

In this paper total harmonic distortion (THD) is calculated & studied at different levels of MLI for induction motor topology. The simulation model is developed in MATLAB/ Simulink software. The rating and the speed of the motor is 33 kW and 1500 rpm respectively. This motor is fed with 5, 7 and 9 level MLI with different SPWM techniques and THD is observed.

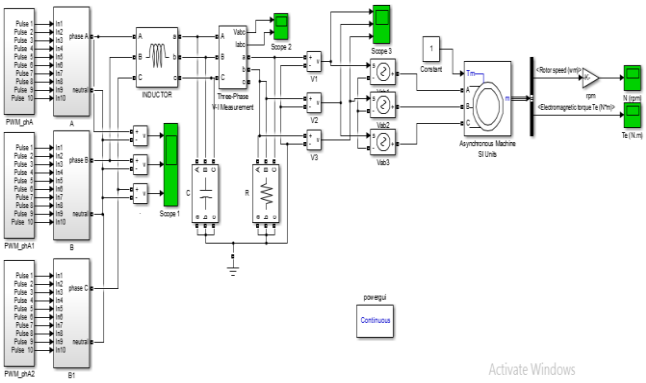

Fig. 6. Simulation Circuit for Induction Motor

Fig.7 shows the speed torque performance of Induction motor by using three phase, 9 level inverter with APOD method. The signal is getting settle after 0.3 seconds at 1500 rpm.

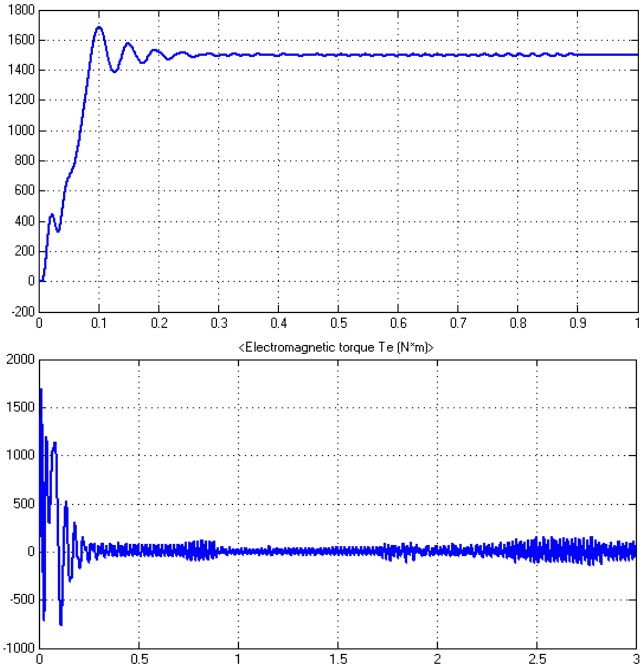

Fig. 7. Speed and Torque Output of Induction Motor

Fig. 8, 9 and 10 illustrates the output phase voltage waveform of five, seven and nine level three phase inverter.

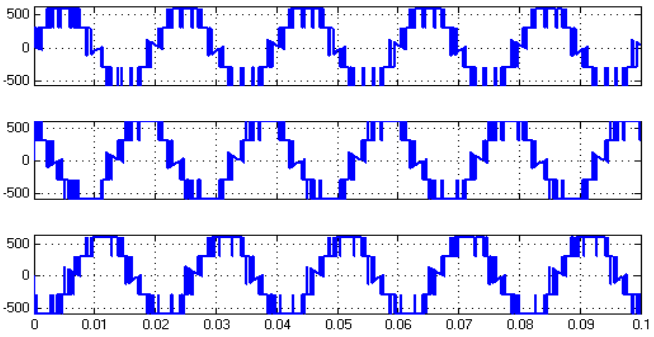

Fig. 8. O/P Voltage waveform of Three Phase 5 Level Inverter

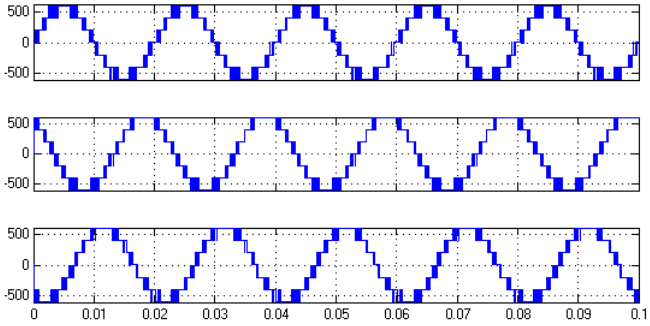

Fig. 9. O/p Voltage waveform of Three-Phase 7 Level Inverter

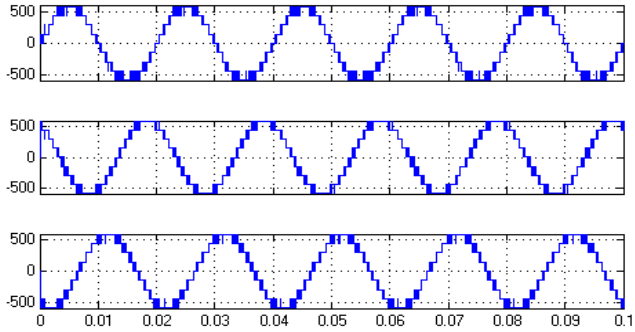

Fig. 10. O/P Voltage waveform of Three-Phase 9 Level Inverter

Fig. 11 illustrates the output voltage as well as current waveform with LC filter. The values of L is 1 H and C is 100nF.

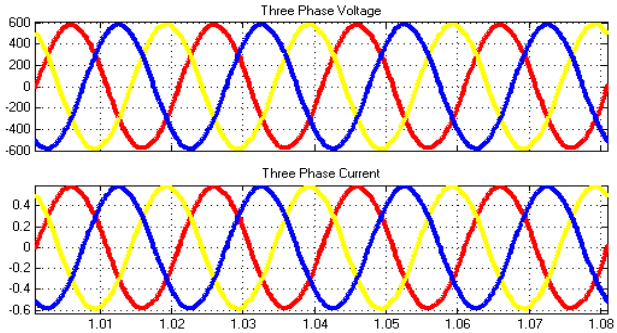

Fig. 11. Three-Phase O/P Voltage & Current of Inverter with Filter

Fig. 11 illustrates the output voltage as well as current waveform with LC filter. The values of L is 1 H and C is 100nF.

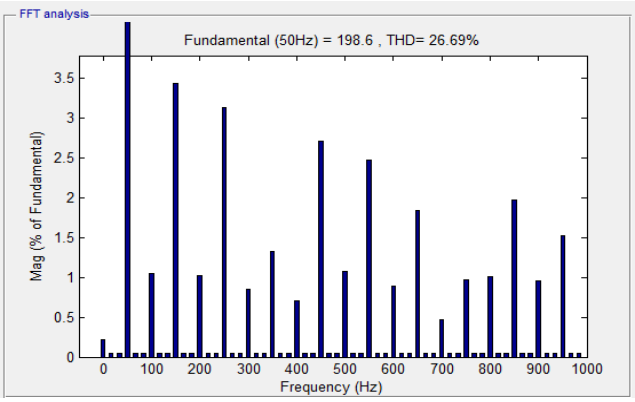

Fig.12 (a)

THD analysis of 5- level inverter is carried out by the PD method. The observed THD is 26.69% for three cycles of one phase.

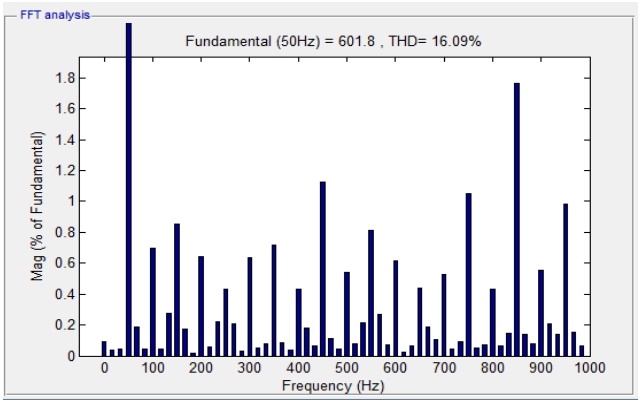

Fig.12 (b)

For 7- level inverter FFT analysis is carried out by PD method. The observed THD is 16.09% for three cycles of one phase.

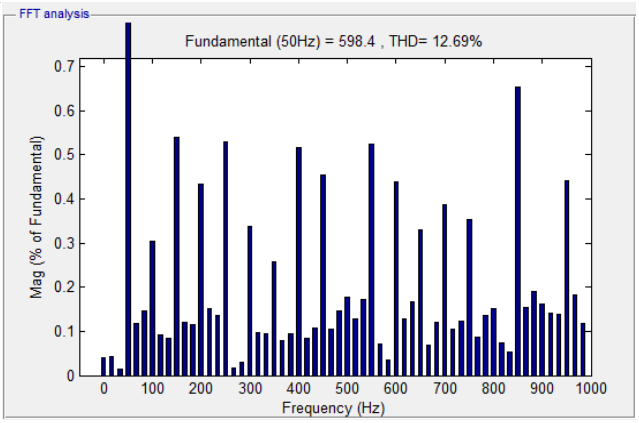

Fig.12 (c)

For 9- level inverter FFT analysis is carried out by PD method. The observed THD is 12.69% for three cycles of one phase.

Fig. 12 (a): THD analysis of 5 Level Inverter (b) THD analysis of 7 Level Inverter (c) THD analysis of 9 Level Inverter utilizing PD strategy.

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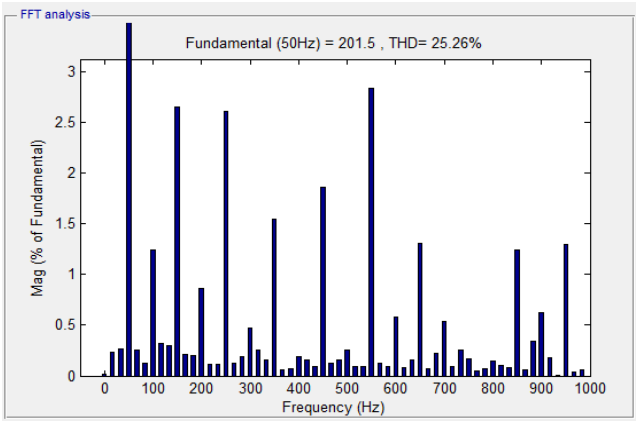

Fig.13 (a)

For 5- level inverter THD analysis is carried out by POD method. The observed THD is 25.26% for three cycles of one phase.

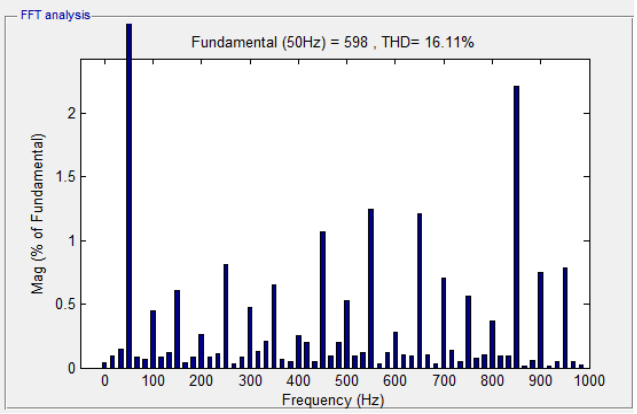

Fig.13 (b)

For 7- level inverter FFT analysis is carried out by POD method. The observed THD is 16.11% for three cycles of one phase.

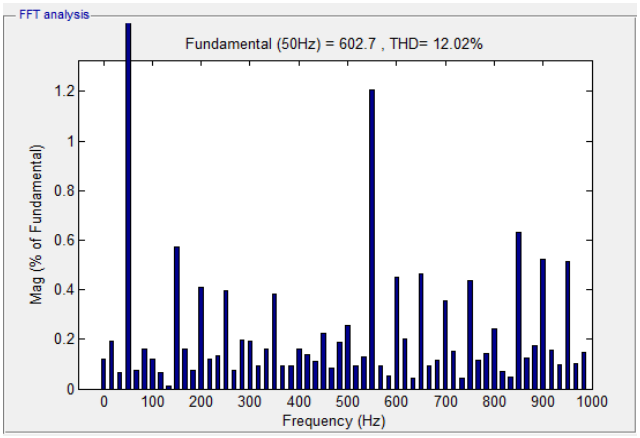

Fig.13 (c)

For 9- level inverter THD analysis is carried out by POD method. The observed THD is 12.02% for three cycles of one phase.

Fig. 13 (a): THD analysis of 5- Level Inverter (b) THD analysis of 7 Level Inverter (c) THD analysis of 9 Level Inverter with POD strategy.

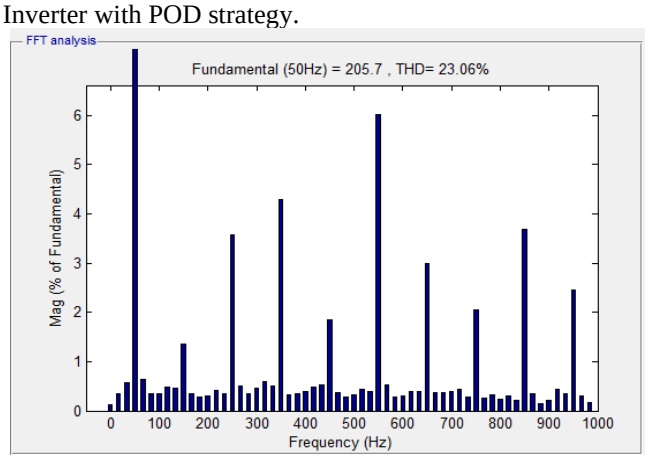

Fig.14 (a)

For 5- level inverter THD analysis is carried out by APOD technique. The observed THD is 23.06% for three cycles of one phase.

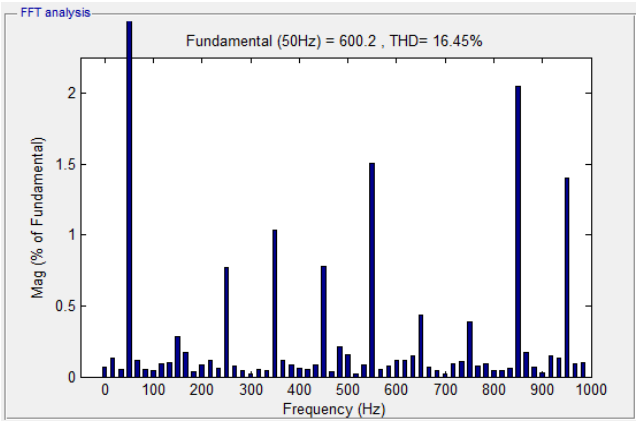

Fig.14 (b)

For 7- level inverter FFT analysis is carried out by APOD method. The observed THD is 16.45% for three cycles of one phase.

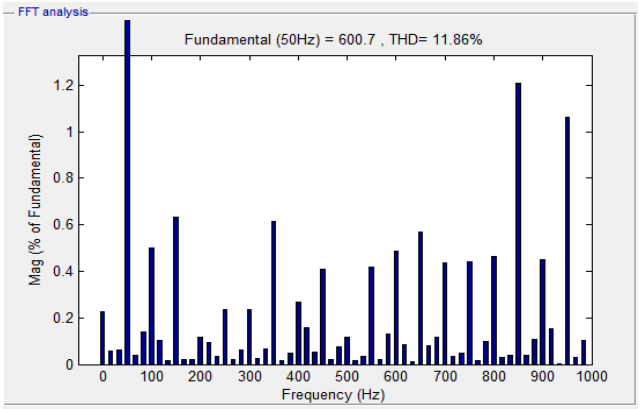

Fig14 (c)

FFT analysis for 9- level inverter is carried out by APOD method. The observed THD is 11.06% for three cycles of one phase.

Fig. 14 (a): THD analysis of 5 Level Inverter (b) THD analysis of 7 Level Inverter (c) THD analysis of 9 Level Inverter for APOD strategy.

Fig. 15, 16, 17 gives the FFT analysis of 5, 7 & 9 level inverter using filter for SPWM techniques.

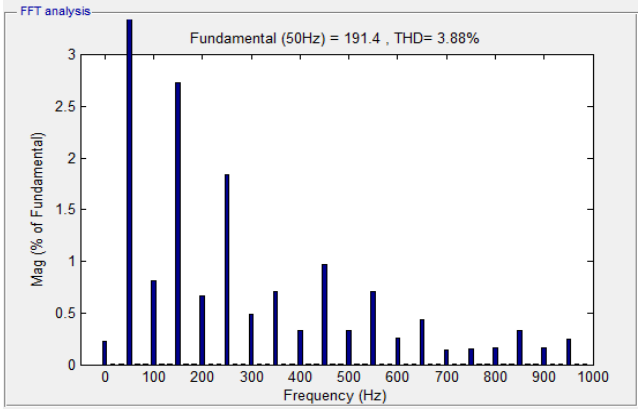

Fig.15 (a)

For 5- level inverter FFT analysis with filter is carried out by PD method. The observed THD is 3.88% for three cycles of one phase.

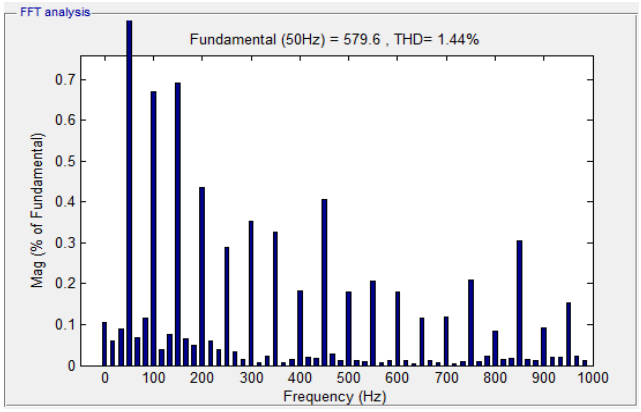

Fig.15 (b)

THD analysis of 7- level inverter with filter is carried out by PD method. The observed THD is 1.44% for three cycles of one phase.

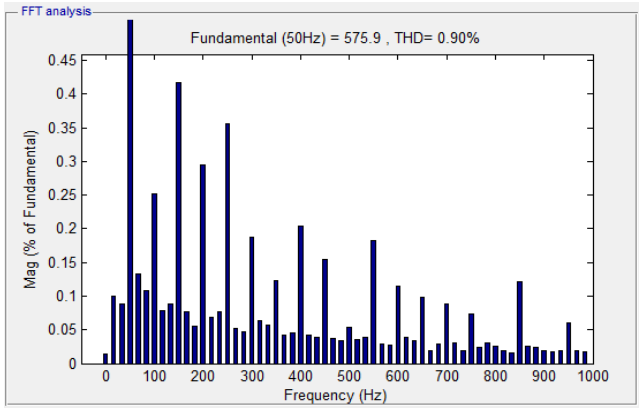

Fig.15 (c)

For 9- level inverter FFT analysis with filter is carried out by PD method. The observed THD is 0.90% for three cycles of one phase.

Fig. 15 (a): THD analysis of 5 Level Inverter (b) THD analysis of 7 Level Inverter (c) THD analysis of 9 Level Inverter for PD method with filter

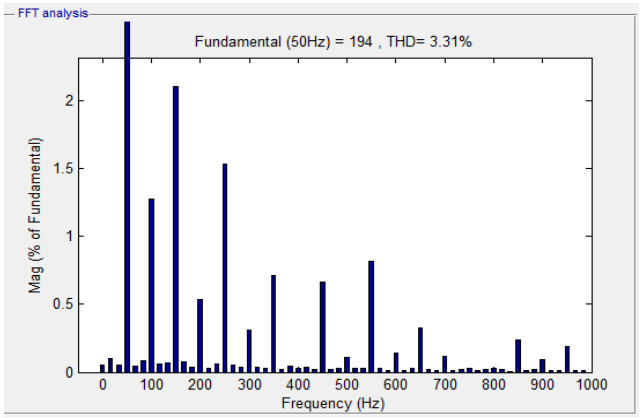

Fig.16 (a)

For 5- level inverter FFT analysis with filter is carried out by POD method. The observed THD is 3.31% for three cycles of one phase.

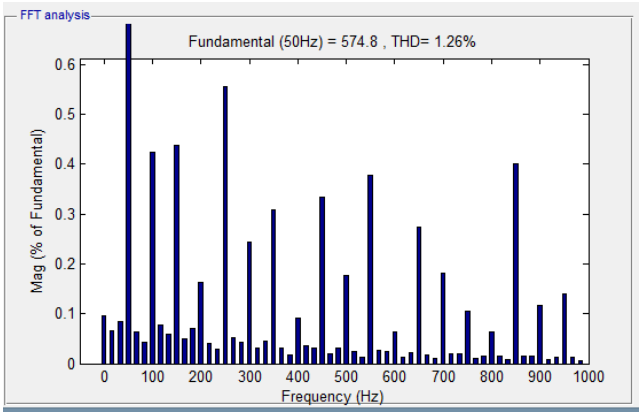

Fig.16 (b)

For 7- level inverter FFT analysis with filter is carried out by POD method. The observed THD is 1.26% for three cycles of one phase.

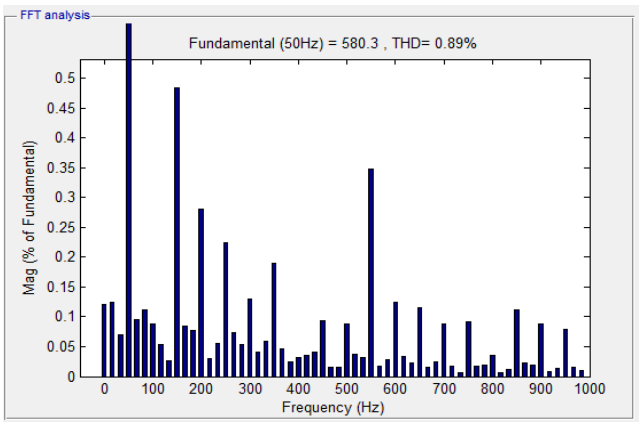

Fig.16 (c)

For 9- level inverter FFT analysis with filter is carried out by POD method. The observed THD is 0.89% for three cycles of one phase.

Fig. 16 (a): THD analysis of 5 Level Inverter (b) THD analysis of 7 Level Inverter (c) THD analysis of 9 Level Inverter for POD method with filter

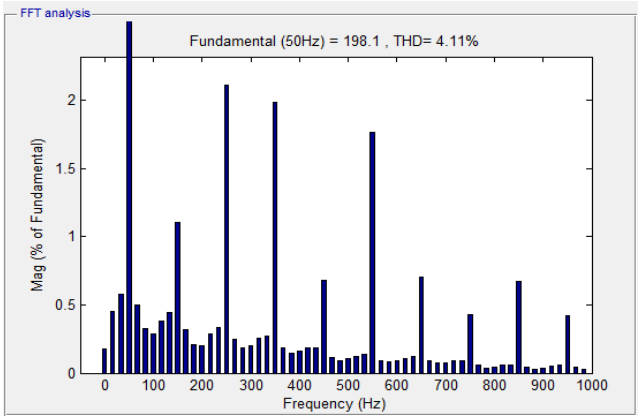

Fig.17 (a)

For 5 level inverter FFT analysis is carried out by filter for APOD method. The observed THD is 4.11% for three cycles of one phase.

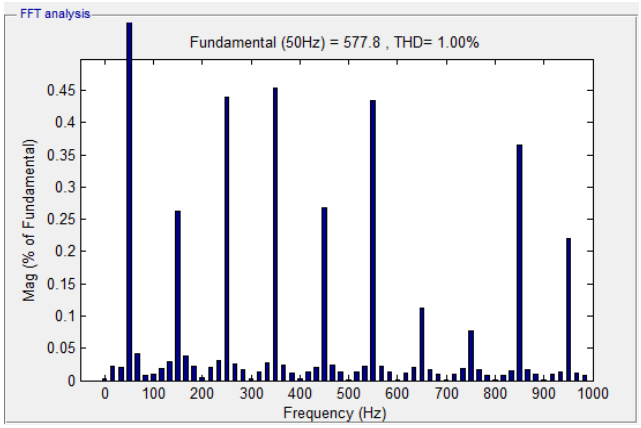

Fig.17 (a)

For 7- level inverter FFT analysis with filter is carried out by APOD method. The observed THD is 1.00% for three cycles of one phase.

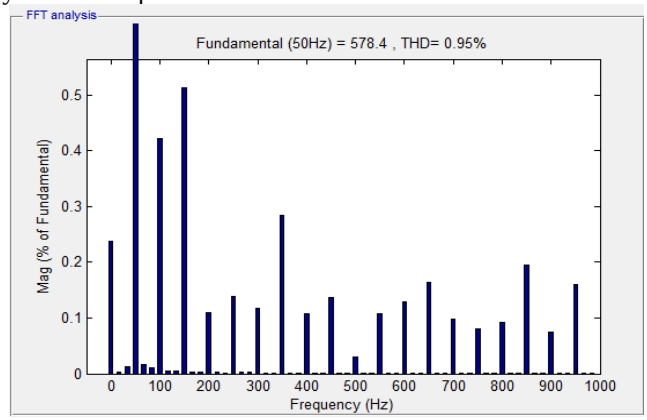

Fig. 17 (c)

For 9- level inverter, FFT analysis with filter is carried out by APOD method. The observed THD is 0.95% for three cycles of one phase.

Fig. 17 (a): THD analysis of 5 Level Inverter (b) THD analysis of 7 Level Inverter (c) THD analysis of 9- Level Inverter for APOD method with filter

Table II: THD analysis for inverter

Levels	Types	Phase R	Phase Y	Phase B
5	PD	26.69	26.70	27.56
	POD	25.26	25.40	22.74
	APOD	23.06	23.29	23.49
7	PD	16.09	14.74	15.16
	POD	16.20	14.98	15.45
	APOD	16.45	16.54	16.99
9	PD	12.69	12.48	12.74
	POD	12.02	12.22	12.31
	APOD	11.83	11.55	11.90

Table 3 gives the comparative analysis for 5, 7 and 9 level inverter without using a filter for three phases (*i.e.* R, Y & B) with by PD, POD, and APOD methods. From this table, it is observed that when no. of levels in the output is increased, the THD is getting lesser. By using the APOD method for 9 level, THD is less as compared to PD, POD methods.

Table 4 provides the comparative analysis of 5, 7 and 9 level inverter with filter for three phases (*i.e.* R, Y & B) with PD, POD, and APOD methods. From this table it is observed that by using filter the THD is improves further.

Table 4: THD analysis for inverter using filter

Levels	Types	Phase R	Phase Y	Phase B
5	PD	3.88	2.63	3.74
	POD	3.31	2.87	5.63
	APOD	4.11	5.07	4.93
7	PD	1.44	1.83	1.91
	POD	1.76	1.67	2.42
	APOD	1.00	0.70	0.85
9	PD	0.90	0.61	1.00
	POD	0.89	1.21	1.42
	APOD	0.94	0.97	0.56

VI. CONCLUSION

In this paper, a new topology of the three-phase multilevel inverter has been used for medium voltage &high power application railway system. The advantage of this method is less number of components as compared to the traditional multilevel inverter. In this paper, the comparative analysis has been carried out with various levels of inverter such as 5 level, 7 level & 9 level. It is observed that when the no. of levels in the output is increased, the THD is getting lesser. The various SPWM techniques are used to reduce the Total Harmonic Distortion (THD) of the respective level of inverters. The 9 level inverter with APOD method has shown better results for THD as compared to the PD and POD methods. The simulation results shows better stability and dynamic response for Asynchronous motor such as Induction motor.

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