A Unique Single Source Nine Level Inverter with Reduced Switching Devices for Single Phase AC Applications

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Abstract: In recent times there is a huge demand in reduced switched multilevel inverter. The multilevel inverter is one of the attractive features in harmonics elimination. This paper proposes single source nine level inverter with reduced switching devices for single phase AC applications. The conventional cascaded and other multilevel inverter comprises of more number of switches, passive components as well as sources. This makes the system larger in size, weight as well as less cost effective. The proposed multilevel inverter has the ability of producing nine levels with reduced number of switches and source. In addition to that the single source nine level inverter utilizes the simplified control algorithm which reduces the complexity. The Sinusoidal Pulse Width Modulation (SPWM) scheme is one of the most common control techniques which have the simple structure. The operation of the circuit and control algorithm is discussed in detail. The results are verified by the Matlab/Simulink which shows the value and righteousness of the system.

Keywords: Single Source, Reduced Switches, Nine Level, THD (Total Harmonic Distortion), Sinusoidal Pulse Width Modulation (SPWM).

I. INTRODUCTION

The multilevel inverters have been used for reaching the high level of power using the semiconductor switches [1]. The use of multilevel inverters divides the maximum value of power into different levels of power through various numbers of switches. The separation of levels reduces the voltage stress across each switch which improves the stability and power quality of the power system [2]. The main objective of the multilevel topology is to reduce the harmonics by increasing the levels of the AC power. The absence of multilevel inverter topology reduces the operation of filters for reducing the harmonics. The filters increase the system size and weight. The multilevel inverter topology has the serious drawback of increased semiconductor switch counts [3]. The increased switch count makes the system bulky and complex. Therefore there is a huge scope in designing the multilevel inverters with reduced switches. The researchers in [5][6] has proposed less number of switches based multilevel inverter but the source as well as passive components count has been increased. The increase of sources and passive components crafts the system less cost effective.

The proposed topology consists of less count of switches as well as single source than the conventional multilevel inverter such as cascaded H Bridge, flying capacitor and diode clamped [7]. The conventional converter becomes problematical while increasing the levels to a more number. The conventional method also faces the problem of unbalance of voltage because of increasing the levels. Therefore the proposed method is implemented with the advantages of less switch count, source, capacitor voltage stability and less complexity. The usage of multiple sources in one circuit not only less cost effective but also it has the drawback of deciding the same or different voltage values that to be used as sources. The usage of single source leads to boost the voltage for different levels. The voltage boost operation includes the usage of step up transformer by increasing the number of turns i.e., turns ratio [7]. The inclusion of transformer makes the circuit complex as well as bulky. Therefore there is in search of transformer less multilevel inverter circuit. Finally the researchers came into implementation of using capacitors for boosting up the voltage. The above solution makes the system less complex as well as size, cost, weight diminish. The total harmonic distortion isn't decreased due to multilevel inverter yet in addition it uses the assistance of control strategies which controls the inverter switches. There are various control techniques utilized for the control of multilevel inverters. One of the simplest control methods is Sinusoidal Pulse Width Modulation (SPWM). SPWM also has the greatest ability to reduce the harmonics values. There are different types of SPWM [8]. The desired SPWM has to be selected for the desired applications and output values.

This paper proposes the multilevel inverter which comprises of nine level, single source, less number of switches. The proposed nine level inverter also utilizes the SPWM technique for the alleviation of harmonic problem to a greater extent. The unique nine level inverter is fed by the single source fed to RL load application is controlled by the SPWM is shown in figure 1. The circuit operations and control strategy are clearly observed from the previous reference works and the proposed work explained in detail with experimental results.

Fig. 1 Proposed Structure
II. PROPOSED TOPOLOGY

Circuit operation:
The proposed unique single source nine level inverter’s circuit diagram is shown in figure 2. The circuit diagram consists of dual sets of switches. The 1<sup>st</sup> set of switch plays the role of improving the switching level and voltage to a desired value. The 2<sup>nd</sup> set of switch plays the role of converting the DC to AC power to the load by changing the positive and negative polarity. The 1<sup>st</sup> set of switch additionally contains the utilization of capacitors and diodes for the voltage boost and levels achievement. The proposed inverter switching pattern is shown in table 1. The capacitors and diodes operation is decided by the 1<sup>st</sup> set of switch. The 2<sup>nd</sup> set of switch only decides the polarity of the voltage and current flow to the load. For 0 voltage level capacitors attain the voltage stability because of that the capacitor C1 and C2 neither charges or discharges. In addition to that both the diodes D1 and D2 also get off during the period of 0V level. For V/2 levels both the Capacitors C1 and C2 discharges, D2 is On. For V level both the capacitor charges and D1 conducts. For 3V/2 level both the capacitors discharges and D2 conducts. For 2V level both the capacitors and diodes are off. The capacitors and diodes operation is decided by the 1<sup>st</sup> set of switch. The negative polarity levels also has the same capacitors and diodes operations. Table 1 represents the switches operation of proposed 9 level inverter.

![Proposed circuit diagram](image1)

![Waveform of IPD](image2)

![Table 1 Switches operation](image3)

![Waveform of POD](image4)

Control strategy:
The multilevel inverters can be controlled by the different control strategies such as SPWM, Space Vector Pulse Width modulation(SVPWM), Selective Harmonic Elimination (SHE). The SPWM is one of the uncomplicated methods. The SPWM also has the benefit of lessening the THD to a more prominent degree. The SPWM operation comprises of comparing the sinusoidal waveform which is known as modulating wave with the triangular waveform which is known as carrier wave[9]. The comparison results decides the desired gate pulses for the inverter switches. There are different types of SPWM techniques. The most commonly used techniques are In phase disposition SPWM (IPD) 2) Phase opposition disposition SPWM (POD) 3) Alternate phase opposition disposition SPWM (APOD).

In IPD all the carrier waves has the same frequency and same phase shift. In POD the carrier wave are divided into two types[10]. One is above zero base level and other is below zero base level. The both types have the same frequency but they are different in phase of 180 degree. In APOD all the carrier waveforms has same frequency but each adjacent carrier wave are phase shifted. The IPD, POD, APOD waveforms with carrier and modulated waveform[11] is shown in figure 3, 4 and 5. The number of carrier waves will be based upon the subtraction of number of voltage levels by 1 ie., in propose paper levels to be attained is nine, then number of carriers is 9-1=8. This paper focuses on POD based SPWM because it diminishes the harmonics at a lower modulation values. The states of operating switches is shown in figure 6.
III. RESULTS

Fig. 5 Waveform of APOD

Fig. 6 States of switches for proposed inverter

Fig. 7 Output 9 level voltage waveform

Fig. 8 Output 9 level current waveform

Fig. 9 Overall Matlab/simulink diagram

Fig. 10 POD based SPWM

Fig. 11 Simulation waveform of gate pulses
The proposed nine level inverter features are verified by using Matlab/Simulink. The output voltage and current waveform of proposed inverter are shown in figure 7 and 8. Figure 9 represents the overall simulation diagram. The POD based SPWM is shown in figure 10. Figure 11 shows the gate pulses simulation waveform. The POD based SPWM simulation waveform is shown in figure 12. Figure 13 shows the THD of output current.

IV. CONCLUSION

The nine level inverter with single source is proposed and it is controlled by the SPWM. The proposed multilevel inverter has the advantages of less semiconductor switches, single source and harmonics decrease to a more prominent esteem. The POD based SPWM is utilized for the generation of gate pulses for the proposed inverter switches. The above utilized has the ability to reduce the harmonics with lower modulation values. The THD value of proposed paper is reduced as 0.98%. The simulation results show the effectiveness and better qualities of the system.

REFERENCES


AUTHORS PROFILE

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