International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-9 Issue-2, December, 2019

Systolic Fir Filter using Bypass Multiplier

E. Swarnalatha, Ch. Hariveena, Saritha Vuppala

Abstract*: In DSP the most common function is Finite Impulse Response (FIR) filter which is realized in field Programmable gate Arrays (FPGAs). For efficient Very Large Scale Integration (VLSI) computation systolic FIR filter architecture has attractive models. High speed is the major concern for fast computation in real time Digital Signal Processing (DSP) applications. In conventional systolic FIR filter method uses general array multiplier structure which takes more time to compute the process with high design complexity with less power. To overcome this problem the systolic FIR filter utilizing Bypass Feed Direct Multiplier(BFDM) is proposed. The proposed method 16 tap systolic FIR parallel processing offers less delay with less design complexity which is used in image and signal processing applications. The proposed method is simulated using Xilinx ISE 12.4 ISE tool and the functions are evaluated by MODELSIM 6.3C.

***Keywords* : systolic FIR filter, bypass feed direct multiplier, Xilinx ISE tool .**

I. INTRODUCTION

Due to the linear phase and stability properties the FIR filter is broadly used in the application of DSP. The overall performance of the processor is depends on the execution speed of the addition and multiplication. Basic building blocks of reconfigurable devices is described in [1].Systolic FIR filter utilizing array multiplier is described in [2].compared the performance in terms of the delay and power with existing method. A study about the digital filter structures namely systolic, direct and transposed array form is described in [3]. To determine discrete Fourier transform a Goertzel algorithm is realized in FPGA altera device.12 tap further desensitized FIR half band filter using modified Russian peasant multiplier is described in [4].It reduces the area due to square root carry select adder in the multiplier part. A spiral based structure for interconnections are used to design the systolic array architecture is described in [5]. Here the K is the filter order and the architecture is consists of L X K cells and this increase the throughput. Realization of systolic FIR architecture using parallel prefix adder is described in [6]. For 8 ,16,32 and 64 bits the adder type was implemented. Systolic structure using DA based one and two dimensional pipeline methods is described in [7] which is realized in XCV2000E FPGA utilizing a hybrid grouping of parameterizable VHDL and Handel-C cores. Low latency and high throughput systolic FIR filter is described in [8].At first for bit parallel LSB, skewed form input and output is used. MAC unit for efficient filter design is described in [9].This method reduces the carry propagation for serial adder using shifter and 2:1 multiplexer block. systolic array with Linear architecture FIR Residue Number System(RNS) is described in [10].pipelined architecture which is consists of modular cells. Uses bit serial systolic arrays and residue serial systolic arrays are designed. A hybrid RNS binary arithmetic for FIR filter is described in [11]. For each modulo it represents conventional binary arithmetic and RNS numbering. To reduce the switching activities high speed bypass multiplier is described in [12].to enhance the fast carry generation carry look ahead function is employed in the addition part. Digit serial FIR for both symmetrical and anti symmetrical cases is described in [14].By switching to FIR filtering is realized using the online processing is described in[15]. By utilizing BFDM the systolic FIR filter designed with less delay is presented. The manuscript is structured as follows. In section II describes the proposed systolic FIR design and in section III describes the result and discussion of the proposed method. Finally in section IV describes conclusion of the work.

II. PROPOSED SYSTEM

The FIR filter can be realized in different ways like transposed, direct and systolic form. The structure for systolic architecture is made up of matrix row like processing units referred as cells. The structure of systolic is shown in the figure 1.

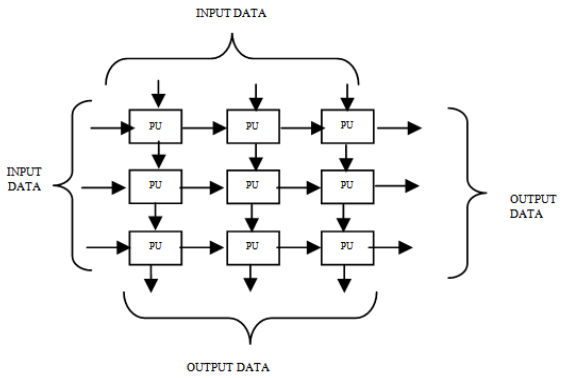

Fig. 1.Strucutre of Systolic.

Revised Manuscript Received on December 30, 2019.
* Correspondence Author
E. Swarnalatha*, Assistant Professor, Dept of ECE , Guru Nanak Institute Of Technology, Khanapur, Telangana, India. Email: swarnalatha.erram@gmail.com
Ch. Hariveena, Assistant Professor, Dept of ECE, CMR Engineering College, Kandlakoya, Medchal, Telangana, India. Email: cherukuhariveena@gmail.com
Saritha Vuppala, Assistant Professor, Dept of ECE Teegala Krishna Reddy Engineering College, Meerpet Medbowli, Hyderabad, Telangana, India. Email: Vuppala.saritha@gmail.com.

Each rows and columns has processing unit (PU) in matrix form. Each PU is depends on one another.

For the given data the output is obtained in row and column wise. The systolic FIR in single PU is the specialized form of parallel computing. In the proposed method the 16-tap systolic structure is shown in the figure 2.

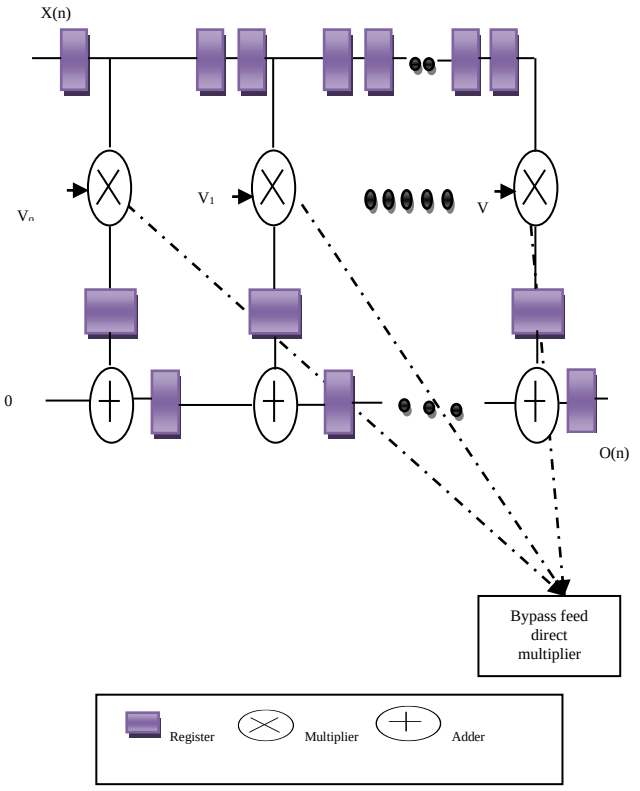

Fig. 2.16-tap systolic FIR fitler.

The systolic FIR filter transfers the data is a pipeline structure which is made up of an array of processing elements. The X(n) is the input V0,V1,…V15 are the coefficients and registers values get multiplied and added at the input and output. Where the x get multiplied and accumulated and results are flow from left to right with high speed due to pipelining. The data flows synchronously across the array elements. The general equation for the FIR filter is formulated as.

$$O(n) = V^T(n).\, x(n)$$

$$= \sum_{k=0}^{L-1} v(k)x(n-k)$$

Any Here the O(n) is the output. In systolic FIR structure the multiplier input originates from the various nodes i.e. from two dynamic inputs, one coefficients input and dynamic input, one pre adder input and one coefficient input, finally from one pre adder output and one dynamic input. Figure 3 shows the BFDM. Here in the multiplier part BFDM is used. In add and shift multiplier method, zero is added to the partial product as U=0 and input Q is added when U=1, this causes unwanted power dissipation. To overcome this problem when U=0 bypass is appears and the partial product get right shifted by position one, this avoids the unwanted adder part.

The bypass and feeder register is used when U=0 for bypass the adder. In every cycle the current bit of next cycle is checked, if it is 0 adders is bypass to the next cycle which is used to store the present partial product. Adder is required when U (n+1) =1 and the clocked feed register is used to store the partial product which is feed to added on the next cycle. In this multiplier, there is no need of shifting LSB only shifting MSB which saves power. Here the LSB is stored in the p latch and the counter is used to open the latch.

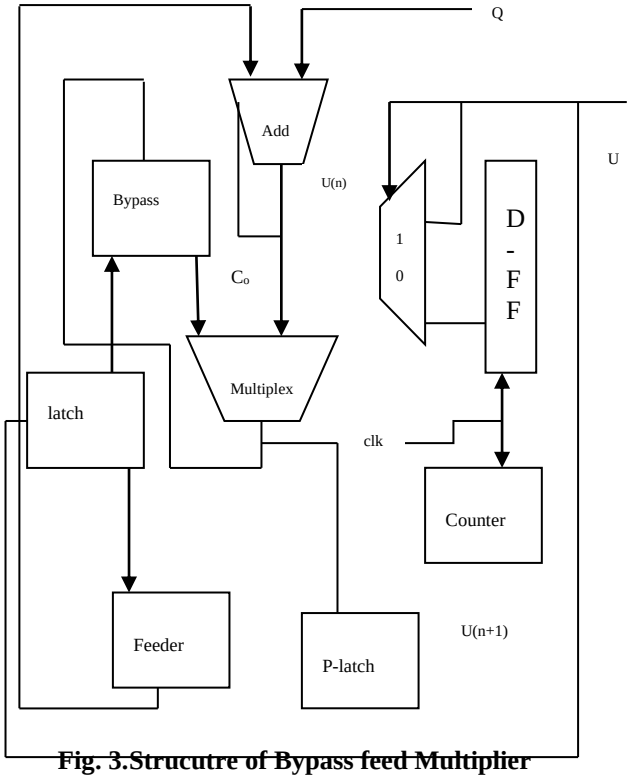

Fig. 3.Strucutre of Bypass feed Multiplier

The activity of functional blocks namely adder, multiplexer selection node, counter, shifting of register, shifting of Partial product registers (latches) is minimized in the bypass feed direct multiplier.

III. RESULT AND DISCUSSION

The proposed method 16- tap systolic FIR parallel processing using bypass feed direct multiplier is implemented using Xilinx 12.4 ISE (Family- Spartan 3, Package-X3CSpq208, Speed:-5 and Devices-XC4VLX15/XCVLX25) design tool to check the functionality. The FIR filter is designed and simulated in MODELSIM6.3c. Figure 4 illustrates the simulation waveform of the proposed systolic FIR filter.

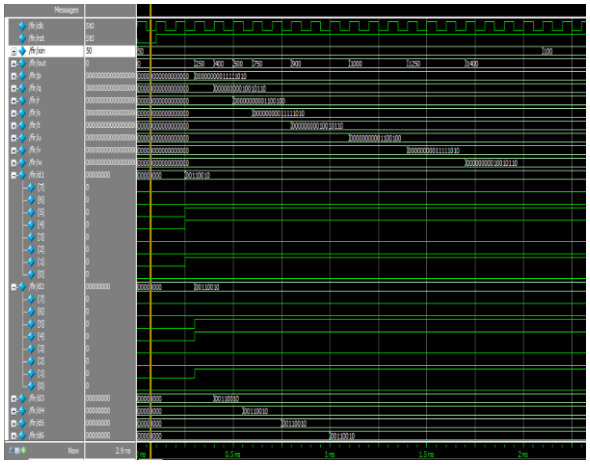

Fig. 4.Simulation waveform of proposed 16-tap systolic FIR filter.

In waveform x_{in} is the input out is the output which is the 8 bit binary data information. The input for multiplier is Q and U is 8 bit and the output of multiplier is 16 bit. After synthesizing the code in Xilinx tool in design summary the delay taken by the proposed method is mentioned in the timing summary. Table 1 shows the comparison table of the conventional and proposed systolic FIR filter.

Table- I: Comparison of conventional and proposed 16-tap systolic FIR filter

Methods	Delay(ns)
Conventional method [8]	15.946
Proposed method	12.391

From the table 1 the delay occupied by the conventional method is 15.946 ns and for proposed method 12.391 ns is obtained. When compare to the conventional method the proposed method provides 22.29% reduction in delay with high speed.

IV. CONCLUSION

In this paper the 16-tap systolic FIR filter utilizing bypass feed direct multiplier is presented using Xilinx ISE 12.4 tool. The designed systolic FIR filter is employed in the image and signal processing applications. Compare to the conventional method the proposed method provides 22.29% reduction in delay with high speed. The systolic FIR filter structure utilizing BFDM shows the efficient result with less design complexity. The switching activity of the functional blocks is decreased in multiplier module. In future, this structure can be realized for VLSI signal processing for noise cancellation with the help of adaptive filter structures.

REFERENCES

1. A. Gougam, and D. Benazzouz, "Synthetic Systolic FIR filter based FPGA," in Systolic FIR filter based FPGA, 2010.
2. S.Kalpana, and P. Samundiswary, "Design of Systolic FIR Filter Using VHDL". International Journal of Engineering Trends and Technology Vol.10,No.5, Apr 2014 ,pp-255-259.
3. R. Seshadri, S. Ramakrishnan, and J. S. Kumar, "Knowledge-based single-tone digital filter implementation for DSP systems". Personal and Ubiquitous Computing, September 2019, pp.1-10.
4. C. U. Kumar, and S. Kamalraj, " Ambient intelligence architecture of MRPM context based 12-tap further desensitized half band FIR filter for EEG signal". Journal of Ambient Intelligence and Humanized Computing, Feb 2019, pp.1-8.
5. R. Wyrzykowski, and S. Ovramenko," Flexible systolic architecture for VLSI FIR filters". IEEE Proceedings (Computers and Digital Techniques), Vol.139, No.2, Mar.1992. pp.170-172.
6. R. Uma, and J. Ponnian, "Systolic FIR filter design with various parallel prefix adders in FPGA: Performance analysis". International Symposium on Electronic System Design, December, 2012, pp. 111-115.
7. P. K. Meher, S. Chandrasekaran, and A. Amira, "FPGA realization of FIR filters by efficient and flexible systolization using distributed arithmetic". IEEE transactions on signal processing, Vol. 56, No.7, 2008, pp.3009-3017.
8. C. G. Caraiscos, and K. Z. Pekmestzi," Low-latency bit-parallel systolic VLSI implementation of FIR digital filters". IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 43, No.7, Jul.1996, pp.529-534.
9. R. Madasamy, and H. Shekhar, "Serial adder based multiplication and accumulation unit (mac)". International Journal Of Advances In Signal And Image Sciences, Vol. 3, No.1, 2017, pp.25-30.
10. M. Taheri, G. Jullien, and W. Miller, "Systolic ROM arrays for implementing RNS FIR filters". IEEE International Conference on Acoustics, Speech, and Signal Processing, Vol. 12, April. 1987. pp. 771-774.
11. M. K. Ibrahim, "Novel digital filter implementations using hybrid RNS-binary arithmetic". Signal processing, Vol.40, No.2-3, November1994. pp.287-294.
12. S. Krishnamurthy, R. Kannan, E. A. Yahya, and K. Bingi." Design of FIR filter using novel pipelined bypass multiplier". IEEE 3rd International Symposium in Robotics and Manufacturing Automation, September 2017, pp. 1-6.
13. R. M. Deshmukh, and R. Keote, "Design of polyphase FIR filter using bypass feed direct multiplier". International Conference on Communications and Signal Processing, April 2015, pp. 1640-1643.
14. J. Valls, M. M. Peiró, T. Sansaloni, and E. Boemo, "A study about FPGA-based digital filters". Workshop on Signal Processing Systems, October 1998, pp. 192-201.
15. U. Ghani, M. Wasim, U. S. Khan, M. Mubasher Saleem, A. Hassan,N. Rashid, M. Islam Tiwana, A. Hamza, and A. Kashif, "Efficient FIR Filter Implementations for Multichannel BCIs Using Xilinx System Generator". BioMed research international, 2018.

AUTHORS PROFILE

E. Swarnalatha, Completed Bachelor Of Engineering On Electronics And Communication Engineering In Princeton College Of Engineering And Technology And Completed The Master Degree On Embedded Systems In Princeton College Of Engineering And Technology, Hyderabad. Totally She Had Teaching Experience As 6.5 Years. Currently Working As Assistant Professor In Guru Nanak Institute Of Technology Khanapur, Telangana, India. Published Papers In Two International Journals.

Ch. Hariveena, Completed B.Tech (ECE) Vijaya Institute Of Technology For Women, Vijayawada And Completed Master Of Engineering On Embedded Systems In Sathyabama University, Chennai. She Had 4 Years Of Experience In The Teaching Field. Currently Working As An Assistant Professor (Dept. Of E.C.E) At CMR Engineering College, Kandlakoya, Medchal, Telangana Published One Paper In International Journal And Wrote An Article On Fingerprint Compression Based On Hough Transform (Under Processing) In Electronic Engineering Times.

V.saritha, Competed B.Tech In Princeton College Of Engineering And Technology And Completed M.Tech In Princeton College Of Engineering And Technology Hyderabad. She Had 5.5 Years Of Experience In Teaching Field. Currently Working As Assistant Professor In The Teegala Krishna Reddy Engineering College.Published One Paper In International Journal.