A Suggestive Low Power TIQ Comparator Architecture using Adiabatic Logic for Implementation of 3-bit Flash type ADC.

Vishal Moyal

Abstract: Power consumption is prime concern for the designers in modern day scenario. For the devices that are power-driven by tiny rechargeable or non-rechargeable batteries over the entire life period, such as medical transplant devices or portable medical instruments, necessitates lowest possible power consumption. In these devices Analog-to-Digital Converter (ADC) isdynamic component to provide connectionamongst Analog and Digital system. The paper is aimed to report the design contests and tactics for low power ADCs which are used in biomedical graft devices and instruments. A comparator module of ADCs used in designing of such devices requires more power than other blocks in the device, a low power comparator is suggested for Threshold-Inverter- Quantizer (TIQ) using Diode-Free-Adiabatic-Logic (DFAL) to implement Flash type ADCs. The projected 3-bit Flash ADC is simulated using Cadence® Virtuoso IC616 with TSMC 65nm technology. The ADC was simulated at peak voltage of 1.2V and capacitive load of 1pF, results in consumption of 5.53 μW of average power, which is 66.03% lesser relative to conservative CMOS-TIQ based comparator. Observed static parameters are: DNL is equal to -0.62/ +0.57 LSB and INL is equal to -0.44/ +0.41 LSB. Dynamic parameters observed results are as: THD = -25.25dB, SNR = 19.45 dB, SNDR = 18.39 dB, ENOB = 2.76 bits, SFDR = 23.4 dB.

Keywords: CMOS, PMOS, NMOS, ADC, TIQ, DFAL, VTC, MUX, LSB, DNL, INL, SFDR, SNR, ENOB.

I. INTRODUCTION

Analog-to-Digital Converter is vital structural parameter in most of the modern-day devices. In the recent past, most of the portable and implantable devices are constructed with very strict necessities for reduction in power consumption. In the electronic systems, used to design devices which will be implanted in the human body; for which consumption of power is becoming one of the most thoughtful aspect. This saving in the consumption of power upsurges the necessity for the development of system built using constructional blocks which operates on low voltage and consumes lowest possible.

Analog to Digital Converters (ADCs) render an analog parameter into its equivalent digital signal, commonly cast off in handing out the information, data computing and transmission system. ADC is the crucial components for the various devices, to maintain the power dissipation at lowest possible value. Medical electronics devices like Pacemakers and Electro-Cardio-Gram machines are distinctive examples of devices which requires very less consumption of power. Analog-to-digital converters are decisive portion of these devices because of its property of consumption of power. Therefore, reducing the power dissipation of the ADCs is utmost vital concern. Low power ADC with low sampling frequency and modest resolution is suitable for such application. These specifications make Flash ADC the suitable choice for those devices Flash ADC is cast-off for the high-speed, low resolution applications.[1]-[5]

In the suggested work, it is considered to design a Threshold-Inverter-Quantizer based on logic of energy recovery known as Diode-Free-Adiabatic-Logic (DFAL-TIQ-Comparator) for implementing Analog-to-Digital Converter which consumes less power. TSMC 65nm technology is used on Cadence® Virtuoso IC616 for parameter extraction.

II. DFAL: DIODE-FREE-ADIABATIC-LOGIC

In past decade, adiabatic-logic played a significant role in the designing of power efficient portable devices, because they outperform conventional CMOS counterparts as far as the consumption of power is concern. Conventional CMOS circuit’s power consumption is given by following mathematical relation,

\[ P_{\text{bias}} = C_{\text{Load}} \times V_{dd}^2 \]

The investigators focused their attention to reduce power supply and capacitive load \((C_{\text{Load}})\), to decrease dissipation of power, but those efforts were not enough to design modern-days power hungry device. The projecting feature of DFAL circuit is that, it doesn’t contain any diode; there is a rare chance of presence of a diode in its path for charging or discharging cycle.[6]-[7]

DFAL inverter depicted in Fig. 1, incorporates split-level sinusoidal clock \(V_P\) and \(V_{PC}\) as power supply, and is kept 180° out of phase. Voltage level of \(V_{PC}\) surpasses \(V_{PC}\) by amount \(V_P/2\), which will expressively reduce voltage variance amongst probes, subsequently power consumption will be condensed. This split nature of clock signal very slowly charges or discharges load capacitance \((C_{\text{Load}})\), in comparisons with adiabatic power clocks, the effectiveness of adiabatic logic circuit is concentrated on how leisurely charging or discharging of load capacitance \((C_{\text{Load}})\) is taking place? The power clock relationship is mathematically articulated as in (2) and (3).[8]
\[ V_p = \frac{V_{ad}}{4} \sin(\omega t + \theta) + \frac{3}{4} V_{dd} \]  
\[ V_{pc} = \frac{V_{ad}}{4} \sin(\omega t + \theta) + \frac{1}{4} V_{dd} \]

The circuit arrangement of DFAL inverter is analogous to the CMOS-Inverter with the advantage of adiabatic operation. The transistor M3 is used as pull-down network next to transistor M2, which is considered as the discharge path for \( C_{load} \). Power-clock (\( V_p \)) , pedals ON-state and OFF-state of \( M_3 \) transistor.

Prime source of power consumption in the adiabatic logic circuit is the discharger route diodes of MOS because the threshold voltage (\( V_{th} \)) drop is recognized as non-adiabatic loss; in case of DFAL inverter ON resistance is the source for the power consumption, known as adiabatic-loss of transistor \( M_3 \). The power consumed by this is lower than that of the power consumed by \( V_{ad} \) drop in diodes.

![Fig. 1. Circuit Schematic for DFAL Inverter](image1)

In accumulation to that, \( M_3 \) is also accustomed to recover the charge from output terminal; hereafter losses in diabatic circuit can be recovered. Still, it is not possible to improve and recover the losses entirely. Consumption of power can’t be entirely reserved, due to nonreversible features of DFAL-Inverter, with transistor \( M_3 \), the power consumption is immensely condensed as compared to the CMOS or any other diode based adiabatic inverter. [8]

The energy consumed by the DFAL inverter is given as

\[ E_{DFAL} = E_{CHARGE} + E_{DISCHARGE} = 0.5C_{I}V_{dd}^2 + 0.5C_{I}(V_{PP}-V_{nn})V_{nn}(4) \]

![Fig. 2. Architecture for traditional Flash type ADC](image2)

### III. CONVENTIONAL FLASH ADC ARCHITECTURE

The schematic representation for traditional Flash type ADC is published in Fig. 2. N-Bit Flash type Analog-to-Digital converter (ADC) circuit, required number of comparators are calculated by \( 2^N - 1 \), here total 7 comparators are essential for the portrayal of 3-bit Flash type ADC. Resistive divider network is castoff to generate different reference voltages, then comparison of these generated reference voltages and analog input signal is carried out in single clock. Reference voltage generated by respective comparator is 1 Least Significant Bit (LSB) over that of comparator reference voltage immediately underneath. Every single comparator generates output as logic 1, when the generated reference voltage is less than analog input applied for measurement, else, the comparator output will be logic 0. This comparison takes place in a single clock cycle only.

Decoder module is implemented for converting Thermometer-Code, produced by comparator into its equivalent binary-code that come close to input signal, by detecting pair of 1-0 and 0-1. [9]

### IV. MODIFIED FLASH ADC DESIGN

In current work comparator section of Flash ADC comprises of DFAL-TIQ which consumes a smaller amount power over traditional CMOS-TIQ comparator section. Output generated by the comparator section is in thermometric code form; hence it should be converted in to its equivalent binary format, for this a transformation Decoder section, capable of converting Thermometric code to desired Binary code is implemented. [9]-[14]

A. DFAL-TIQ comparator

Comparator is utmost critical module in Flash type ADC. It plays a vital role for converting analog voltage at input node, into logic 0 or 1, by equating it, with generated reference voltage. Numerous methods like differential amplifier latch comparator, Quantum Voltage (QV) comparator, autozeroed comparator,
sequentially sampled comparator, dynamic comparator and Threshold Inverter Quantizer (TIQ) comparator are suggested for the implementation of the comparator section; out of which TIQ comparator is the most suitable for the low power flash ADC implementation [13]-[17].

DFAL-TIQ comparators in the suggested work are judiciously selected to attain 0.065 Vstep size, which is premediated from analog input voltage full-scale range. Premeditated step size is denoted as 1 LSB in further consideration and mathematically represented as follows [5].

\[
V_{th} = \frac{|V_{tp}| + V_{tp} \sqrt{(Kn/Kp)}}{1 + V_{tp} / Kn/Kp}
\]

(5)

Here \(V_{tp}\) signifies threshold voltage of \(N_{MOS}\) transistor and \(V_{tn}\) signifies threshold voltage of \(P_{MOS}\) transistor which are used for LSB calculation where \(\mu_n\) gives the mobility of \(N_{MOS}\) and \(\mu_p\) represents the mobility of \(P_{MOS}\) and transistors respectively.

The DFAL-TIQ comparator section with sized (Quantized) \(P_{MOS}\) and \(N_{MOS}\) transistors is depicted in Fig. 3. is applied with analog input signal; trailed by identical gain booster stage to deliver the full voltage swing and improve the linearity of the system [12]. Using the mathematical relation given in (5) and step size of the full swing voltage (LSB), reference voltage for each and every stage of comparator are determined by calculating width \(W\) of \(P_{MOS}\) and \(N_{MOS}\) transistors of TIQ comparator, which is represented in Table-I.

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Reference Voltage</th>
<th>(W_p^\ast) (µm)</th>
<th>(W_n^\ast) (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.416</td>
<td>0.150</td>
<td>25.600</td>
</tr>
<tr>
<td>2</td>
<td>0.467</td>
<td>0.150</td>
<td>2.190</td>
</tr>
<tr>
<td>3</td>
<td>0.518</td>
<td>0.150</td>
<td>0.569</td>
</tr>
<tr>
<td>4</td>
<td>0.569</td>
<td>0.107</td>
<td>0.150</td>
</tr>
<tr>
<td>5</td>
<td>0.620</td>
<td>0.291</td>
<td>0.150</td>
</tr>
<tr>
<td>6</td>
<td>0.671</td>
<td>0.846</td>
<td>0.150</td>
</tr>
<tr>
<td>7</td>
<td>0.722</td>
<td>3.230</td>
<td>0.150</td>
</tr>
</tbody>
</table>

\(\ast\) Length of \(P_{MOS}\) and \(N_{MOS}\) is kept identical and minimum at 65nm

For attaining the different quantizer levels in \(P_{MOS}\) side \((W/L)_{n}\) is held in reserve at least value, at the same time, the channel widths of the \(P_{MOS}\) transistors are speckled to curtail the flow of current during metastable region i.e. Voltage Transfer Curve (VTC). For \(N_{MOS}\) channel width calculation described process is repeated in the other way.

Parametric DC sweep analysis is carried over a full-scale range input voltage of 0 to 1.2 V and attained variation of reference voltage as a function of variation in aspect ratio of transistors, as depicted in Fig.4.

B. Multiplexer based Code Converter (Decoder)

Output of this comparator section is available in the thermometric code format as presented in Table-II. Here thermometric code is represented by bits Y6 – Y0 and Binary Code is by B2 – B0.

<table>
<thead>
<tr>
<th>Table-II: Truth Table of code converter stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermometric Code</td>
</tr>
<tr>
<td>Y6</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>1</td>
</tr>
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</table>

From the values of above table, is clear that B2=Y3. When Y3=0 at the moment B1=Y1 and When Y3=1 the value of B1=Y5; by witnessing such relations; which are comparable to the basic equation of 2:1 multiplexer (MUX) the code converter stage (Decoder) is implemented and depicted in Fig. 5. [14-16].
C. DFAL-TIQ Flash Architecture

Complete schematic diagram for anticipated Flash ADC is conveyed in Fig. 6, which is a two-stage architecture. First stage contains of DFAL-TIQ comparator along with gain booster stage. In the second stage, the code converter is implemented in cascade with the comparator stage to furnish a whole ADC.

Fig 7 shows the layout extracted using cadence tools; the DRC and LVS done using Mentor Graphics Calibre interactive tool.

V. SIMULATED RESULTS

Projected flash type ADC is simulated using Cadence-Virtuoso-IC616 using TSMC-65nm technology, the experimental results for the DC sweep analysis and transient sweep analysis are as extracted in Fig. 8 and Fig. 9 respectively. From these two responses plots, it is illusory that with the variation of the input in systematically rectilinear manner, and output binary bits \( B_0, B_1, \) and \( B_2 \) are perceived; which in sequence appears as 111, 110, 101, 100, 011, 010, 001, and 000 after a specific time interval. This time interval is decided by the systematic variation of the widths and lengths of the MOS transistors used in the design.

Fig 8. DC sweep response of Flash type ADC

Fig 9. Transient response of Flash type ADC

Transient analysis of projected DFAL-TIQ ADC circuit is carried out at several input frequency signal in direction to attain comparative analysis of power consumption at 1.2V; is as presented in Fig. 10.

Fig 10. Power consumption comparison as a function of frequency
Static and dynamic parameters for the proposed design were observed; and DNL/INL plots for ADC with proposed DFAL-TIQ comparator are displayed in Fig. 11 and the conforming values are: DNL is equal to -0.62 LSB / + 0.57 LSB and INL is equal to -0.44 LSB / + 0.41 LSB.

**Fig. 11. Dynamic parameter response plot for proposed ADC**

To determine dynamic parameter of the proposed Flash type ADC, Fast Fourier Transform (FFT) test is a carried out and observed results are as THD = 25.25 dB, SNDR = 18.39 dB, ENOB = 2.76 bits SFDR = 23.4 dB [18].

**VI. CONCLUSION**

In this paper, DFAL inverter based TIQ method has been proposed for decrease in the power consumption in comparator section of Flash type ADC. The proposed arrangement effectively curtailed the power consumption up to 63% of the traditional CMOS inverter based TIQ Flash ADC. The proposed method showed the static and dynamic parameter of Flash ADC and the conforming values are: DNL is equal to -0.62 LSB / + 0.57 LSB and INL is equal to -0.44 LSB / + 0.41 LSB, THD = 25.25 dB, SNR = 19.45 dB, SNDR = 18.39 dB, ENOB = 2.76 bits SFDR = 23.4 dB.

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