

A Proposed Cascaded Multilevel Inverter with R-Load at Different Carrier Frequencies



Lipika Nanda, Aryadhara Pradhan

Abstract: Cascaded multilevel inverter has the major problem as voltage imbalance across the capacitors connected in circuits which are acting like dc sources. The number of level generation depends on the number of DC sources and switches placed in cascaded multilevel inverter topology. In this proposed topology the positive levels and zero levels of the inverter have been explained. This topology also work in symmetrical condition. The topology is simulated in MATLAB and its THDs are calculated at different modulation index. The voltage stress and loss calculations are carried out at different carrier frequencies.

Keywords: THD, Switching loss, Reduced device count, Modulation index

I. INTRODUCTION

In cascaded multilevel inverter as the number of levels increases it increases the net effective switches and DC sources present in the circuit. This may cause the overall system to be more expensive and complex. When all the DC source voltage values are same it is said to be symmetrical and when not same known as asymmetrical configuration[1-3]. The topological improvement of MLIs is an interesting and popular research field to achieve efficient, cost-effective, and compact energy conversion systems[4]. Several innovative MLI topologies, known as “reduced device count (RDC),” have been reported in recent years [5-6]. In this paper a new proposed topology is tested for both symmetrical and asymmetrical configurations. Finally its merits and demerits are also discussed.

II. OPERATING PRINCIPLE

Compared to other existing topologies this topology is simple in design. It consists of 3 DC sources and 6 switches. S_1 and S_2 are bidirectional considering an AC current in the load to impose zero voltage over the load, S_1 and S_2 needs to be bidirectional. The generalized expressions are $S = (N+5)/2$ and $V = (N-1)/2$ where S =number of switches, V =number of voltage sources and N =number of levels.

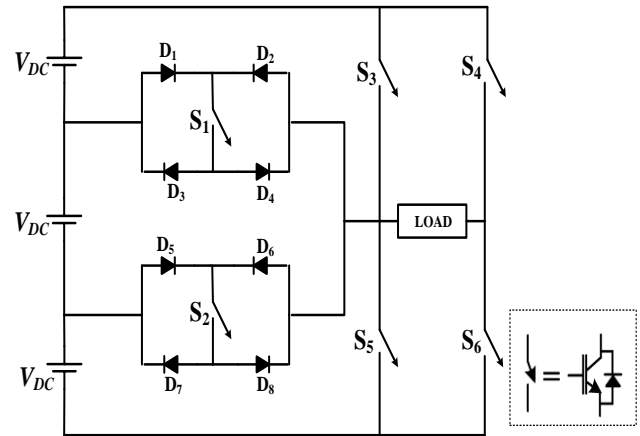
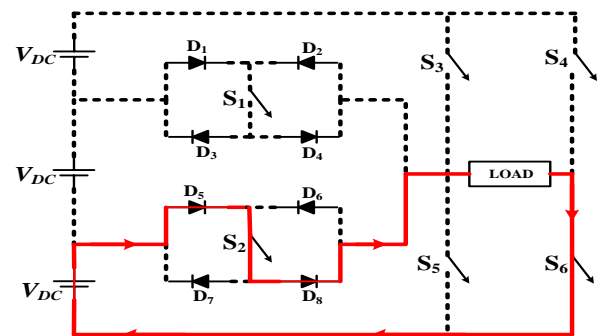


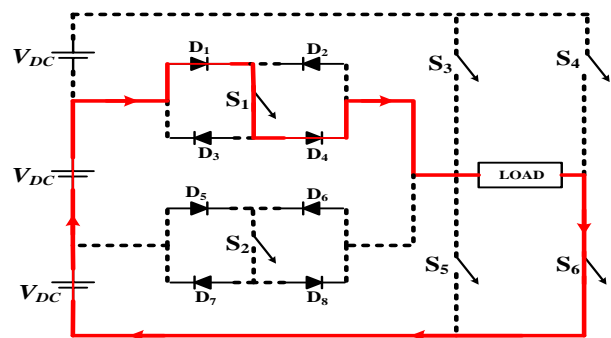
Fig.1 Proposed topology

A. Modes of operation

In this section the positive levels and zero levels of the inverter have been explained. For generating positive V_{dc} across the load terminal bidirectional switch S_2 has been switched on. D_5 and D_8 are the corresponding diodes of the switch S_2 which have been turned on also.



Mode-1



Mode-2

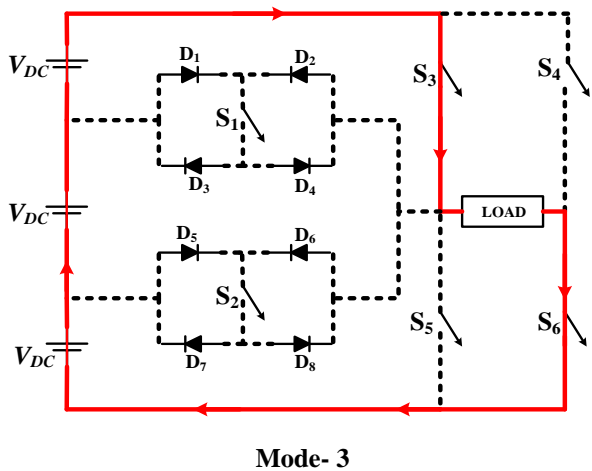
Revised Manuscript Received on December 30, 2019.

* Correspondence Author

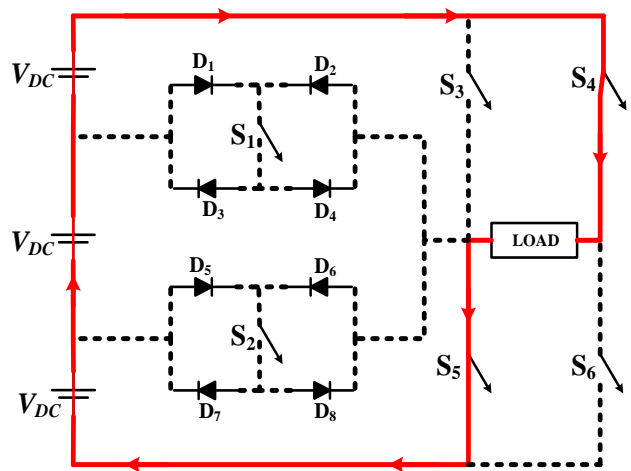
Lipika Nanda*, School of Electrical Engineering, KIIT Deemed to be University, Bhubaneswar, India. E-mail: lnandafel@kiit.ac.in

Aryadhara Pradhan, School of Electrical Engineering, KIIT Deemed to be University, Bhubaneswar, India. E-mail: apradhanfel@kiit.ac.in

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>)

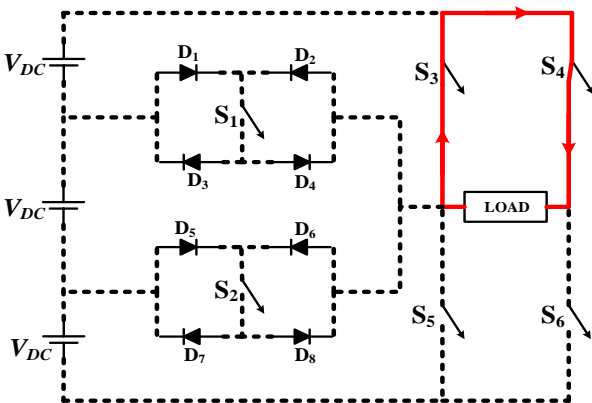


Mode-3

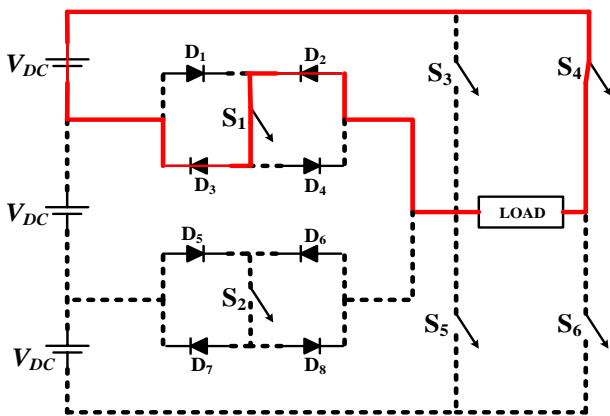


Mode-7

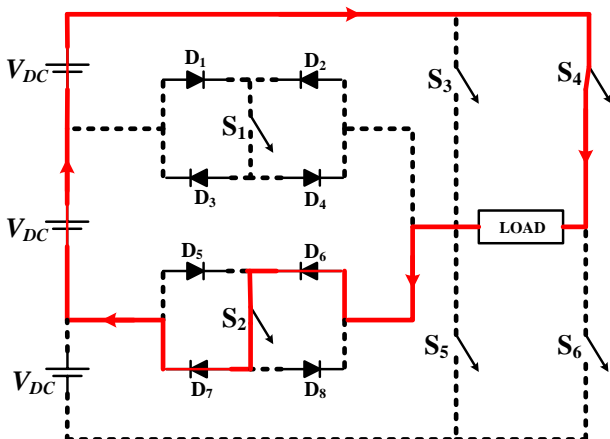
Fig.2. Different modes of operation



Mode-4



Mode-5



Mode-6

B. Switching states

Bidirectional switch S_1 turned on to produce $2V_{dc}$ across the load terminal and current path has been represented in mode-2 operation of the inverter. In mode-3 all the DC sources acting together to produce $3V_{dc}$ across the load. S_4 and S_6 are turned off and switches S_3 and S_6 are turned on in the H-bridge configuration. S_3 and S_4 are turned on and it is represented in mode 4 operation to produce zero level.

Table.I Switching states

Sl. No	S_1	S_2	S_3	S_4	S_5	S_6	D_1D_4	D_2D_3	D_5D_8	D_6D_7	Output voltage (V)
1	Off	On	off	off	off	on	Off	off	on	off	V_{dc}
2	On	Off	off	off	off	on	On	off	off	off	$2V_{dc}$
3	Off	Off	On	off	off	on	Off	off	off	off	$3V_{dc}$
4	Off	Off	On	on	off	off	Off	off	off	off	0
5	On	Off	off	on	off	off	Off	on	off	off	$-V_{dc}$
6	Off	On	off	on	off	off	Off	off	off	on	$-2V_{dc}$
7	Off	Off	off	on	On	off	Off	off	off	off	$-3V_{dc}$

Table I. describes the switching states of inverter. Switching states describe about all the conducting switches along with the conducting diodes in each level generation switches S_1 and S_2 of circuit diagram are unidirectional in nature.

III. SIMULATION RESULT ANALYSIS

All the DC sources are taken as 10 V DC and resistance as 80 Ω. PWM generation is by IPD switching scheme.

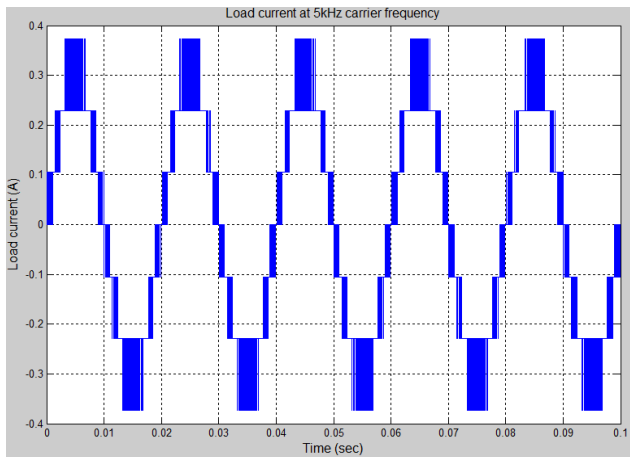
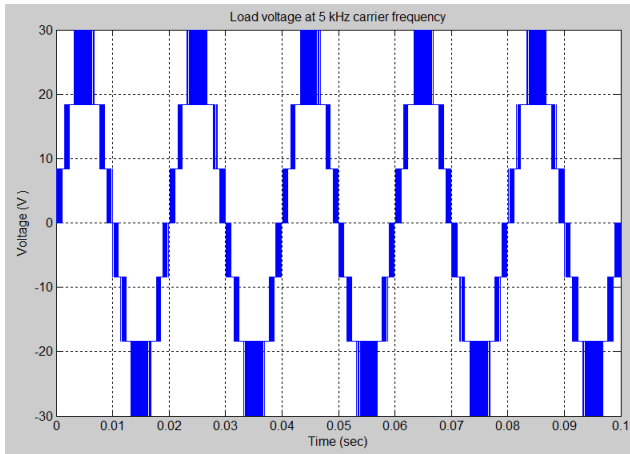


Fig.3. Output voltage and current

Average output voltage =29.06 V and load current =3.6A for R = 80 Ω at carrier frequency = 5 kHz have been obtained.

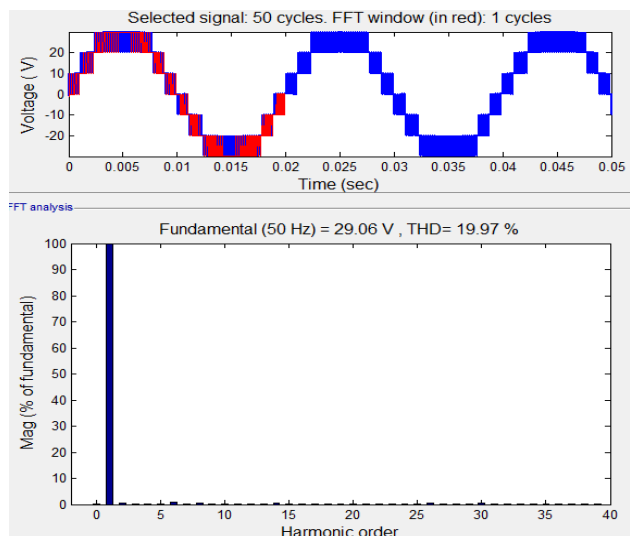


Fig.4. THD analysis of output voltage

At R = 80 Ω, THD=19.97%, fundamental output voltage = 29.06 V.

Table II. Modulation index vs THD

PWM	MI	THD (%)	Fundamental output voltage (simulated)	Fundamental output voltage (calculated)
APOD	0.8	24.87	22.69	24.2
	0.9	24.72	25.66	26.3
	1	20.29	28.9	30
IPD	0.8	24.82	22.82	24.2
	0.9	24.6	25.73	26.4
	1	19.8	29.01	29.9

Table II. presents APOD and IPD switching schemes comparison for voltage THD. At Different modulation index, fundamental output voltages have been simulated and compared with calculated values .

Table III. Voltage stresses across the switches

Conventional topology (V)	Proposed Topology					
	S ₁ (V)	S ₂ (V)	S ₃ (V)	S ₄ (V)	S ₅ (V)	S ₆ (V)
10 V (across all switches)	18.2	18.2	30	30	30	30

IV. LOSS CALCULATION

Two types of power losses: Conduction losses and Switching losses, which are generally occurred in all types of multilevel inverter, are described in detail as below.

A. Conduction losses (P_c) are occurred in ON state of power electronic devices. For this calculation the instantaneous conduction losses of a transistor (P_{c, T(t)}) and diode (P_{c, D(t)}) can be represented as follows:

$$P_{c,T}(t) = [V_T + R_T i^\beta(t)]i(t) \tag{1}$$

$$P_{c,D}(t) = [V_D + R_D i(t)]i(t) \tag{2}$$

Where, V_T and V_D are the voltages of the transistor and diode respectively in the ON-state. R_T and R_D are the equivalent resistance of the transistor and diode, and β is a constant specification of the relative transistor. While calculating the conduction losses the internal resistance of each components (like power switches, capacitors etc) must be same and all the power switches have the same ON-state resistance.

B. Switching losses (PSW)

It occurs when the switch is in a transition state. In transition state, switches position changed from one state to another that is from ON to OFF and from OFF to ON state. The Turn-on and turn-off energy loss (E_{on}, E_{off}) can be represented for switching frequency, f_s as follows:

$$E_{i,on} = \int_0^{t_{on}} V_{sw,i} \left(1 - \frac{t}{t_{on}}\right) I_i \left(\frac{t}{t_{on}}\right) dt = \frac{1}{6} V_{sw,i} I_i t_{on} \tag{3}$$

$$E_{i,off} = \int_0^{t_{off}} V_{sw,i} \left(1 - \frac{t}{t_{off}}\right) I_i \left(\frac{t}{t_{off}}\right) dt = \frac{1}{6} V_{sw,i} I_i t_{off} \tag{4}$$



where $E_{i,on}$ = turn-on loss of the switch
 t_{on} = turn-on time of the switch
 $I_i (I'_i)$ =current through the switch after (before) turning on (off)
 $V_{sw, i}$ = ON-state voltage on the switch.
 $E_{off,i}$ = turn-off loss of the switch I
 t_{off} = turn-off time of the switch.
 To find the energy loss per fundamental cycle, firstly calculate the number of ON transition ($N_{on,i}$) and the number of OFF transition ($N_{off,i}$) per cycle. Then the energy loss per cycle for the i^{th} switches are given below
 The switching power loss of the i^{th} switch per cycle can be expressed as

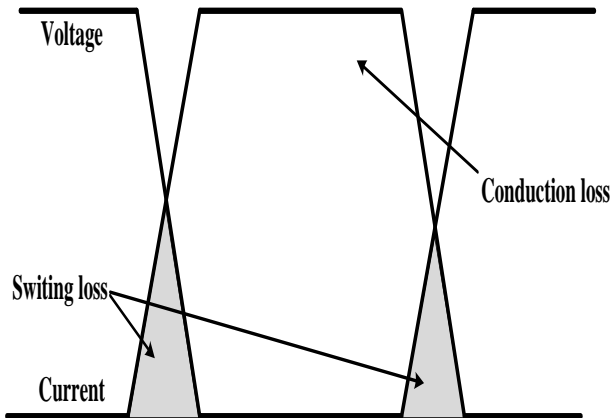


Fig.5. Power losses of power electronic switching devices.

$$E_{i,sw} = (N_{on,i} \times E_{i,on}) + (N_{off,i} \times E_{i,off}) \quad (5)$$

The switching power loss of the i^{th} switch per cycle can be expressed as

$$P_{i,sw} = \frac{(N_{on,i} \times E_{i,on}) + (N_{off,i} \times E_{i,off})}{T} \quad (6)$$

$$P_{sw} = \sum_{i=1}^{N_{switch}} P_{i,sw} = \sum_{i=1}^{N_{switch}} \left[\frac{(N_{on,i} \times E_{i,on}) + (N_{off,i} \times E_{i,off})}{T} \right] \quad (7)$$

The total losses of the MLI will be

$$P_{Loss} = P_C + P_{SW} \quad (8)$$

As losses in inverter are having major role, in order to calculate inverter loss, a voltage measuring device and a current measuring device have been connected with each switch to get inverter loss in MATLAB simulation.

Table IV. Calculation of circuit loss of the inverter

Losses (W)	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	Total loss (W)
Switching loss (W)	0.035	0.0016	0.0012	0.0023	0.05	0.048	0.06	0.06	0.029
Conduction loss (W)	0.0051	0.0052	0.0052	0.0052	0.0055	0.0051	0.005	0.045	0.081
Total loss (W)	0.040	0.0068	0.0062	0.0075	0.0555	0.054	0.065	0.0105	0.0249

Table 4 represents switching loss, conduction loss and total loss of each switch presented in proposed topology . Finally the total loss of the inverter has been calculated .

Table V. Loss of inverter switches at different carrier frequency

Carrier frequency (kHz)	Input voltage (V)	Input current (A)	Input power (W)	Output voltage (V)	Output current (A)	Output power (W)	Circuit total loss (W)
1	40	0.354	14.16	28.35	0.351	9.95	4.05
2	40	0.35	14	28.35	0.35	9.92	4.08
5	40	0.351	14.04	28.35	0.3482	9.87	4.13
10	40	0.345	13.83	28.35	0.354	10.03	3.97
20	40	0.35	14	28.35	0.3475	9.85	4.15

Table 5 represents loss of inverter switches at different carrier frequencies. The circuit total loss increases with increase in carrier frequency. Thus reduces the output power and efficiency of inverter.

V. CONCLUSION

All the simulations are carried out in MATLAB/SIMULINK environment. The circuited is suitable for symmetrical configuration. However it is not suitable for asymmetrical configuration of cascaded multilevel inverter topology. It has been observed that the proposed topology reduces THD to larger extent compared to conventional cascaded MLI topology .At same carrier frequency, if modulation index (MI) increases voltage THD reduces resulting improved sinusoidal load waveform. The voltage stress across each switch has been calculated also.With increase in carrier frequency the inverter losses also increased. Hence the carrier frequency has been kept below the audio frequency range.

REFERENCES

1. K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu and S. Jain, "Multilevel Inverter Topologies With Reduced Device Count: A Review," in *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135-151, Jan. 2016
2. L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo and M. A. M. Prats, "The age of multilevel converters arrives," in *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28-39, June 2008.
3. R. A. Krishna and L. P. Suresh, "A brief review on multi level inverter topologies," *2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT)*, Nagercoil, 2016, pp. 1-6.
4. Y. Hinago and H. Koizumi, "A single phase multilevel inverter using switched series/parallel DC voltage sources," *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA, 2009, pp. 1962-1967.
5. E. Babaei and S. S. Gowgani, "Hybrid Multilevel Inverter Using Switched Capacitor Units," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4614-4621, Sept. 2014.
6. S. P. Gautam, L. K. Sahu and S. Gupta, "Reduction in number of devices for symmetrical and asymmetrical multilevel inverters," in *IET Power Electronics*, vol. 9, no. 4, pp. 698-709, 3 30 2016.

AUTHORS PROFILE



Lipika Nanda had completed MTECH in Power Electronics and Drives in the year 2007. She is working as Assistant Professor, School of Electrical Engineering, KIIT Deemed to be University since 2007. She has more than 10 years of teaching experiences in the field of Power Electronics and Drives. Her major area of interest is multilevel inverters. She has guided 10 M.Tech students and many B.Tech students. She has published 16 papers both in international and national journals.



Dr. Arjadhara Pradhan has completed her Ph.D in the area Photovoltaics and MPPT from KIIT. Her area of expertise is Solar Photovoltaics and renewable energy systems. She was awarded with the "Institutional award" for best paper from Institution of Engineers, Odisha in the year 2012. Her broad working area is Solar Photovoltaics and renewable energy systems.