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Design of a Sampler circuit for Flash ADC using 45nm Technology

Vanitha Soman , Sudhakar S Mande

Abstract*: This paper presents design of a sampler circuit for folding flash ADC. There is a desire for Low power high performance ADC for communication. For low power the size of the ADC should be minimized and for the fast performance flash can be used. Hence to reduce the number of transistors in flash ADC folding network is proposed here. Sampling is the important technique used in the ADC part. In this discussion the sampler circuit includes a differential track and hold switch followed by a variable gain amplifier with a gain of 1 db, a buffer and a folding network. An input voltage of1 V and the sampling frequency of 1GS/s is applied to the sampler circuit. Effective number of bits of more than 5.7 bits is achieved also THD is below -35db in VGA. Buffer achieves a ENOB of 10bits with THD less than -65db. This sampler circuit is designed with the technology of 45nm for coherent sampling. Worst case SNDR is calculated.

Keywords: Variable gain amplifier (VGA), buffer, Effective number of bits (ENOB), Total harmonic distortion (THD).

I. INTRODUCTION

Analog-to-digital converter (ADC) is an essential building block in wireless and wire line communication system. The circuit is used to obtain the digital signal from analog input. To design the ADC system, sampler block is the basic one.

ADC consists of sampler which is the important one for the analog electronics system design [1]. While designing the sample and hold circuit a resistance issue occurred. Hence bootstrapped circuit is developed [2]. But this is not applicable for high speed applications. Low gain pre-amplifier stage is used for sampler circuit for low swing operation [3][4] developed with non time interleaved flash. Non time interleaving is not good for high speed operation and hence these sampler is adapted with the calibration technique [5].Most of the sampling circuit are developed with Flash ADC [6]. Many types are available like Miller capacitance, Switched capacitance, current mode and voltage mode for the S & H circuit design [7-9]. These techniques have been used for high speed applications [10]. In the above mentioned types charge injection and clock feed through are the main issues. Using of the differential switching technique the charge injection could be eliminated [11]. Clock feed through is to be suppressed by dummy switch technique also minimized by the voltage mode sample and hold circuit [12]. Charge cancellation is the main issue in the circuit and hence dummy transistor technique is used. For the high performance current mode S& H is used. Based on the sampling frequency system performance would be increased [13].Low power high performance is the requirement for the ADC Design and hence it is developed [14][15]. This paper presents the design of a sampler with a MOSFET switch, variable gain amplifier, buffer and a folding network module which is used for folding flash ADC. Sampling frequency of (fs) 1GHz and DFT point of 2048 (N= 2048) with 1V is applied for the proposed circuit. This paper is divided into five sections. Section 2 deals with the proposed architecture for sampler, Section 3 discusses the design procedures for MOS switch, VGA, buffer and folding network. Section 4 shows the simulation results and section 5 concludes the paper.

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* Correspondence Author
Vanitha Soman, Electronics and Telecommunication Engineering, Terna Engineering College, Mumbai University, Navi Mumbai, India.
Email: vanitha.soman@gmail.com
Sudhakar S Mande, Professor, Electronics and Telecommunication Engineeing, Don Bosco Institute of technology, Mumbai, India. Email:ssmande@yahoo.com

II. METHODOLOGY

In this work, the circuit is designed using 45nm CMOS technology, with a process parameter as shown in Table II. And the simulations were performed using the cadence software.

A. Architecture of proposed sampler circuit

Figure 1 shows the proposed architecture of the sampler used for folding flash ADC. A Systematic design of sampler circuit for flash ADC is proposed.

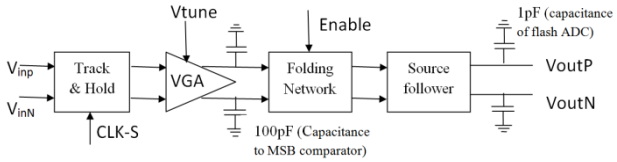

Figure 1

Track & Hold (T & H) which receives an input signal with a bandwidth of 500 MHz and maximum differential input swing of 500mVpp. Variable gain Amplifier (VGA) receives the input from T and H .

The VGA gain will be tuned so that the gain of the proposed VGA is 1. Source follower is proposed to isolate the flash ADC and folding network. These modules are designed and simulated.

III. DIFFERENTIAL TRACK AND HOLD SWITCH DESIGN

Design Specification from table I. Maximum differential input signal swing of 500 m Vpp is applied. Input common mode voltage of 0.4 V with the Sampling frequency fs = 1 GHz is given. For coherent sampling input signal frequency such that, 245 MHz $< f_{signal} <$ 255 MHz and the worst case SNDR > 37 dB (ENOB of 6 bits).

TABLE I: **Design Specification of sampler circuit**

Modules / Input parameter	T & H Switch	VGA	Folding N/W	Source follower
Input	1V	1V	1V	1V
Input common mode Voltage	0.4V	0.4	0.3	0.3
Output common mode voltage	0.4V	0.3	0.3	0.7
Capacitive load		100fF	1pF	100Ff
ENOB	>6 Bits	>5	O/P=0 when Enable =1 O/P=1 when Enable =0	>10bits
Gain range	-	1 < G ≤ 2 (with -3 dB bandwidth > 3 GHz)	-	-3dB bandwidth ≥ 2 GHz
Vtune	-	Vtune 0 V ≤ Vtune ≤ 0.5V	-	-
THD	-	≤-35dB	-	≤-55dB

A. MOS Switch Design

A proper signal frequency is chosen such that condition for coherent sampling is met.

$$\frac{f_{in}}{f_s} = \frac{M}{N} \quad (1)$$

$\tau = R_{switch} * C_H$, R_{switch} is the resistance of switch in triode region,

$$R_{switch} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_T)} \quad (2)$$

TABLE II: **Process parameter for 45nm**

Parameter	value
Cgs0	58.3p F/µm
tox	2.2nm
Cjsw	57 fF/ µm
µnCox	250µA/V^2
µpCox	280µA/V^2
For L= 70nm	VTP= 450mV

TABLE III: **Aspect ratio for MOS switch**

Designed Value	W/L	L	W
Switch	16	45nm	720
Dummy	8	45nm	360

Simulated Value	W/L	L	W
Switch		45nm	12
Dummy		45nm	6

whenever gate voltage of switch is brought down to 0 to Vdd, the inversion charge that was created in channel during on-operation needs to discharge. Here the condition has taken as half of the charge goes to source and other half goes to right and sits on hold capacitor thereby creating an error voltage held in sample value. To avoid this dummy switch is used; these switches suck the charge injected by the main switch during the hold operation. The size of the dummy switch should also be half of the main switch. Aspect ratio values are tabulated in table III. Simulation results of track and hold shown in figure 4 and figure 5

B. VGA CIRCUIT DIAGRAM

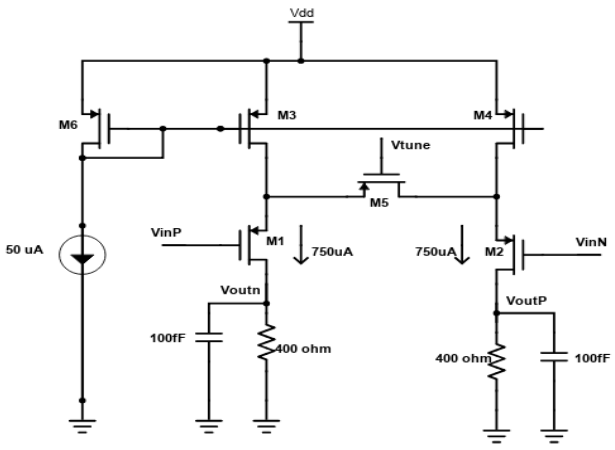

Figure 2

Figure 2 shows the circuit diagram of the variable gain amplifier. The resistance of MOS M5 acts like the source de-generation resistance. By varying the resistance of this MOSFET, the gain of the VGA can be changed. Input voltage Vtune acts as a control voltage to tune the gain of the VGA. Specifications for the VGA from table I, Input common mode voltage = 0.4 V, Output common mode voltage = 0.3 V, Capacitive load of 100 fF (MOS capacitors), Tunable gain (G) range: 1 < G ≤ 2 (with -3 dB bandwidth > 3 GHz), Range of Vtune: 0 V≤ Vtune ≤ 0.5 V, With gain of 1.5, the THD ≤ -35 dB these inputs are applied to the circuit. Schematic diagram shown in figure 6. Calculated aspect ratio values are tabulated in table 4. AC analysis simulation results shown in figure 7 and DFT spectrum shown in figure 8.

TABLE IV: **Aspect ratio values for VGA**

Designed Value	**W/L**	**L**	**W**
MOS Transistors(M1, M2)	4285	70nm	300nm
Current Source(M3,M4)	120	70nm	8.4um
Tunable Load (M5)	50	500nm	25um
Current Mirror(M6)	8	70nm	560um

Simulated Value	**W/L**	**L**	**W**
MOS Transistors(M1, M2)	2857	70nm	200nm
Current Source(M3,M4)	340	70nm	23.75um
Tunable Load (M5)	60	500nm	30nm
Current Mirror(M6)	15	56nm	1um

C. SOURCE FOLLOWER

Common source amplifier is proposed here. The source follower is used to drive the high capacitive load of a flash ADC. The circuit diagram of the PMOS source follower is shown in the Fig. 3.The master transistors (amplifying) transistors ought to operate in sub-threshold region .Current in sub threshold region is given by

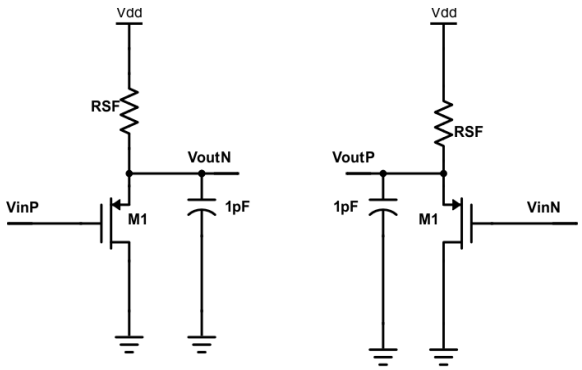

Figure 3

$$I_D = \mu_P C_{OX} * \frac{W}{L} * V_T^2 * \exp \frac{|V_{SG} - V_{TP}|}{\eta * V_{TP}} \quad (3)$$

for the common source amplifier with source degeneration whose gain is given by

$$A_V = \frac{R_D}{\frac{1}{gm} + \frac{R_{ON}}{2}} \quad (4)$$

R_{ON} is the resistance of the MOSFET M5 which is operating in linear region. (W/L) M5 > 24.5, V_{tune} =0,(W/L) M5 < 106.91 V_{tune}=0.5. Current sources M3, M4 are to be in saturation

$$I_D = \mu_P C_{OX} * \frac{W}{L} * (V_{SG} - |V_{TP}|)^2 \quad (5)$$

Design Flow: The specifications for the source follower from table I. Input common mode voltage = 0.3V, Output common mode voltage = 0.7V, Capacitive load of 1pF (MOS capacitors),-3dB bandwidth ≥ 2 GHz, THD ≤ -55dB.

Gain of this source amplifier is given by

$$A_V = \frac{gm * R_{SF}}{1 + gm*} \quad (6)$$

Bandwidth of half circuit is given by :

$$\text{Bandwidth} = \frac{1}{2\pi * R_{eff} * C} \quad (7)$$

In this work source follower is designed for the bandwidth of 2.5 GHz. The amplifying transistors are operated in sub-threshold region. To get aspect-ratio of amplifying transistors (M1, M2), current in sub-threshold region equation is used. Aspect ratio values are tabulated in the table V. simulated results are shown in figure 9 and AC analysis shown in figure 10.

TABLE V: Aspect ratio values for Source Follower

Designed Value	**W/L**	**L**	**W**
M1	4663	100nm	466u
M2	4663	100nm	466u
Resistor	RSF=367 Ω	-	-

D. FOLDING NETWROK

Folding network is proposed here to consider the negative input as a positive one when it is folded. This is designed with the Track and hold circuit. The simulated circuit is shown in fig 11. And the folding network output is shown in figure 12,13.

Results of the all module values are tabulated in table VI.

IV. SIMULATION RESULTS

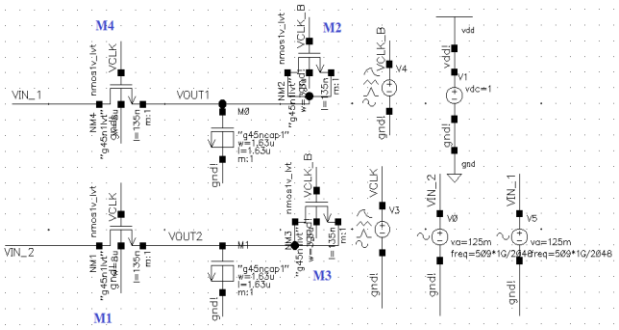

Fig. 4: MOS Switch schematic

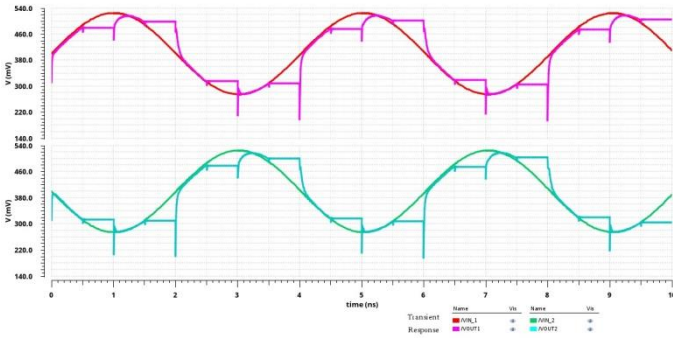

Fig. 5: Differential input and output of the switch

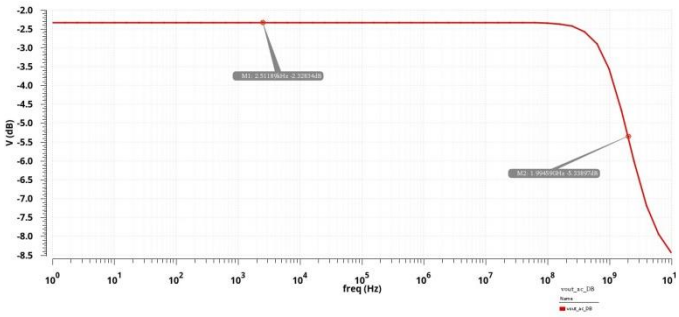

Fig. 7: AC Analysis of VGA

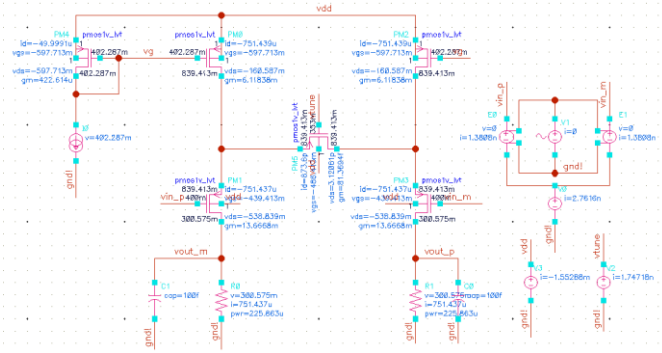

Fig. 6: Schematic of VGA

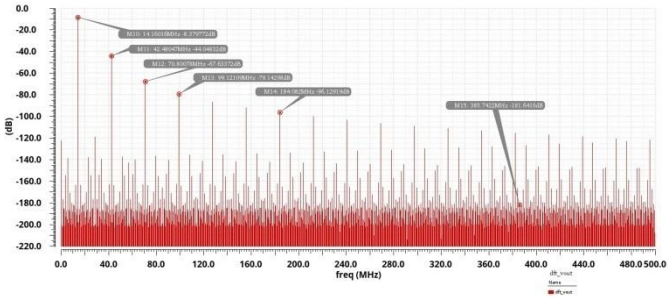

Fig. 8: DFT spectrum of VGA

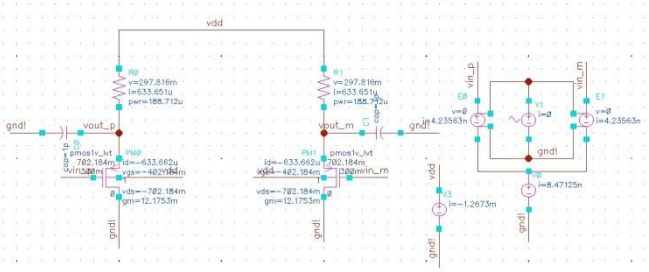

Fig. 9: Schematic of Source follower

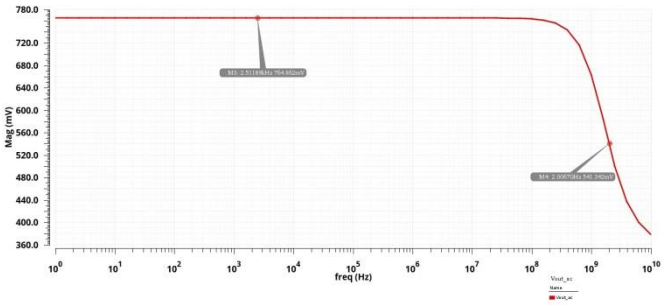

Fig. 10: AC analysis of source follower

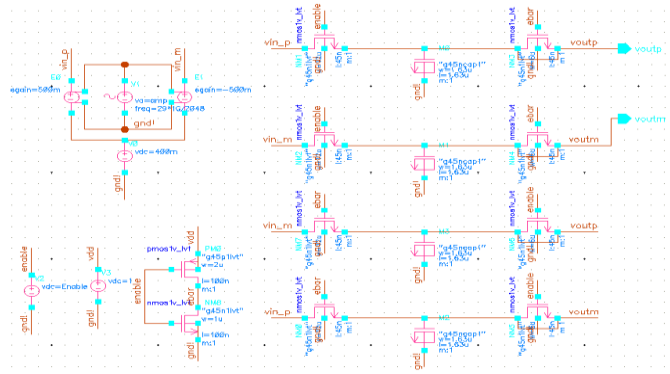

Fig. 11: Schematic of Folding network

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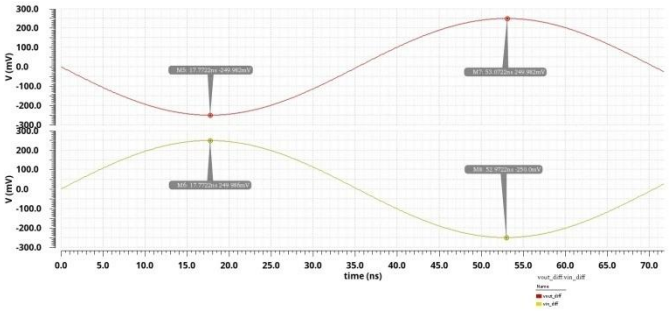

Fig. 12: Folding Network Output when Enable=0

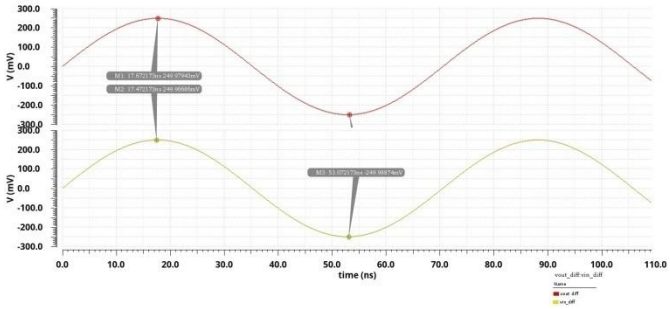

Fig. 13: Folding Network Output when Enable=1

TABLE VI: **Result of sampler circuit 45nm technology**

Modules Output Parameter	Switch	VGA	Source Follower	Folding Network
Input (Volt)	1	1	1	1
ENOB (Bits)	>6.452	>5.628	>10	Enable=0 o/p=1
SNDR	40.6093	35.6436	62.4043	Enable=1 o/p=0
SFDR	40.6678	35.668	62.409	-
THD	-	-35.647	-62.4096	-

V. CONCLUSION

In this paper the sampler circuit for folding flash ADC with folding network is designed with the 45nm technology. According to the design specification the modules are simulated and verified with the designed aspect ratio vales for the input of 1V with 1GS/s. The proposed system of folding network is achieved output for the enable values. Effective number of bits has been achieved as good as for the next level design. Simulation results have confirmed that this sampler circuit is suitable for the flash ADC design. With the help of this proposed folding technique a 4 bit ADC would be developed with the less number of CMOS transistors. This sampler circuit is the enhancement for the folding flash design for the next phase of our research work.

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AUTHOURS PROFILE

Vanitha Soman is a research scholar in Electronics and telecommunication engineering under Mumbai university. She has received her ME(Applied electronics) degree from Anna University, Trichy (2011). She is interested in analog and mixed signal systems for electronics.

Sudhakar S Mande has a Ph.D in Microelcetronics from IIT Bombay (2011). He has published many international journals. His interested areas are analog and digital VLSI, Embedded systems and Image processing.