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Design of Self Controllable Voltage Level Circuit (SVL) for Low Power and High Speed 12t Sram at 15nm Technology

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Abstract: - Due to trend of decreasing the device Size and increase in the chip density, the complexity in design increased and it became very complex. The main factor which is main concern in this step is Power dissipation. This can be occurring in many forms like Dynamic, subthreshold leakage and Gate leakage. For every situation the designer has to try to reduce this Power Dissipation factor. In this paper we designed a low power 12T SRAM by using the 15nm technology. SRAMs have large number of applications in high speed registers, microprocessors, small memory banks, general computing applications etc. Therefore delay, power, speed, leakage current and stability are the main concerns. These parameters are in trade off to each other. This paper focuses on the leakage current, power and stability in 12T SRAM bit -cell. We introduce a circuit "self - controllable Voltage Level (SVL)" circuit. The main task of this circuit is to reduce the stand-by leakage power of 12T SRAM. In our Work, We are using the Cadence Virtuoso simulation tool for simulating our circuit. After Comparing our results to the previous methods used for reducing the power leakage we found that there is reduction in average power compare to the previous methods used for power reduction techniques.

Keywords:- SRAM, SVL 15nm,Cadence, 12TSRAM, Leakage current, Static Noise Margin(SNM).

I. INTRODUCTION

Basically in Digital design two types of Memory used :- RAM(Random Access memory) & ROM(Read Only Memory). Out of these two in digital circuit design we are mainly using RAM. SRAM is widely used compare to the DRAM in Digital design. RAM is also known as Read-write Memory [1]. The nature of RAM is Volatile, meaning of volatile is that the data which is saved in the SRAM it will be vanished once the power of the circuit is off. Memory is one of the important factors on which digital circuit depends. The reason behind it is as it is used to store and save the data in the binary form. The data which we get from the input device will be stored in memory in the form of binary and after processing on these binary data it will be go to output device to show the result [2].

Except RAM and ROM there are two other types of memory which are used in the digital world :- Semiconductor and magnetic memory. Semiconductor memories are used for faster operation in small capacity [3].

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There are three states in which the SRAM operates. These are:- Standby stage (in which the SRAM memory circuit is in ideal situation), Reading stage (in which the data is requested by circuit) & Writing stage(In this stage the data contents are going to be updated)[4-5].

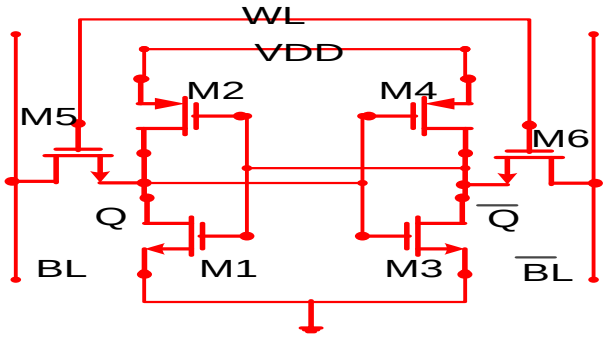

Figure1 : Basic SRAM structure

Figure 1 shows basic structure of the SRAM. The three state of the SRAM can be understood by the help of the figure1[6].

Standby State :-

If the Word line is not clamed, the Transistor M5 and M6 are not going to be operated as it is disconnected from the bit lines . Transistor M1 to M4 will form two cross coupled inverters. Theses transistor will support each other as they all are associated to power supply[8-9].

Reading :-

The read cycle of the SRAM will started by pre-charging the BL AND BL! . By pre-charging the bit lines will reach to the threshold value. By enabling the ,the word line WL the functions of all the transistors can be evaluate . The M_5 and M_6 transistors can be enabled by using the word line WL. The bit line BL voltage will be either slightly drop when then transistor M_3 is ON as it is NMOS and transistor M4 will be in off as it is PMOS. It may be in the rise condition when transistor M4 is on condition as M4 is a PMOS . With help of a amplifier which can be work as a sense amplifier we can realize which line has the higher voltage and by that we can tell whether **1** or **0** stored.[10]

Write:-

The writing in SRAM totally depends on the status of BL and BL! If we want to write 0 then there should be supply of 0 to BL and vice versa. The stability of the NMOS are more than the PMOS transistors when both are of same sized. Consequently, when there is writing process is going on in one transistor pair for example M3 and M4 , there will be also change in the voltage level of the other transistor pair which is in opposite , for example M1 and M2.

This means that the M_1 and M_2 transistors can be easily controlled by other transistors and so on. Due to this reason cross-coupled inverters will start, the magnify the writing process.[11]

II. TYPES OF THE SRAM

4T SRAM

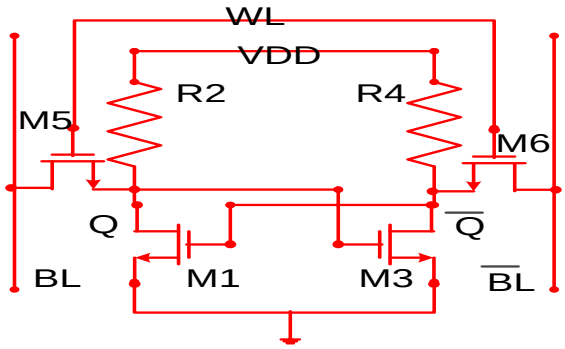

Figure 2. The 4T SRAM

Figure 2 shows the 4T SRAM . The Four transistor SRAM have the advantage of density. The resistors of 4T SRAM have small volume and it can store large values. This type of memory can be used in Video memory. The cost of per memory bit is less as we can pack more bits on a one wafer due to reason of fixed cost of processing a silicon wafer in one wafer. The SRAM can be enabled by using the word line WL , which can access the transistor M5 and M6 .The bit lines BL and BL! Are the main thing by which we can find whither transfer of data is on read or write operations? In the Read stage, the bit line will be go High to Low and Low to High due to the inverts presented in the SRAM cell. Due to this reason the SRAM is better than the DRAM. In DRAM, we are using storage capacitor, due to which the bit line will swing upwards and downwards. The size of an SRAM with m address lines and n data lines is 2^m words, or $2^m \times n$ bits.

8TSRAM

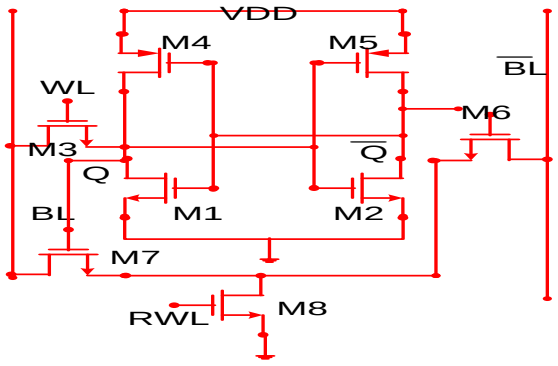

Figure 3. 8T SRAM.

Figure 3 shows the 8TSRAM. The main advantage of the 8T SRAM cell is reduced leakage current and the less dynamic power consumption by it. In this SRAM , the M3 will work as write access transistor . This transistor will be handled by the write word Line (WWL). The M8 transistor will work as read access transistor, which will be controlled by the read word line(RWL). During the write operation the WWL will go high and RWL will maintained to Vgnd. Due to this reason transistor M8 will be cutoff. To write "1" into the cell Bit Line (BL) is pre-charged to a high value. And it will be forced to the write access transistor M3. To write "0" into the Bitcell line (BL), the BL will be discharged . To perform the write operation the BL, will reduced the dynamic power decay and leakage power. During read operation, RWL will go to High and the WWL will be kept at Vgnd. In this process the write access transistor will be cut off . Assume that "1" is stored in the left and "0" is stored in right side. The BL will be discharged from the transistor M7 and M8. The transistor M6 will be cutoff .

9TSRAM

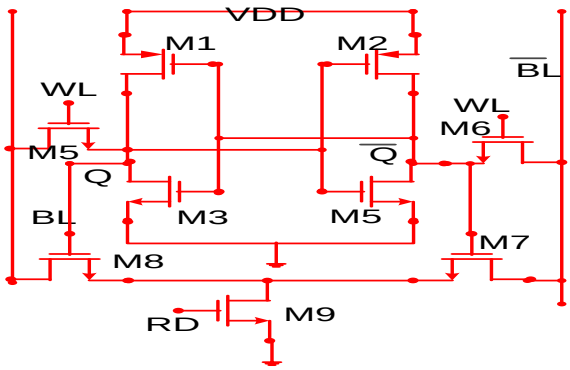

Figure 4 . 9TSRAM

Figure 4 shows the 9TSRAM. In this SRAM, two write Access Transistor, M5 and M6 will be controlled by the write signal WL. This type of SRAM consist of two parts . The upper Sub-Circuit consist of 6 Transistors (M3,M4,M5,M6,M1& M2). The data will be stored in this upper sub-circuit part only. The lower Sub-part consist of three Transistor. The bit line Transistors M7 &M8 and read access transistor M9. The M7 and M8 will be handled by the data stored in the cell. The M9 will be controlled by the read signal (RD).

10TSRAM

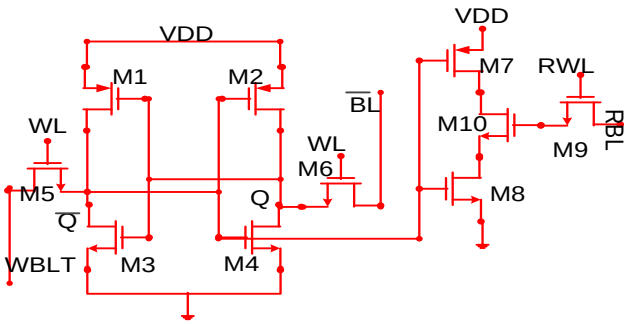

Figure 5 10T SRAM

Figure 5 is the 10TSRAM. In this type of SRAM There are 10 transistors M1 to M10. Basically, it is identically to the 6TSRAM. Only the difference is that M1 and M2 are connected to a virtual supply voltage rail of Vdd. The write access occurred to the write access transistors M5 & M6. There will be write bit lines WBLT and WBLC. Transistors M8 to M10 used a buffer for reading operation. Read Access will be occurred by the help of RBL. RBL is pre -charged for the read access. The word line for the read operation is different from the write word line.

III. PURPOSED METHOD

1.1 Self-Controlled Voltage Level (SVL)

By the self-controlled Voltage level (SVL) we can control the dc voltage for active load circuit. By this voltage level a maximum dc voltage can be maximized on the request also it can be go to stand mode by decreasing the voltage level. **Figure 6** shows the simplified diagram of SVL of 12T SRAM.

By the SVL , the leakage power can be drastically reduced of CMOS logic circuit. By SVL there will be minimal overheads in the terms of the chip area and the speed of the CMOS logic circuits. The SVL will also help in the retaining the data even in the standby mode. Basically there are two Techniques to control and reduce the leakage power (Pst):- One is to use a multi threshold-voltage CMOS (MTCMOS) and another technique involves by using a variable threshold-voltage CMOS (VTCMOS)

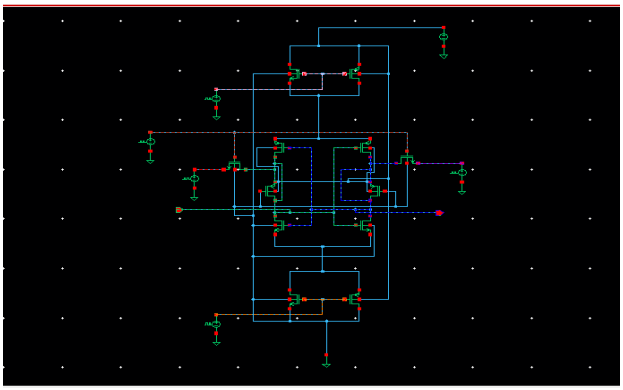

Figure 6 Schematic diagram of SVL of 12T SRAM

In the MTCMOS technique the Pst reduced by removing the power supply by using the high threshold voltage MOSFET switches. The main problem in this is both memories and Filp-flops can not hold the data after it.

In the VTCMOS technique , reduces the Pst by increasing the substage biases. In this technique also there is some problems like a large area penalty and a large power penalty . The reason behind it is that substrate-biased supply needs low leakage power.

The SRAM will be in active mode if the Clock pulse will be low. In this situation there will be no degradation in the SNM (Static Noise Margin). In the Standby Mode, the Clock pulse CL will go to High and due to this reason the supply voltage of the SRAM will reduced .This will also decrease the leakage current and it also reduces the static Nosie Margin (SNM).

3.1.1 Multiple Threshold Voltage CMOS:

In the method, we have multiple transistors with Multiple Threshold voltages (Vth), due to this reason we can optimise delay and power. The Vth of the MOSFET is the voltage which is formed at gate which occurred at the interface between insulating layer i.e oxide and the substrate i.e body of the Transistor. Low Vth will be useful in the critical paths for minimize the clock period. Also the low Vth switches very fast. But the problem in the low Vth is that they have high static leakage power. High Vth can be used to reduce static leakage power which is 10 times compare to the low Vth devices. There are two techniques by which we can create this type of CMOS. First one is to apply variable bias voltage (Vb) to the base or the bulk terminal of the Transistor. Another Method is by adjusting the gate oxide thickness and the gate oxide dielectric constant.

The main drawback of this method is maintain the proper biasing level .

3.1.2 Variable Threshold Voltage:

In this Technique, the threshold voltage of the low threshold are varying by the help of the variable substrate bias voltage by a control circuitry. This method requires twin well or the triple well techniques. The area overhead of the substrate bias control is very less in this . The biggest problem in this technique is that for implementing this technique we need a very large area.

In our Purposed technique, the Self Controllable dc circuits can be used to reduce the leakage power. The main advantage of this circuit us that based upon the requirement the circuit will get the power supply and if not required it will be cut off , which means it will be in standby. Also by using our technique the leakage power can be reduced , especially in the standby mode

IV. WORKING OF THE PURPOSED CIRCUIT

During the read and write cycle both high SVL and low SVL are ON. During steady state both these HSVL and LSVL are OFF to save the power. Due to the use of LSVL and HSVL the drive voltage for inverter gets reduced. This will no doubt decrease the power loss but increase the response time of inverter (transient time to switch) to remove this problem two diode connected MOSFET'S are used.

During standby mode condition both high SVL and low SVL are in OFF condition. Only the cross coupled inverters work in order to store the data. Here the two pre-charge transistors are used in order to reduce the voltage which is created at the points M5 and M6 when they are in ON condition

V. RESULTS AND DISCUSSION

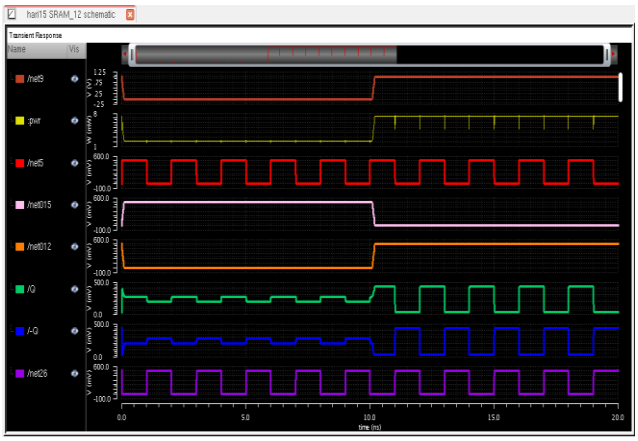

Figure 7 Output waveform1

The above **figure 7** explains that when the word line is 0 the output waveforms Q and –Q consumes less power and when the word line is 1 then the output Q and –Q gives whatever the bit lines is given whether it is read/write operation.

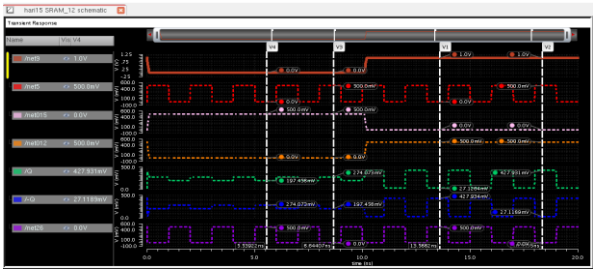

Figure 8. Output waveform2

The above **figure 8** clearly says that SRAM consumes less power when the circuit is in standby mode whether it is read/write operation.

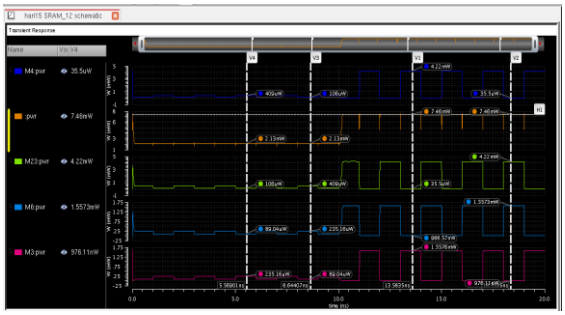

Figure 9. Output waveform3

The above **figure 9** explains that the power consumption of NMOS and PMOS transistors used in low power SVL 12T SRAM. It explains that the NMOS and PMOS consumes less power when the circuit is in standby mode.

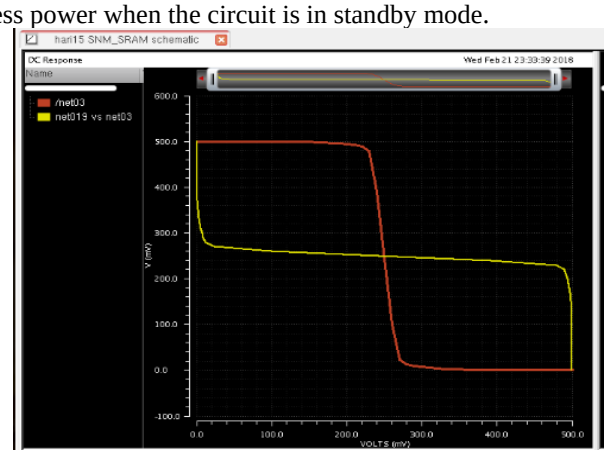

Figure 10. SNM graph

The above **figure 10** shows a graph which clearly states the performance of SRAM is improved by considering the value largest square of noise voltage of two cross coupled inverters. Because of this the noise immunity increases and speed also increases.

Observation Table

Table 1 observations of the proposed design

Reference	Technology	Supply Voltage	Precharge Voltage	Power consumption	Leakage current
SVL circuit for low power 7T SRAM cell	45nm	0.7V	1V	8.15mw	4.18pA
Proposed method	15nm	0.5V	0.3V	7.46mw	1.38pA

From the above table 1, we can easily find out that the power consumption and leakage current are reduced compared to the previous proposed SVL circuit for SRAM. In this we have used 15nm technology in order to consider the lower voltage for the transistor in order to work even in sub threshold region.

VI. CONCLUSION AND FUTURE SCOPES

In the previous proposed SRAM circuits the power is consumed even when it is not required i.e. in standby mode. In the procedure of reducing the consumption of power a low power SVL 12T SRAM circuit is proposed. In the proposed circuit self-controllable dc circuits are used to minimize the leakage power.

The advantage of this circuit is when required its supply voltage to the circuit and if not required it cut off the supply voltage (cut off means here reduce the supply voltage to stand by the technique). This technique drastically decreases the leakage power in the standby mode.

In **our purposed circuit** , there are other several advantages as high Vds is used to load circuits for high speed operations. In the stand-by mode it will be used to load the minimum Vds. SVL can also used for small power dissipation , less speed degradation nd also very less overhead .Even by the SVL we can get high noise immunity and data retentions

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