International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-9 Issue-2, December, 2019

Mathematical Modeling, Control Design, Simulation & Implementation of Electric Vehicle Charger

R. G. Mapari, D. G. Bhalke, Rahul Parbat

Abstract*: A proposed technique to deal with improves the power factor of single-stage rectifiers and to control the load voltage against the adjustment in grid voltage and load is exhibited. This converter topology is assessed based on execution and its remarkable highlights like simple in construction, cost efficient and high degree of performance are communicated about to examine its correctness. The proposed control technique is bridgeless, transformer-less and output current sensor-less and comprises of just two Bi-directional IGBTs and two diodes. The voltage control is accomplished by a simple voltage divider to convey to a controller to control the duty cycles of pulse width modulated signal. This paper concentrated on the numerical displaying of single stage bi-directional converter utilized in electric vehicle.

Keywords: Bridgeless-Sensor-less-Transformer-less converter, duty cycle single phase converter, PWM converter, voltage regulation.

I. INTRODUCTION

In upcoming years, the design and development of electric vehicles (EVs) is estimated to boost exponentially, because of the wasting of oil and the natural effect related with its utilization. Hence, there is an inclination to arrange endeavors to decrease urban contamination and ozone harming substance outflows.

At present, one of the most significant issues in EV improvement is the lack of charging foundation [1] [2]. One can charge EVs at home; however the charge time is very long. To advance the EV improvement, it is important to introduce quick charging mechanism for charging stations in which the EV battery must be charged in very small time. On the other hand, the weakness of quick charging is the powerful request and its effect on the framework. So as to address this, sustainable sources and capacity frameworks can be introduced in these stations [2].

This paper is centered on the factor of mathematical modelling of an EV quick charging strategy. So as to improve the gainfulness of the quick charging stations and to diminish the high vitality requested from the conventional electricity sources.

Revised Manuscript Received on December 30, 2019.
* Correspondence Author
Dr. R. G. Mapari*, Dept. of E &TC, PCCOER Ravet, Pune, India. Email: rahul.mapari@pccoer.in
Dr. D. G. Bhalke, Dept. of E&TC, AISSMS COE, Pune, India. Email: dgbhalke@aissmscoe.com
Mr. Rahul Parbat, Dept. of E&TC, PCCOER Ravet, Pune, India. Email: rahul.parbat@pccoer.in

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC BY-NC-ND license (http://creativecommons.org/licenses/by-nc-nd/4.0/)

II. MODELING

In primary stage, modelling of primary switch, driver, controller inductor and capacitor design has been considered for complete modeling of single phase converter.

A. Modeling of Switch

Identification the importance, IGBT semiconductor device as a switch is chosen. As IGBT having features like high switching recurrence and high current conveying capacity. The examination among IGBT and MOSFET switch dependent on frequency and voltage handling of capacity is appeared in Fig. 1.

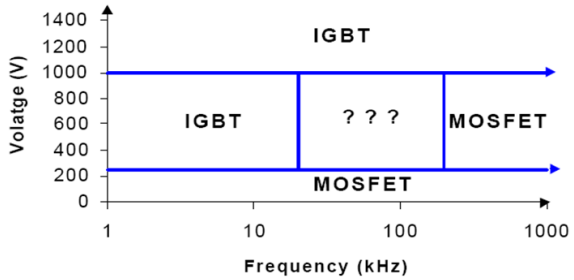


Fig. 1.Comparison between IGBT and MOSFET switch

B. Modeling of Driver

For active conversion of voltage sources author choose IGBT switch as mentioned in above section. To drive IGBT's two driver cards are available, one is International Rectifier (IR) series most popular IR210 and second is VLA 503 hybrid IC. According to our design most suitable driver is VLA503 because of its features as mentioned below [3],

- Electrical isolation- High and low voltage isolation between input and output of the system through optocoupler,
- No bootstrap operation is required,
- Gate suddenly OFF the switch due to +15V and -9V provision.

C. Modeling of controller

For controlling and computerized usage of a large portion of the piece of the framework creator favored DSPic33FJ64mc802 controller, which having every one of the highlights of advanced sign processor (DSP). ASIC IC's are readily available in the market which having all operations in one pack.

But it is not suitable for our project because of following problems,

- In ASIC bi-directional flow of power is not allowed,
- Duty cycle remains constant and switching frequency varies. And the range of switching frequency is from 60 KHz and above.
- As switching frequency increases inductor size is reduces but problem is it require ferrite material which is costly.

Against that DSPic33FJ64mc802 controller removes all above drawback also in our project we vary duty cycle by keeping switching frequency constant (20 KHz). The features of DSPic33FJ64mc802 digital controller are as given below,16 bit digital signal controller,

- Linear data memory upto 64Kbytes,
- Flash program memory 64Kbytes,
- RAM 16Kbytes,
- ADC 10 bit,
- Operating voltage 3.3V,
- 28 pin integrated circuit(IC)

D. Input inductor Design

The inductor swell current is 20% to 40% of the yield current. For our design we consider it 40% of output current.

$$\Delta IL = 0.4 \times Io \times \frac{VDC}{VINpeak}$$

$$\therefore \Delta IL = 1.23$$

ΔIL = estimated inductor ripple current
To find inductor value we use formula as given below;

$$L = \frac{VINpeak \times (Vo - VINpeak)}{\Delta IL \times fs \times Vo}$$

V_{IN}peak = typical input voltage
V_o = desired output voltage
f_S = minimum switching frequency of the converter
ΔI_L = estimated inductor ripple current

$$\therefore L = 1.90mH$$

E. Output capacitor Design

Best practice is to use low equivalent series resistance (ESR) capacitors to limit the wave on the yield voltage. Fired capacitors are a decent decision if the dielectric material is better. With outer remuneration, the accompanying conditions can be utilized to alter the yield capacitor esteems for an ideal yield voltage swell:

$$Cout(min) = \frac{Iomax \times D}{fs \times \Delta Vout}$$

Where,
Cout (min) = minimum output capacitance
Io (max) = maximum output current of the application
D = duty cycle
fs = minimum switching frequency of the converter
ΔVout = desired output voltage ripple
The ESR of the output capacitor adds some more ripple, given with the equation:

$$\Delta Vout(ESR) = ESR \times \left\{\frac{Iomax}{1 - D} + \frac{\Delta IL}{2}\right\}$$

Where,
ΔVout (ESR) = additional output voltage ripple due to capacitors ESR
ESR = equivalent series resistance of the used output capacitor = 0.1
Iout (max) = maximum output current of the application
D = duty cycle calculated in table 3.3
ΔIL = inductor ripple current

$$\therefore \Delta Vout(ESR) = 0.499$$

$$\therefore Cout(min) = 105\mu F$$

From above values of inductor and capacitor, for our work we choose the values shown in TableI.

Table I. Values of selected inductor and capacitor

Sr. No.	Parameter	Symbol	Value
1.	Input inductor	L	1mH
2.	Output capacitance	C	440µF

III. CONTROL BLOCK FOR SINGLE PHASE CONVERTER

Fig. 2 shows the control block for single phase converter to achieve the high power factor, DC voltage regulation, bi-directional power flow and reduced current harmonics.

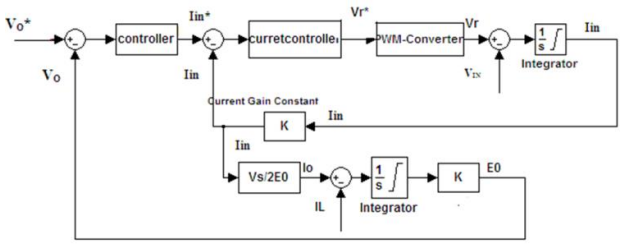


Fig. 2.Control block for single phase converter

V_O* is the reference yield voltage that we need to accomplish. The genuine criticism voltage VO is contrasted and the reference voltage V_O* [4]. The result of the comparator is the difference between them we called it is blunder; this distinction is then input to the voltage controller so as to make the move against it. Since any adjustment in yield capacitor voltage V_O as appeared in Fig. 3.9 because of progress in load there is change in load current and we know in perfect case for 100% productivity yield control is equivalent to include control.

$$V\hat{}in \times I\hat{}in = vo \times IL$$

V^in and *I^in* are top estimations of info voltage and information current. As IL changes, the item *Vo×IL* change so to remunerate it top worth *I^in* important to change henceforth yield of controller is *Iin** that is required reference input current. This *Iin** moving through inductor. The real information current *Iin*is detected and contrasted and the reference input current *Iin**. The distinction between them is nourished to the present controller. The present controller is balanced with the end goal that for any adjustment in input current *Iin*, it change the normal central voltage *Vr (VAB)*.

Consequently yield of controller is reference normal principal voltage *Vr** and is nourished to the PWM converter. This reference principal voltage is goes about as a tweaking sign to the PWM converter. The bearer recurrence is picked so high that PWM converters activity turns out to be quicker, so that *Iin* and *Iin** stays sinusoidal and unaltered. Likewise *Iin* and *Vin* both are sinusoidal and in stage to get high power factor.

From Fig. 2 the input side representation of the single phase converter circuit is shown in Fig. 3. From this we can find the actual input current Iin.

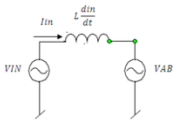


Fig. 3.Input side representation of the single phase converter circuit

By applying KVL, we can write the equation

$$VIN + L\frac{din}{dt} = Vr$$

$$\therefore Vr - VIN = L\frac{din}{dt}$$

By taking integration of both sides, we can write,

$$Iin = \frac{1}{L}\int (Vr - VIN)dt$$

This real information current *Iin* with current increase *K* is nourished to the comparator where it is contrasted and reference input current *Iin**.

The real yield voltage V_O is discovering utilizing the real information current *Iin*. We know for the high info control factor utilizing power balance, $VINrms \times Iinrms = Vo \times Io$

$$\therefore \frac{VINpeak}{\sqrt{2}} \times \frac{Iinpeak}{\sqrt{2}} = Vo \times Io$$

Iinpeak already we know,

$$\therefore Io = \frac{VINpeak \times Iinpeak}{2Vo}$$

This is the DC estimation of yield current. Capacitor esteem has been picked to such an extent that DC voltage swells are limited. From above condition we can draw the square schematic as appeared in Fig. 4 to ascertain DC estimation of yield current.

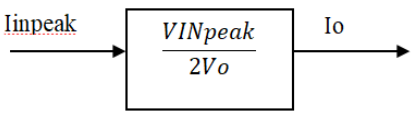


Fig. 4.Block schematic to obtain output current

This present *Io* is sustained to the comparator where second information is stacking current *IL*. Undeniably yield capacitor current *Io* and burden current *IL* both are same, subsequently the contrast between them is zero. Assume at any moment load changes the heap current *IL* will transform, it answered to the controller that the distinction between capacitor current *Io* and burden current *IL* gets more noteworthy than zero. This distinction is sustained to the integrator which goes about as a controller to control the yield voltage V_O this is appeared in Fig. 5.

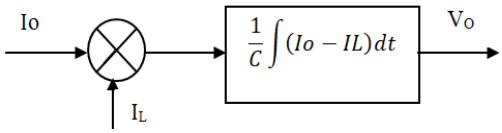


Fig. 5.Block schematic to obtain output voltage

From Fig. 3.2, the output side representation of the single phase converter circuit is shown in Fig. 3.8. From this we can find the actual output voltage Vo.

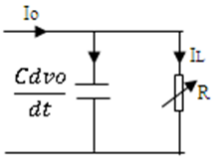


Fig. 6.output side representation of the single phase converter circuit

The actual output voltage is finding out by applying KCL at the output side of single phase converter circuit as shown in Fig. 6 it is given below,

$$Io = \frac{cdv}{dt} + IL$$

By simplifying above equation,

$$(Io - IL) = \frac{cdvo}{dt}$$

Using this equation, the output voltage can be written as,

$$vo = \frac{1}{c}\int (Io - IL)dt$$

IV. DESIGN OF PWM CONVERTER

Fig. 7 shows the generalized waveform to visualize the PWM scheme. Triangular wave is fixed with high recurrence so as to make the quick move [5]. We accept it as 20 KHz for the recreation and experimentation. The normal central voltage Vr*(t) is goes about as an adjusting signal. For all intents and purposes, despite the fact that the triangular recurrence is high there is a postponement between activity started period and real move made period. That defer we called as a first request slack and it is of one triangular period Tr. It is appeared in Fig. 8.

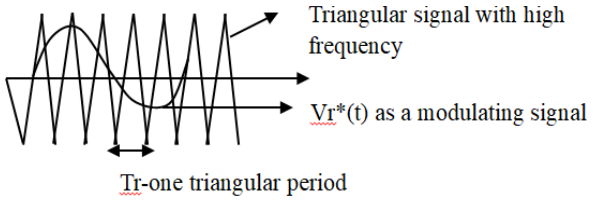


Fig. 7.Generalized waveform for PWM generation

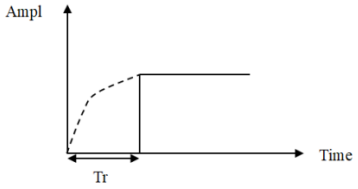


Fig. 8.Fig. 3.10 Representation of first order lag.

The reference average fundamental voltage Vr* depends upon actual output hence it require a gain we called it as G. The PWM converter with first order lag is denoted as, and it is shown in Fig. 9.

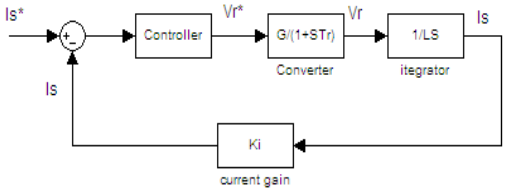


Fig. 9.Control block for the PWM converter

V. DESIGN OF CONTROLLER

Structure of controller depends on the way that the unfaltering state blunder (the contrast between reference input and real criticism yield of the framework) ought to be zero and at the zero crossovers time frame increase ought to be high. The PI controller utilizing operation amp is appeared in Fig. 10.

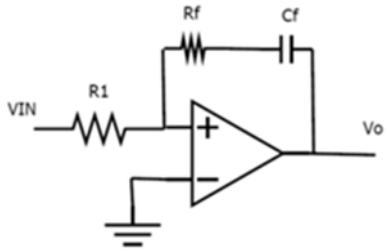


Fig. 10. PI controller using op-amp

The gain of the controller in Laplace domain is given as,

$$\frac{Vo(s)}{Vi(s)} = \frac{Rf}{R1} + \frac{1}{R1Cfs}$$

We take $\frac{Rf}{R1} = K$

$$\therefore \frac{Vo(s)}{Vi(s)} = K\left[\frac{1 + RfCfs}{RfCfs}\right]$$

Above equation is express in terms of, $K\frac{(1+sT)}{sT}$ as a controller to have a zero steady state

$$\lim_{s\to 0} s.E(s) \quad = 0$$

E(s) is the steady state error. By choosing the value of 'T' the phase can be adjusted and infinite gain is obtained at zero frequency. Using above PI controller the control block is show in Fig. 11.

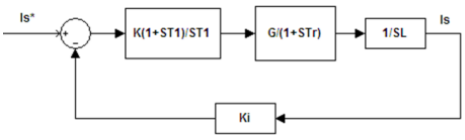


Fig. 11. The control block using PI controller

The transfer function of above block is given as,

$$\frac{Iin(t)}{Iin^*(t)} = \frac{G(s)H(s)}{1 + G(s)H(s)}$$

$$= \frac{\frac{K(1+sT1)}{sT1} \times \frac{G}{(1+sTr)} \times \frac{1}{sL}}{1 + \frac{K(1+sT1)}{sT1} \times \frac{G}{(1+sTr)} \times \frac{K}{sL}}$$

We choose T1 such that the dominant large elements are canceled, i.e.$T1 = Tr$, Hence $(1 + sT1)$ and $(1 + sTr)$ get canceled then above equation can be simplified as,

$$\frac{Iin(t)}{Iin^*(t)} = \frac{(s^2LT1KG)/_{s^2T1L}}{S^2LT1 + KGKi}$$

$$\therefore \frac{Iin(t)}{Iin^*(t)} = \frac{KG}{s^2LT1 + KGKi}$$

Any reaction of a framework for a unit step input is relies on denominator. In above condition at denominator the damping factor is missing for shaft zero undoing henceforth framework begins to sway. In this way pick controller with the end goal that at whatever point there is change in input, yield ought to tail it promptly. From Fig. 3.12 we can compose the condition,

$$VIN(t) + L\frac{dIin(t)}{dt} = Vr^*(t)$$

$$\therefore \frac{dIin(t)}{dt} = \frac{Vr^*(t) - VIN(t)}{L}$$

For the controller gain is required, using that gain G we can rewrite above equation as,

$$\therefore \frac{dIin(t)}{dt} = \frac{G.Vr^*(t) - VIN(t)}{L}$$

In general case where reference value change, the feedback behave like a first order lag. The difference equation is given as,

$$T\frac{di}{dt} + Iin(t) = \frac{Iin^*(t)}{Ki}$$

$$\therefore \frac{di}{dt} = \frac{1}{KiT}[Iin^*(t) - Iin(t)]$$

By equating above two equations we can write,

$$\frac{G.Vr^*(t) - VIN(t)}{L} = \frac{1}{KiT}[Iin^*(t) - Iin(t)]$$

Above equation can be simplified to find the reference average fundamental voltage Vr*(t) as,

$$\therefore Vr^*(t) = \frac{L}{KiTG}[Iin^*(t) - Iin(t)]$$

Where,
Ki = Current gain
G = Converter gain
T = First order time constant
Above equation can be represented in control block as shown in Fig. 12.

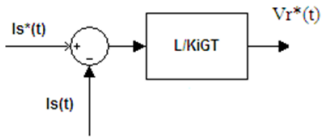


Fig. 12. The control block using PI controller to obtain Vr*

We need a steady framework from above condition and it is conceivable by picking suitable estimation of first request time consistent T. To think that it's first we draw the control circle which comprises of controller, converter and integrator as show in Fig.13.

Let us find the transfer function,

$$\frac{Iin(t)}{Iin^*(t)} = \frac{\frac{L}{KiGT} \times \frac{G}{1+sTr} \times \frac{1}{sL}}{1 + \left[\frac{L}{KiGT} \times \frac{G}{1+sTr} \times \frac{Ki}{sL}\right]}$$

By simplifying above equation,

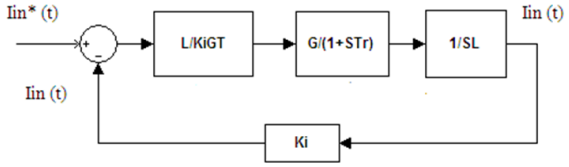


Fig. 13. The control loop using controller, converter and integrator

$$\frac{Iin(t)}{Iin^*(t)} = \frac{1/Ki}{1 + sT + s^2TTr}$$

Above condition shows that it has both first request advertisement second request time and it has a damping factor'ξ' subsequently framework will be progressively insecure. Pick the estimation of 'T' to such an extent that framework will give ideal reaction. Above condition ca be composed as,

$$\frac{Iin(t)}{Iin^*(t)} = \frac{1/KiTTr}{s^2 + \frac{1}{Tr}s + \frac{1}{TTr}}$$

This equation is similar to the second order response system and it is,

$$\frac{\omega n^2}{s^2 + 2\xi\omega n s + \omega n^2}$$

By comparing above two equations we can write,

$$\omega n^2 = \frac{1}{TTr}$$

$$2\xi\omega n = \frac{1}{Tr}$$

$$\therefore \xi = \frac{\sqrt{T}}{2\sqrt{Tr}}$$

For second order good response system,

$$\xi = 0.707 = \frac{1}{\sqrt{2}}$$

By putting this value in above equation the first order time constant 'T' for which system give optimum response is,

$$T = 2Tr$$

VI. VOLTAGE CONTROL DESIGN

As shown in above section actual input current Iin is obtained using controller and converter design. Also for the power balance we know,

Input power = output power

$$VINrms \times Iinrms = Vo \times Io$$

$$\therefore \frac{VINpeak}{\sqrt{2}} \times \frac{Iinpeak}{\sqrt{2}} = VoIo$$

In last section we find the control block for Iin value, it consider as an input to find the value of output current Io as shown in Fig. 14.

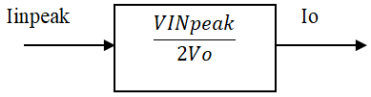


Fig. 14. Control block to find output current Io

The output current *Io* nourished to the comparator where second info is load current IL. For no adjustment in load *IL* = 0, subsequently yield current *Io* is legitimately given to the yield capacitor C. At that point the capacitor is gotten as appeared in Fig. 15.

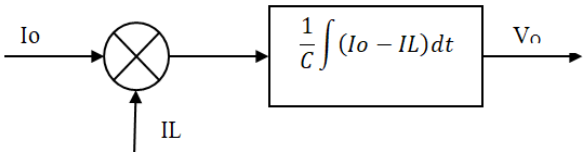


Fig. 15. Control block to find output voltage VO

The transfer function of current control loop as shown in equation number

$$\frac{Iin(t)}{Iin^*(t)} = \frac{1/Ki}{1 + sT + s^2TTr}$$

The above equation consists of square term s^2TTr referred as square of frequencies. Therefore the current loop acts very fast compare to the voltage control loop. To compensate this effect, for design of voltage control loop we approximate the current control loop as,

$$\frac{Iin(t)}{Iin^*(t)} = \frac{1/Ki}{1 + sT}$$

The final voltage control loop block diagram is shown in Fig. 16.

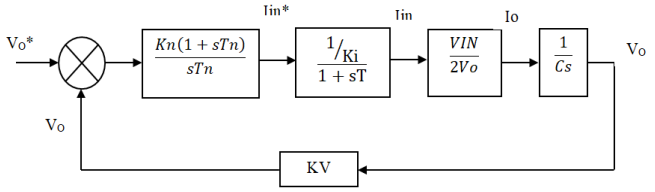


Fig. 16. block diagram voltage control loop

Here author choose PI controller for gooddynamicresponse. Here we assume load current IL = 0 and output current Io is directly given to the capacitor. The transfer function of above block is,

$$\frac{Vo}{Vo*} = \frac{G(s)}{1+G(s)H(s)}$$
$$= \frac{\frac{Kn(1+sTn)}{sTn} \times \frac{1/Ki}{1+sT} \times \frac{VINpeak}{2VosC}}{1+\left(\frac{Kn(1+sTn)}{sTn} \times \frac{1/Ki}{1+sT} \times \frac{VINpeak}{2VosC}\right) \times Kv}$$

For pole zero cancelation we pick Tn to such an extent that, it drop with the post for example Tn = T. After cancelation the denominator comprise of S2 term henceforth it has damping factor'ξ' which causes precariousness [6]. We need zero relentless state blunder and great powerful reaction with novel addition. For that it critical to pick estimations of Tn and Kn. The dynamic execution of a control framework is great if the controlled variable quickly arrives at the reference input. For any recurrence of information variety, the yield should follow the information variable quickly. The plot of modulus of close circle gain versus recurrence is appear in Fig. 17.

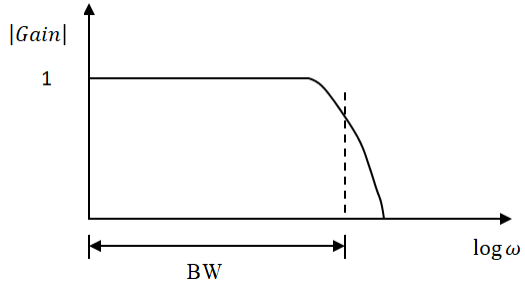


Fig. 17. Plot of modulus of close loop gain versus frequency

Optimization aims at bringing the gain as close as unity over a wide frequency range. Let us take second order canonical system transfer function,

$$F(j\omega) = \frac{b0}{a0 + j\omega a1 + (j\omega)^2 a2}$$

At low frequency range i.e. at starting, we assume b0 = a0

$$\therefore F(j\omega) = \frac{a0}{(a0 - a2\omega^2) + j\omega a1}$$

By multiplying numerator and denominator with complex conjugate of denominator and finding out modulus

$$\therefore F(j\omega) = \frac{a0 \times [(a0 - a2\omega^2) - j\omega a1]}{[a0 + j\omega a1 + (j\omega)^2 a2] \times [(a0 - a2\omega^2) - j\omega a1]}$$

By taking modulus of both side we will get,

$$\therefore |F(j\omega)| = \sqrt{\frac{a0}{a0^2 + \omega^2(a1^2 - 2a0a2) + \omega^4 a2^2}}$$

In order to increase the bandwidth to get optimum performance again we assume (a12 = 2a0a2)

$$\therefore |F(j\omega)|optimum = \sqrt{\frac{1}{1+\omega^4\left(a2/a0\right)^2}}$$

Now let us take third order system close loop transfer function

$$F(j\omega) = \frac{b0 + j\omega b1}{a0 + j\omega a1 + (j\omega)^2 a2 + (j\omega)^3 a3}$$

Again for low frequency range i.e. at starting, we assume b0 = a0 and b1 = a1

$$F(j\omega) = \frac{a0 + j\omega a1}{(a0 - \omega^2 a2) + j\omega(a1 - \omega^2 a3)}$$

By multiplying numerator and denominator with complex conjugate of denominator and finding out modulus

$$\therefore |F(j\omega)| = \sqrt{\frac{a0^2 + \omega^2 a1^2}{a0^2 + \omega^2(a1^2 - 2a0a2) + \omega^4(a2^2 - 2a1a3) + \omega^6 a3^2}}$$

For optimization again we use conditions that

$$a1^2 = 2a0a2$$
$$a2^2 = 2a1a3$$
$$\therefore |F(j\omega)| = \sqrt{\frac{1+\omega^2\left(a1/a0\right)^2}{1+\omega^2\left(a3/a0\right)^2}}$$

Now consider voltage control loop and its transfer function as discuss in above point,

$$\frac{Vo}{Vo*} = \frac{G(s)}{1+G(s)H(s)}$$
$$= \frac{\frac{Kn(1+sTn)}{sTn} \times \frac{1/Ki}{1+sT} \times \frac{VINpeak}{2VosC}}{1+\left(\frac{Kn(1+sTn)}{sTn} \times \frac{1/Ki}{1+sT} \times \frac{VINpeak}{2VosC}\right) \times Kv}$$

By simplifying it we will get,

$$\frac{Vo}{Vo*} = \frac{Kn(1+sTn) \times VINpeak}{Kis^2Tn2VoC(1+sT) + KnKvVINpeak(1+sTn)}$$

$$\therefore Vo/(Vo*) = (VINpeakTnKns + VINpeakKn)/(KnKvVINpeak + s(KnKvVINpeakTn) + s\^2 (KiTn2VoC) + s\^3 (KiTnT2VoC))$$

This is a third order system and compare with the generalized third order system we will get,

$$b1 = VINpeakTnKn$$

$$b0 = VINpeakKn$$

$$a0 = KnKvVINpeak$$

$$a1 = (KnKvVINpeakTn)$$

$$a2 = (KiTn2VoC)$$

$$a3 = (KiTnT2VoC)$$

Using the assumed conditions above, we can write,

$$(KnKvVINpeakTn)^2 = 2(KnKvVINpeak) \times (KiTn2VoC)$$

$$\therefore Kn = \frac{4KiVoC}{KvVINpeakTn}$$

Also,

$$(KiTn2VoC)^2 = 2(KnKvVINpeakTn) \times (KiTnT2VoC)$$

$$\therefore Kn = \frac{KiVoC}{KvVINpeakT}$$

From it we can find the value of Tn.
Basic definition and parameters, which characterize PWM methods, are summarized in Table II. The simulation

Table II. Basic parameters of system

Sr. No.	Parameter	Symbol	Value
1.	Line r.m.s. voltage	V_{IN}	$140V_{AC}$
2.	Boosted DC voltage	V_O	300 V_{DC}
3.	Switching frequency	*fs*	20KHz
4.	Line frequency	*f*	50Hz
5.	Rated DC power	Po	1KW
6.	Input peak voltage	V_{IN}peak	$\sqrt{2}$ V_{IN}rms = 160V
7.	Rated load current	Io	$\frac{po}{VDC} = 3.3Amp$
8.	Assume efficiency of system	η	90%
9.	Peak input current	Iinpeak	$\frac{Po}{VINpeak} = 6.26Amp$
10.	Line r.m.s. current	Iinrms	$\frac{Iinpeak}{\sqrt{2}} = 4.42Amp$
11.	Assumed modulation index	m	0.8
12.	Fundamental peak voltage	Vrpeak	m × VDC = 240V
13.	Fundamental r.m.s. voltage	$Vr_{(rms)}$	$\frac{Vrpeak}{\sqrt{2}} = 170V$
14.	Maximum duty cycle	D	$1 - \frac{VINmin \times \eta}{VDC} = 0.58$
15.	Triangular period	Tr	50µsec
16.	Controller gain	G	40

VII. RESULTS

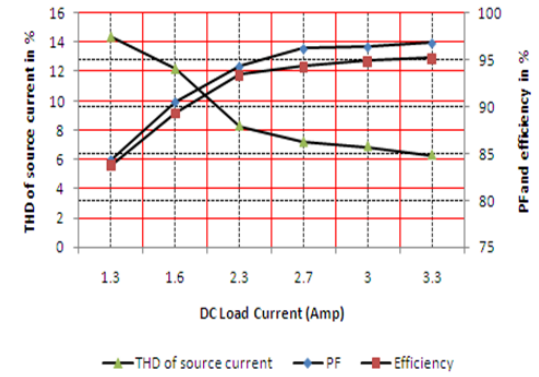
The performance examination of single stage bi-directional converter is made for different electrical loads going from 90Ω to 250Ω. The parameters examined during the investigation are power factor, efficiency, THD and DC load current. The detail examination of parameter esteems are appeared in table 3. The detail analysis is appeared in Fig. 18 a and 18 b. Fig. 6a demonstrates the diagram express to the assessed parameters for the CASE I. It is clearly seen that full load proficiency is 95.2% and power factor is 97.8%. The chart characterizes parameters for the CASE II is appeared in Fig. 6b. It is indicated that full load effectiveness is 78.4% and control factor is 80.3%.

Table III.Parameter Values For Detail Analysis of Single Phase Bi-Directional Converter
Case I- Rectification with CSPWM and Inversion with SPWM

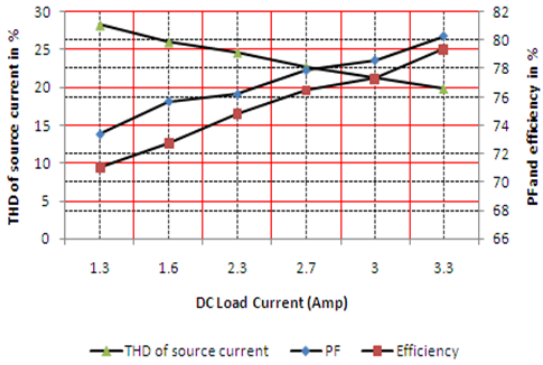
Load Resistance in (Ω)	DC load current (Amp.)	Power factor (%)	Efficiency (%)	THD (%)
225	1.3	84.3	83.7	14.4
180	1.6	90.5	89.3	12.2
130	2.3	94.3	93.4	8.3
110	2.7	96.2	94.3	7.2
100	3	96.4	94.9	6.9
90	3.3	97.8	95.2	6.3

Case II- Rectification with CSPWM and Inversion with SPWM

Load Resistance in (Ω)	DC load current (Amp.)	Power factor (%)	Efficiency (%)	THD (%)
225	1.3	73.4	70	28.3
180	1.6	75.7	71.7	26
130	2.3	76.2	73.8	24.6
110	2.7	77.9	77.5	22.7
100	3	78.6	74.3	21.3
90	3.3	80.3	75.4	19.8



(a)



(b)

Fig. 18. (a) **Variation in power factor, efficiency and THD with change in load and DC load current for case** I-rectification with CSPWM and inversion with SPWM. (b) Variation in power factor, efficiency and THD with change in load and DC load current for case II-rectification and inversion both with SPWM.

Fig. 19. Experimental Set-Up Of Laboratory Model

VIII. CONCLUSIONS

This paper focused on the modeling of switches, modeling of IGBT driver, modeling of controller. The designing of input inductor, output DC link capacitor and PWM converter are discussed. Also it highlights different control blocks used in simulation and explain the mechanism of DC link voltage regulation. The parameters are calculated using modeling and design which are used to build the control block in simulation and circuit diagram in laboratory implementation.

REFERENCES

1. Rahul GanpatMapari, DG Wakde, "A simple predictive Pwm voltage controlled technique for implementation of single phase inverter with precesion rectifier", Journal of Engineering Research and Applications, VOL. 03, pp. 1772-1775, 2013.
2. J.A.Domínguez-Navarro, R. Dufo-López, J.M. Yusta-Loyo, J.S. Artal-Sevil, J.L. Bernal-Agustín, "Design of an electric vehicle fast-charging station with integration of renewable energy and storage systems", International Journal of Electrical Power & Energy Systems, vol. 105, pp. 46-58, 2019.
3. Rahul GanpatMapari, DG Wakde, "A Simple Control Strategy Technique for a Single-phase Bridgeless Active Rectifier with High Power Factor and Voltage Stabilization Using Partial Digital Implementation", *Artificial Intelligence and Evolutionary Algorithms in Engineering Systems*, Springer, New Delhi, pp. 17-26, 2015
4. Rahul GanpatMapari, DG Wakde, "Modeling, simulation and implementation of the single-phase unity power factor active rectifier for minimizing the input current harmonic distortions", *International Conference on Circuits, Power and Computing Technologies (ICCPCT)*, IEEE, pp. 265-268, 2013.
5. Rahul G Mapari, SA Patil, DB Talage, DG Wakade, Gear shifting using Retrofit Automatic Manual Transmission technique in Wind Energy Conversion System, *3rd International Symposium & Exhibition in Sustainable Energy & Environment (ISESEE)*, IEEE, pp. 33-35, 2011.
6. R Mapari, R Parbat, "Analysis of Single Phase Bi-Directional Converter for Improvements in Power Factor and Reduction in Harmonic Distortions", International Journal of Applied Engineering Research Vol.14, Iuuse16, pp. 3566-3572, 2019.

AUTHORS PROFILE

Dr. Rahul G. Maparireceived the bachelor & master degree in electronics engineering from SavitribaiPhule Pune University, India, in 2004 & 2007 respectively, and the Ph.D. degree in Electronics & Telecommunication engineering from Amravati University, India in 2016.
From 2005 to 2017, he worked at SavitribaiPhule Pune University involved in teaching and research in power converters. Since 2017, he has been with Department of Electronics & Telecommunication Engineering of PimpriChinchwad College of Engineering & Research (PCCOE&R), and is currently working as Professor and Head of the department. His research interests are power converters and switching techniques. Dr. Mapari is a member of Institute of Engineers and IEEE

Dr. D.G. Bhalkehas received the bachelor degree in E&TC engineering from Dr. B.A.M.U. Aurangabad, & master degree in Electronics engineering from Shivaji University, Kolhapur in 1998 & 2005 respectively, and the Ph.D. degree in Electronics & Communication engineering from National Institute of technology, Warangal, India in 2016.
He is having 21 years of teaching experience at SavitribaiPhule Pune University, Pune and his research areas are speech and audio processing. Since 2017, he has been with Department of Electronics & Telecommunication Engineering of AISSMS College of Engineering Pune and is currently working as Professor and Head of the department. Dr. Bhalke is a Fellow member of Institute of Engineers and member of IETE, ISTE.

Mr. Rahul S. Parbatreceived the bachelor degree in Electronics and Telecommunication Engineering in 2010 and master degree in Microwave Engineering in 2015 from SavitribaiPhule Pune University, India, respectively.
From 2013 to 2019, he worked at SavitribaiPhule Pune University Since 2018, he has been with Department of Electronics & Telecommunication Engineering of PimpriChinchwad College of Engineering & Research (PCCOE&R), and is currently working as Assistant Professor. His research interests are power converters and optimization of battery charger time of electric vehicles.