

# Power Quality Improvement in DG System using BOA based Interlined Unified Power Quality Conditioner



M. Anitha, T.R. Jyothsna

**Abstract:** To improve the power quality of multi-feeder distribution system, this paper proposes a concept of Interline Power Flow Controller (IUPQC). IUPQC is a structure of two filters such as, series and shunt filters. The causes for poor power quality of system is due to harmonics, power factor variations and changes in system voltage. The purpose of these converters is to mitigate the PQ issues. The reference signals required for series and shunt converters of iUPQC system is generated with the help of conventional controllers and PWM controllers. The PLL used to match the phase sequence of converters. For obtaining better improvement in Power Quality this paper is implemented with one of the optimization technique such as Bull Optimization Technique (BOA). The purpose of BOA is used to control the DC Link Voltage of iUPQC. With the help of this BOA technique, the variations in voltage and current are reduced to enhance the power quality. The effectiveness of this proposed system with BOA technique is tested and verified using Matlab/Simulink environment.

**Key words:** Interline Unified Power Quality Conditioner (IUPQC), Bull optimization algorithm (BOA), Phase angle control (PAC), Firefly Algorithm (FA), Ant lion Optimization Algorithm (ALO).

## I. INTRODUCTION

The latest power distribution system is fetching very susceptible to the various PQ (Power-Quality) problems [1]. PQ in distribution systems is a focal concern for industrial, commercial and residential purposes. Increased affair above this matter has run to quantifying PQ variations, reviewing the features of power disturbances and specifying solutions to these power quality problems. PQ is mostly exaggerated by the increased usage of non-linear loads such as powered electronic equipment, variable speed drives, and electronic control gears. Indigent power quality can disturb the security, reliability, and efficiency of several categories of equipment. Many parts of PQ are harmonics; flicker and imbalance have turn out to be stern concerns. Furthermore, lightning strikes on transmission lines, switching of capacitor banks and several network faults can too instigate PQ problems [2].

In consequence of the growth of powered electronic devices such as Flexible AC Transmission System (FACTS) and custom power devices, deregulated power systems with multipurpose new-fangled control abilities have performed. Reasonably slight concentration, however, has been fervent to system sag enhancement [3]. It is recognised that FACTS-based devices, viz., SVC, STATCOM, and DVR can deliver an effectual solution to voltage sag difficulties. Therefore, a recent distribution system needs a better steadiness of voltage being provided and the current drawn which is an elemental viewpoint to the end user. One latest and the very assuring solution is UPQC (Unified Power-Quality Conditioner). UPQC is a custom power device that contains shunt and series converters linked back to back on the dc side and distributes with load current and supply-voltage insufficiencies. The shunt inverter delivers reactive power and harmonic rewards by injecting a shunt current to the load. The series inverter is used in the compensation of voltage related problems, for example, sag and fabulous in source voltage by interleaving a controllable series voltage.

Conveniently, UPQC has been ultimate solution to progress the PQ in the electrical distribution system. The control method is not suitable for UPQC system for the motive that the dc sources are exchanged by capacitors in the UPQC system [4]. Accordingly, there is a requirement to consider several PQ mitigation procedures to convalesce the quality of power supplied. This shortage can be overwhelmed by unique intelligent optimization algorithms known as heuristic approaches are executed to solve PQ distributions. Some sounds regarded optimization systems are Evolutionary Programming (EP), Genetic Algorithm (GA), Simulated Annealing (SA), Differential Evolution (DE), Particle Swarm Optimization (PSO) and Artificial Bee Colony (ABC), etc. The improvement of UPQC PQ problem in a viable environment includes in the minimization of power losses [5].

## II. PROPOSED METHODOLOGY

The structure of Interline power flow controller is shown in figure 1. It consists of two back to back converters with a common dc link capacitor. These two converters are connected to two feeders of distribution system for maintain system conditions. In this case we consider two feeder system. The shunt vsc converter of system is connected to feeder-1 and series vsc converter is connected to feeder-2.

Revised Manuscript Received on December 30, 2019.

\* Correspondence Author

**M.Anitha** (Mallipeddi Anitha), Assistant Professor, Faculty of Electrical and Electronics Engineering, RVR & JCCE, Chowdavaram, Guntur.

**Dr.T.R.Jyothsna** (Tummala Radha Krishnan Jyothsna), Professor, Department of Electrical and Electronics Engineering, Andhra University, Visakhapatnam, India

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>)

# Power Quality Improvement in DG System using BOA based Interlined Unified Power Quality Conditioner

There is a boosting transformer is connected between series converter and transmission system to maintain the voltage levels. IUPQC can act as a (a) smart circuit breaker, (b) also acts as power flow controller between grid and microgrid to repay the active and reactive power references of the series converter [6].

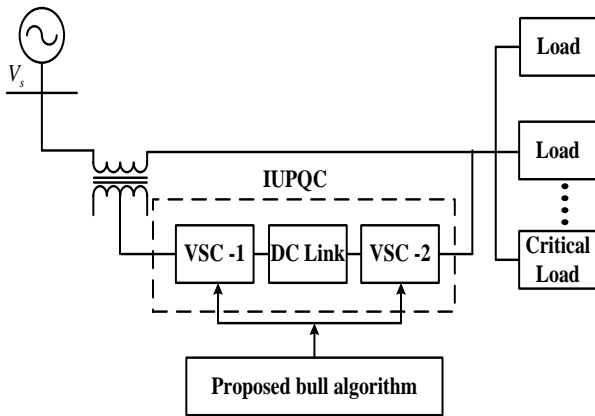


Figure 1: Structure of the proposed method

In the proposed method, the IUPQC is used to compensate the PQ issues with the help of the bull algorithm. The power sharing between the sources to the load is by achieves through maintain the dc link voltage. Initially, the normal voltage and current characteristics are analyzed, and then the PQ issues are created using the non-linear load, unbalanced load or critical load. The PQ issues are mitigated in the use of IUPQC device and bull algorithm is assist to the mitigation process via power sharing, dc link voltage regulation. The connected structure of IUPQC with distribution system is shown in figure 2.

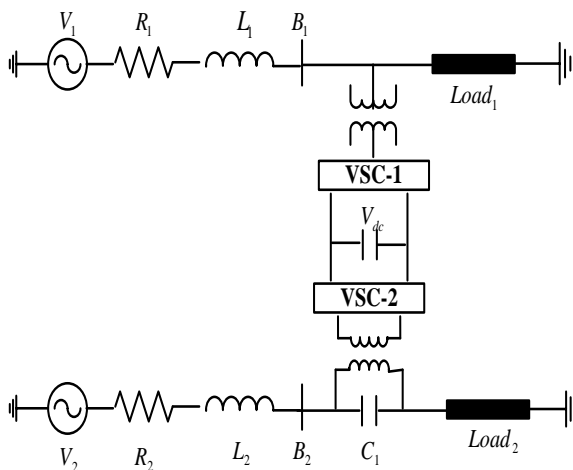


Figure 2: IUPQC structure in the distribution system

Incidentally, the IUPQC exemplify a traditional power device that is effusively in employment in the distribution scheme to restrict the conflict that has an actual impact on the efficiency in function of the non-linear or critical load. Dependably, the IUPQC concealments the sequences active power filter (APF) over and above the shunt APF. The sequence APF effectual provides the compensation amongst the distribution scheme and the sub-transmission scheme affecting to the harmonics [7]. Into the

bargain, the BOA algorithm assistance the regulation of voltage from the DC link capacitor. The power that the shunt section distributes or suck up, relaxes on the power conditions of the sequences compensator and the power mandatory to strip the losses. The detailed control process of the PAC control, series and shunt control techniques are described in the following sections.

## III. IUPQC CONTROL TECHNIQUES

### A. Phase Angle Controller:

The aim of the series inverter is to maintain the load voltage at desired limit. And also, it maintains the reactive power demanded by load is at constant. With the help of power angle, the series converter maintain the reactive power at fixed value under any circumstances i.e voltage variations or load changes. The phase angle is calculated based on the source voltage and load voltage. The phase angle is changed for reactive power control in the system [8]. The phase angle changed through the reactive power, the disturbances are compensated via the filters. The phase angle control phaser diagram is illustrated in figure3.

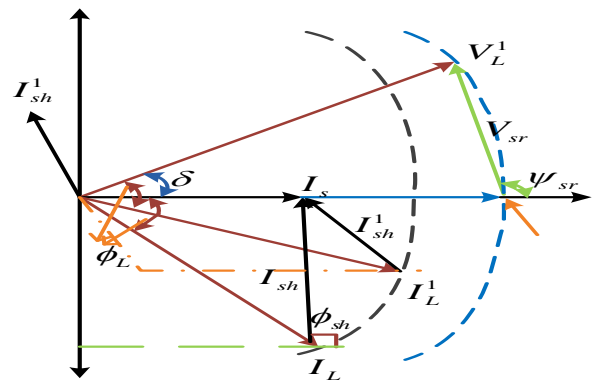


Figure 3: Phasor diagram of the PAC control scheme

### B. Control Diagram of the Series APF controller

The gate pulses required for series VSC is obtained by general PWM controller. And the reference voltage signals are obtained by controlling of dc bus and line voltage parameters. The magnitude required for reference signal is obtained with dc link voltage controller and required phase angle is to get with phase angle controller. The control diagram for series converter is shown in figure 4.

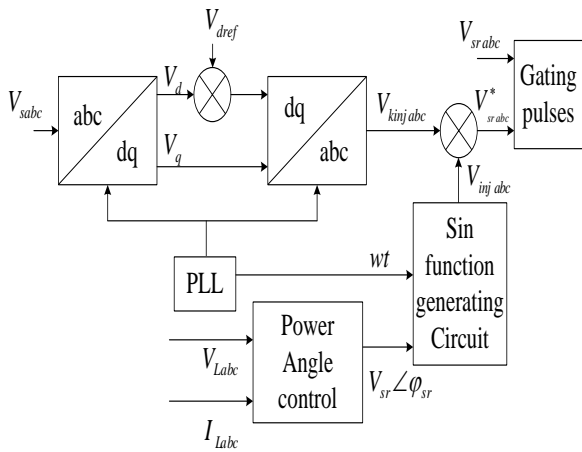


Figure 4: control structure of the series inverter

In this APF controller, the source voltage is transformed into dq-axis and that component is compared with reference direct voltage. Again, this error component converted to 3-phase components. The combined value of error component and phase angle control value is applied to PWM controller for generating gate signals required for VSC.

C. Controlling of the Shunt APF controller

Here, PQ-theory method is used to generate reference current signals required for shunt apf controller. In this case, the actual load voltage and currents are converted into αβ-coordinates. Form these coordinates, the active and reactive powers are to be calculated. These reference powers are compared with rated power and then converted to reference currents with the help of conventional PI controllers [9]. And Inverse Park’s transformation is used for getting general abc components and applied to PWM controller to get gate signals.

The expressions for calculating powers using currents are shown below.

$$p = v_{\alpha} \cdot i_{\alpha} + v_{\beta} \cdot i_{\beta} = \bar{p} + \tilde{p}$$

$$q = v_{\beta} \cdot i_{\alpha} - v_{\alpha} \cdot i_{\beta} = \bar{q} + \tilde{q}$$

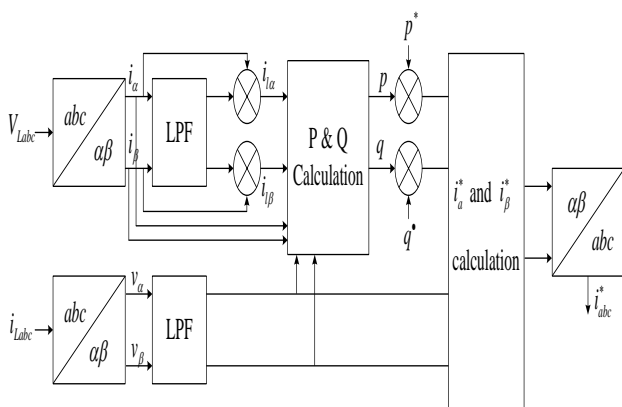


Figure 5: control structure of the shunt inverter

IV. BULL OPTIMIZATION ALGORITHM

The boa algorithm is utilized to hold the dc link voltage as a steady. The reference dc link voltage and regular dc link voltage is fed the enter of the set of rules. The error voltage or voltage difference of the dc hyperlink voltage is decreased and maintained inside the constant manner. Basically, the boa is the evolutionary algorithm. It is utilized the genetic operators, crossover and mutation. The proposed algorithm makes use of effective capabilities of the ga. One of the essential hazards of the ga is that it does now not use the great individual to provide a brand new technology. But, the satisfactory man or woman is actively used in the proposed set of rules. All individuals produced attempt to get better people via taking a certain part of the great man or woman. The choice algorithm that is the basic principle of the ga selects the first-rate people to be transferred into the new era. The individuals created on the initial stage live on by being mutated either until the fine end result is discovered or a sure iteration variety is reached [10]. The grade by grade method of the boa set of rules is given underneath.

Step1: Initialization

Step2: Fitness

Step3: Crossover

Step4: Mutation

Step5: Settings and benchmark functions

A. Initialization

Initialize the population, i.e choose, the values of dc link voltage and reference voltages are initial commands with a limit of number N and Dimension D. The expression for initial population is shown below.

$$X_{ab} = X_b^{\max} - R * (X_b^{\max} - X_a^{\min}) \quad (4)$$

B. Fitness

The fitness is allocated based on the optimization problem. The dc link voltage is maintained equal to the reference voltage. It is denoted by the equation,

$$V_{dc}^* = V_{dc} \quad (5)$$

The dc link voltage is maintained by calculating the error voltage between, dc link voltage to reference dc link voltage are minimized. By the way of the dc link voltage control is achieved in the IUPQC device.



# Power Quality Improvement in DG System using BOA based Interlined Unified Power Quality Conditioner

## C. Crossover

Individual's technique the current quality solution received to date with the help of the manner of crossover. A two-factor crossover operation is used within the proposed set of rules. Random numbers named as r1 and r2 are generated for an individual with d dimensions of the dc link voltages. The variety of random variety is inside [0, d].

If the random number  $R_1$  is larger than  $R_2$ , then genes that belong to a certain individual are replaced with those of the best individual in  $[R_1, R_2]$ . Otherwise, genes that belong to a certain individual are replaced with those of the best individual in  $[R_2, R_1]$ . If crossing points are close to each other in the crossover operation, then the individual performs more exploration. Otherwise, the individual performs more exploitation [11].

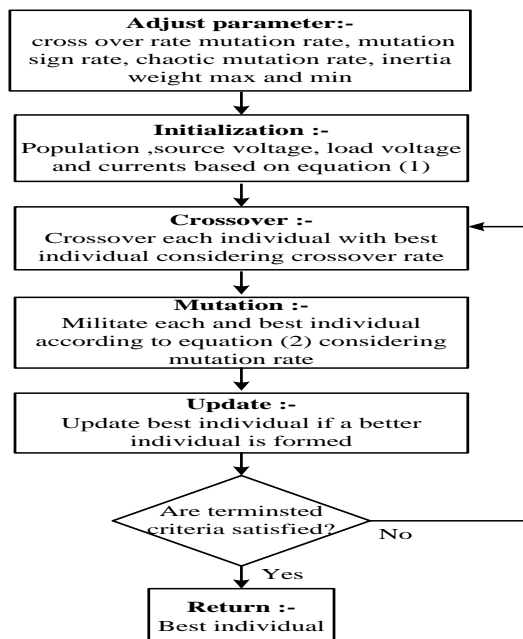
## D. Mutation

The purpose is to find better people via doing research around the values of the gene inside the proposed algorithm. For the answer to transport forward fast and efficiently and to cast off nearby minima, the mutation system must play an energetic function. A gene of every character is mutated according to the mutation price. The mutation system is accomplished by way of using equation (6)

$$M_{ab} = \begin{cases} X_{ab} + W * R_1 * X_{ab}, & R_2 \leq 0.5 \\ X_{ab} + W * R_1 * X_{ab}, & O.W \end{cases} \quad (6)$$

## E. Settings and benchmark functions

Take a look at the performance of the boa algorithm, the benchmark take a look at capabilities are applied. These functions include unimodal, multimodal, separable, non-separable, normal, and irregular check functions. This benchmark features set could be very massive, and those capabilities have different characteristics utilized in continuous problems. The usage of the benchmark features, the boa algorithm overall performance is evaluated based on [11].



## Figure 6: Flow chart of the BOA algorithm

Based on the flow chart, the process of the bull algorithm is maintaining the dc link voltage in the IUPQC. The input is the dc link voltage and it is compared reference dc link voltage, the error value is minimized with the utilization of the BOA algorithm. By the way, the dc link voltage is maintained in the control system. The PQ issues are compensated in the utilization of the BOA with IUPQC device. The proposed controller results are analyzed and illustrated in the following section.

## V. RESULTS AND DISCUSSIONS

The proposed method can be executed in MATLAB/Simulink working platform. At this point, the proposed method is actually based on IUPQC which is assisting the control for generating reference signals of the system. With this proposed method, voltage sag and swell problems tend to be compensating the sag appearance all the way through PAC control signals in distribution systems. Afterwards the controlled signals are produced from the proposed method that pulses can compensate the PQ issues in the utilization of the IUPQC. For that reason, the proposed method is also employed to enhance the performance of IUPQC not counting compensate the voltage sag and swell issues. The proposed method is experimented and its performance analysed. The Simulink model of the proposed system is illustrated in the figure 7. The performance analysis of the planned method is computed and explained in the following section.

### A. Performance Analysis

Figure 8 presents the normal behaviour of the distribution system current and voltage in the feeders 1 and 2. The PQ of the system along with non-linear load is enhanced because of the help of a proposed control technique based IUPQC.

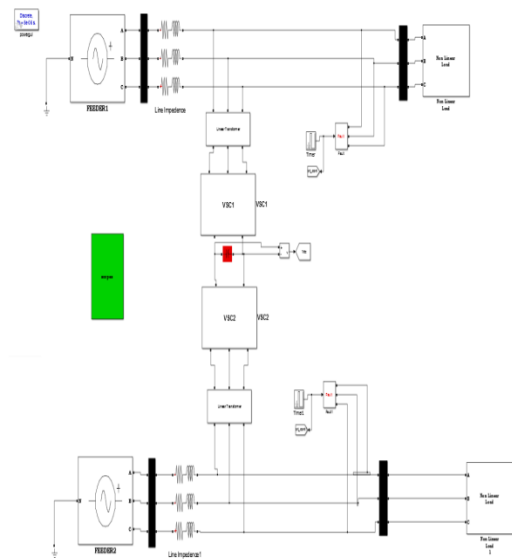


Figure 7: Simulink diagram of the IUPQC with proposed controller

**Table 1: Implementation parameters of (a) System and (b) Algorithm**

Description of parameters		Values
Source Voltage		230 V
Source current		20.2 A
Nominal frequency		50 Hz
Dc- link voltage		420 V
Dc-link capacitor		200 $\mu F$
Shunt filter	R,L	5 m $\Omega$ ,150 $\mu H$
Series filter	R	0.0004 H
Load voltage		230 V
Load current		20.5 A

(a)

Description of parameters	Algorithms	Values
No of search agents	BOA	2
Mutation(w)		0.5
Iteration No		1
No of search agents	FA	2
Upper bound		100
Lower bound		0.1
Dimension		3
Max iteration		5
No of search agents	ALO	2
Upper bound		1000
Lower bound		1
Dimension		3

(b)

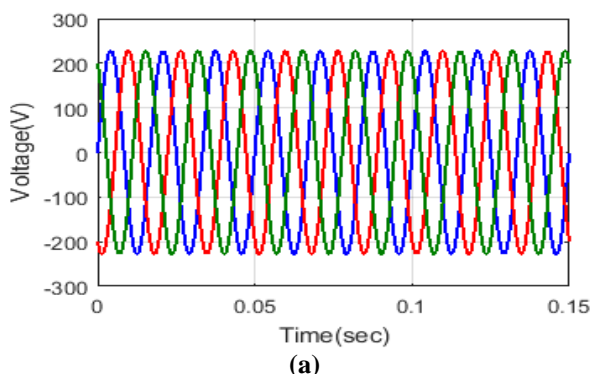
The performances of the proposed technique are estimated during the voltage sag and swell conditions analysed their results in three cases which are explained as follows. The investigated outputs of the proposed technique are contrasted with FA based IUPQC controller and ALO based IUPQC controller.

**Case A:** Swell at feeders 1 and 2

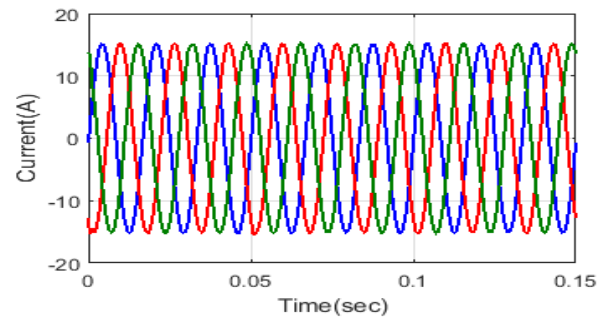
**Case B:** Sag at feeders 1 and 2

**Case C:** Sag at feeder 1 and swell at feeders 2

The investigated outputs of the proposed method are analysed with IUPQC controller. The normal behaviour of the source side voltage and current is illustrated. The voltage level is 230V and the current is 15A. Then the disturbances are created in the way giving the unbalance load, non-linear load or critical load. Here, using the non-linear or unbalanced load for created the disturbance in the system.



(a)



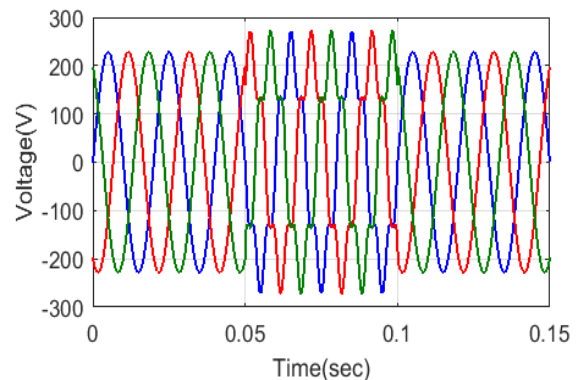
(b)

**Figure 8: Analysis of the Source side (a) voltage and (b) current**

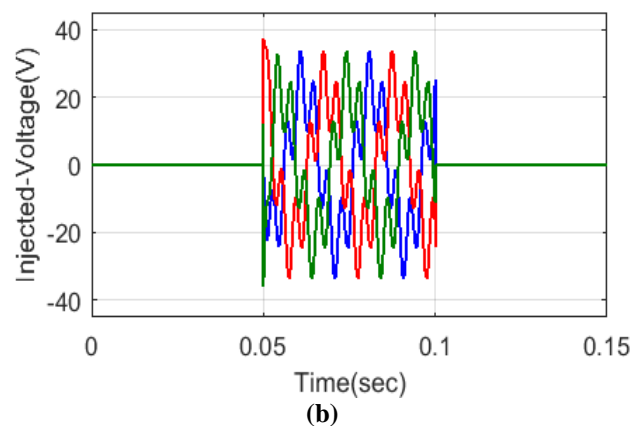
The source side voltage and current is smooth variation at the time of the smooth load. When provide the non-linear load or unbalanced load in the load side, the current and voltage is disturbed because of the PQ issues such as sag, swell, distortion etc. These disturbances are compensated with the utilization of the IUPQC with bull algorithm. The IUPQC is connected in the distribution system with the two feeders (feeder1 and feeder 2) for compensation. At first case 1, the sag is introduced in the feeder 1 and feeder 2. During the sag condition, the fault signals and compensated signals are analysed in the following section.

**Case A: Swell at feeders 1 and 2**

The swell is initiated in the system use of the non-linear load, unbalanced load or critical load in the load side. The voltage swell signal is shown in Figure 9. The mitigation is achieved through the use of proposed controller.

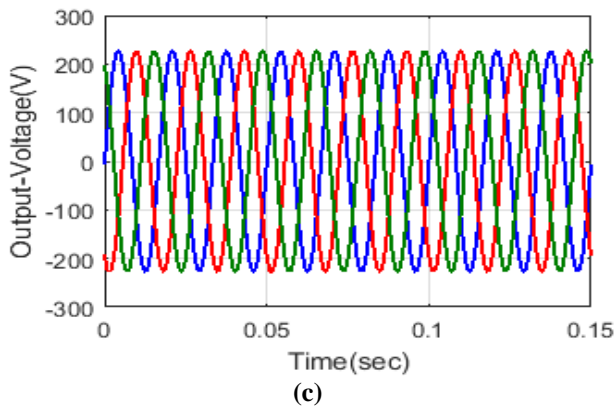


(a)



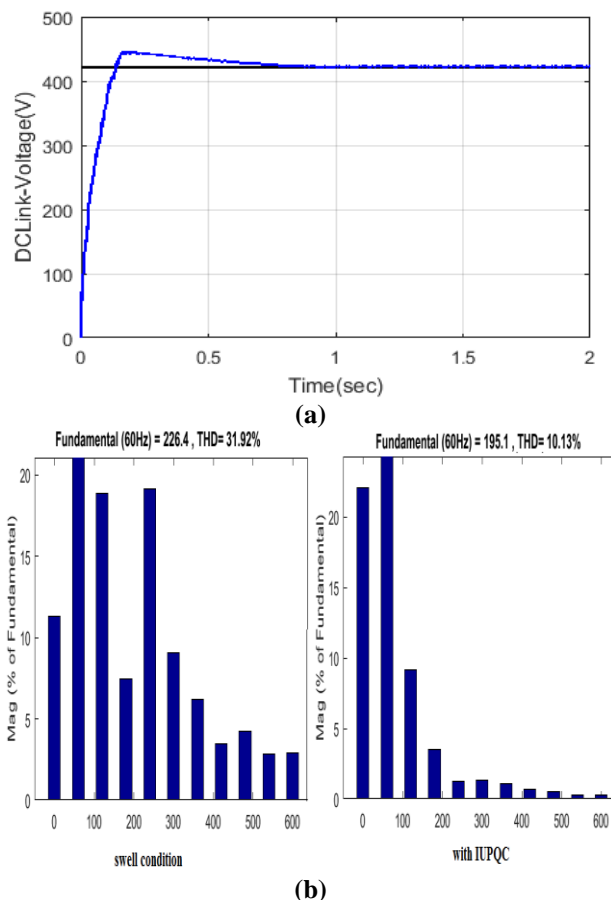
(b)

# Power Quality Improvement in DG System using BOA based Interlined Unified Power Quality Conditioner



**Figure 9: Analysis of the (a) Voltage swell, (b) Injected voltage and (c) Output voltage**

The figure 8(a) illustrates the normal voltage of the system. The normal voltage of the system is 230V. Figure 9(a) illustrates the disturbance voltage. Initially, 230V is maintained in the constant level to at 0-0.05s, then it is increased the voltage to 30V (i.e. 260V) at 0.05s-0.1s due to the load variation. The increased voltage is compensated with the help of the IUPQC device through the series filter. The injected voltage from the series filter is 30V, it is compensated the voltage swell and the excess voltage is stored in the capacitor of the IUPQC is presented figure 9(b). The compensated output is illustrated in the figure 9(c). Then the proposed BOA algorithm is utilized to maintain the dc link voltage as a constant level. The variation of the dc link voltage is illustrated in the figure 10.

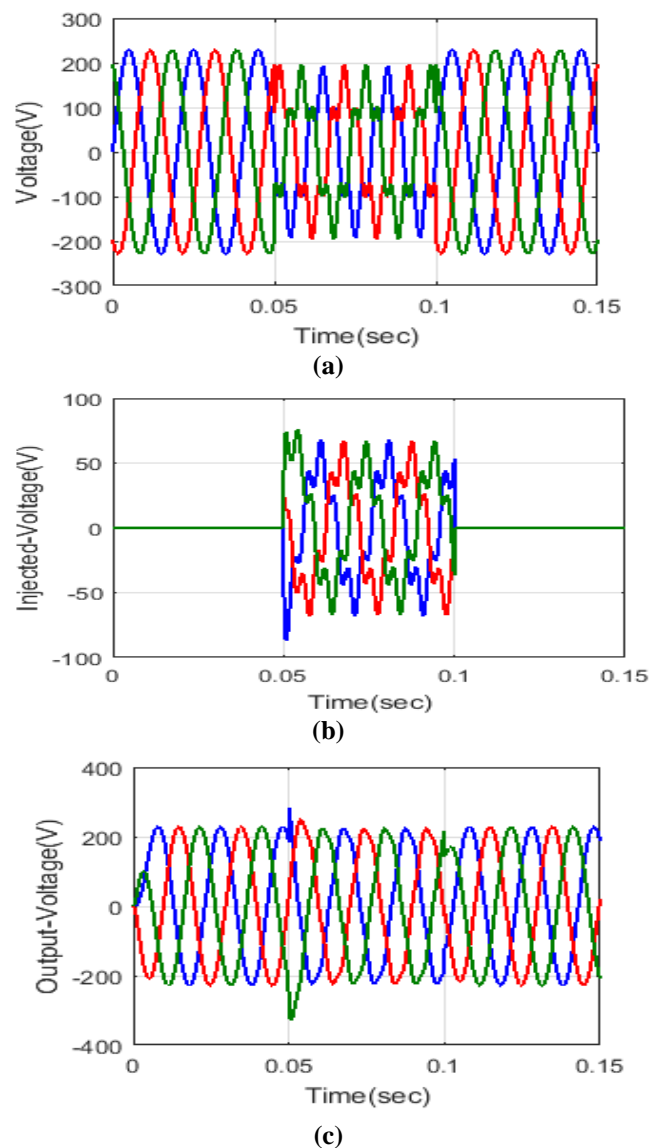


**Figure 10: Analysis of the (a) dc link voltage and (b) THD ratio**

Here, the dc link voltage level is 420V; the voltage is variation due to the disturbance. The voltage is maintained as constant it is illustrated in the figure 10(a). THD ratio is analyzed in the proposed method is illustrated in the figure 10(b). During swell condition the THD ratio is 31.92%, it is minimized with the IUPQC to 10.13%.

## Case B: Sag at feeders 1 and 2

The second case is the voltage sag condition in feeder 1 and feeder 2. Normally, the sag is defined as a decrease the voltage level 10% to 90% within the period of the half or full cycle. The IUPQC device is compensated the voltage via PAC control. In figure 8 (a) is describes the normal source voltage of the system. The voltage is 230V and its move on stable when the disturbance is occurred in the signal, the voltage is disturbed. Here, the disturbance is created with the help of the nonlinear load; critical load or unbalanced load in the load side for testing the performance of the IUPQC if it is mitigate the PQ issues. The voltage sag is presented in the figure 11(b).



**Figure11: Analysis of the (a) Voltage sag, (b) Injected voltage and (c) Output voltage**

The voltage sag is compensated through the IUPQC device. The series and shunt filters are used to provide voltage and current to compensate the sag condition. The voltage sag signal gives the information about the level of the voltage is decreased from the source voltage. The voltage is decreased to 180V from the 230V of the normal voltage. Then the voltage is compensated through the injected voltage from the series filter of IUPQC. The filter is injected the voltage level is 50V-60V for compensation it is illustrated in the figure 11(c). When the voltage sag is compensated, the performance of the system is improved. The regulation of DC link voltage is one of the tasks in the system, since the injecting voltage depends on the regulated voltage of DC link capacitor. The proposed BOA algorithm regulates the DC link voltage and reduces the harmonics in the inverter.

So, IUPQC dc link voltage control is a main issue, the dc link voltage is maintained the constant level through the proposed controller of the BOA algorithm. The figure 12(a) shows the dc link voltage. It is observed that due to the effect of sag, the variation of the dc link voltage is maintained with the use of the BOA algorithm.

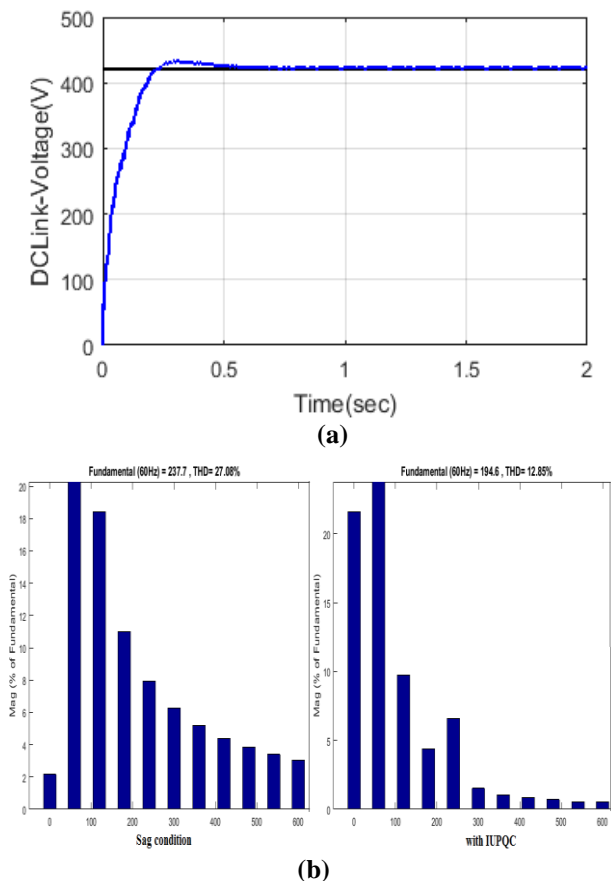


Figure 12: Analysis of the (a) dc link voltage and (b) THD ratio

The THD ratio is analyzed for the performance testing of the proposed controller. Before connected IUPQC, the THD ratio is 27.08% and it reduced to 12.85% after connected with IUPQC device. The IUPQC device also decreases the harmonics in the signals.

**Case C: Sag at feeder 1 and swell at feeders 2**

In this case, the sag is analyzed in the feeder 1 and the swell is analyzed in the feeder 2. The performance signals are illustrated in the figure 13. The sag and swell is an important PQ issues in the systems. It affected the system

and reduces the performance of the system. So, need to compensate the PQ issues of voltage sag and swell. The proposed controller IUPQC with BOA is used for balanced the PQ issues in the system. The sag and swell is introduced by the way of the non-linear load. Then the sag is present in the feeder 1 at 0.05-0.1s and swell is present in the feeder 2 at 0.05-0.1s. The series filter is injected the voltage from IUPQC for compensate the PQ issues. At feeder 1 the normal voltage is 230V and it is reduced to 170V or 160V because of the various loads. The injected voltage is 60V; it is compensate the sag in the feeder 1. The series filter is injected the voltage from IUPQC for compensate the PQ issues. At feeder 2 the normal voltage is 230V and it is increased to 280V or 270V because of the various loads. The injected voltage is 40V; it is compensate the swell in the feeder 2.

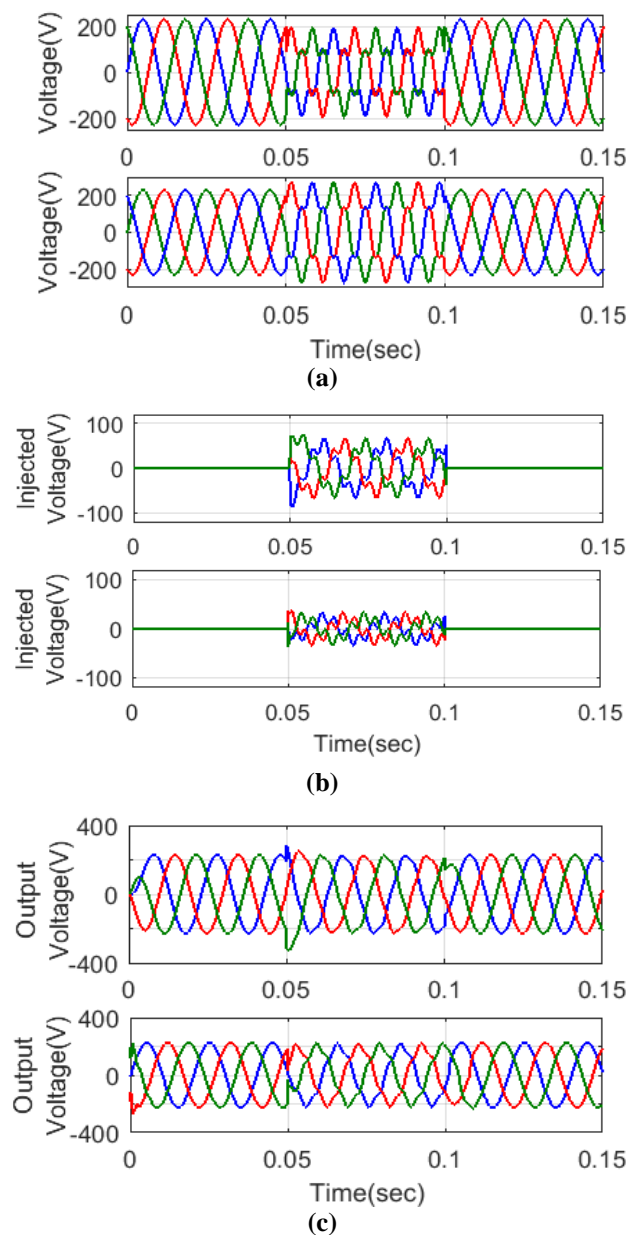
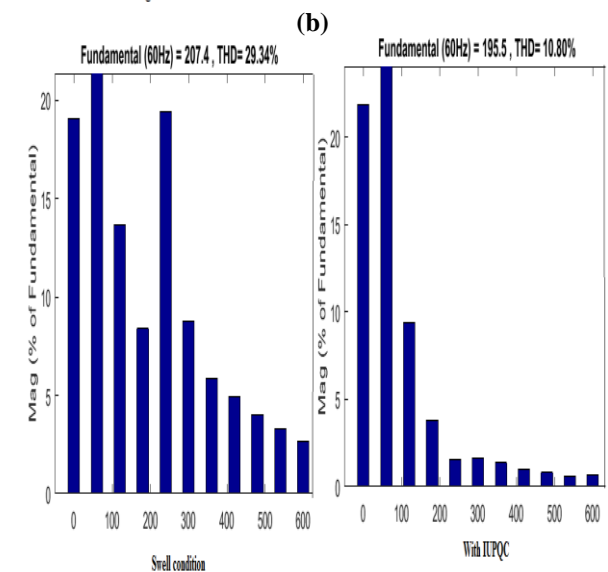
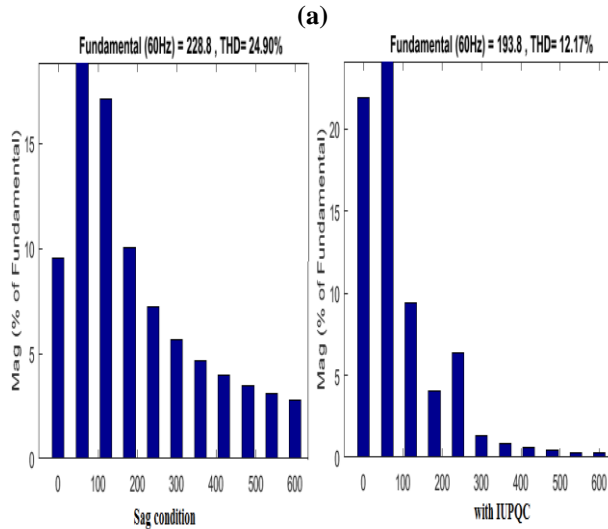
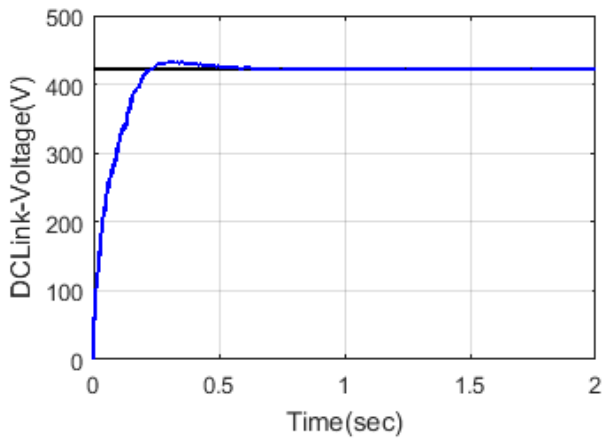


Figure 13: Analysis of the (a) Voltage sag and voltage swell (b) Injected voltages and (c) Output voltage



# Power Quality Improvement in DG System using BOA based Interlined Unified Power Quality Conditioner



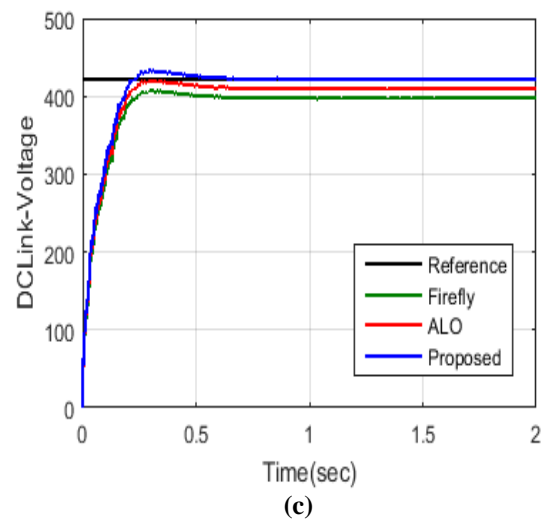
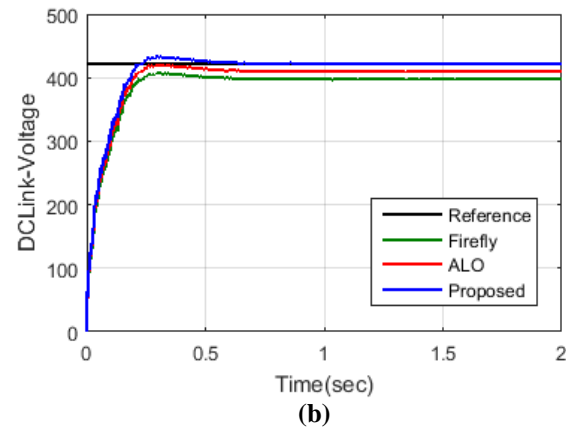
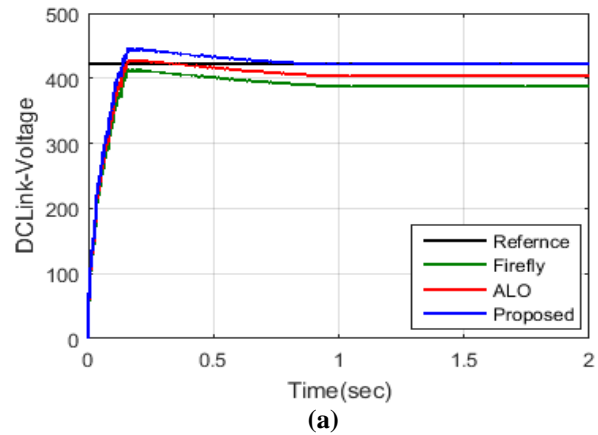
**Figure 14: Analysis of the (a) dc link voltage, (b) THD ratio for feeder 1 and (c) THD ratio for feeder 2**

By the utilization of the proposed method the objective function is achieved in the system. The compensated or output voltage is presented in the figure 13(c). The dc link voltage control is presented in figure 14(a). The reference dc link voltage is 420V, then it is maintained in the way of utilize the BOA algorithm. The reactive power of the feeder 1 and feeder 2 is illustrated in the figure 14(b). The reactive power is improve power factor of the system. At feeder 1 before IUPQC the THD ratio is

24.90V, then it is reduced to 12.17% because of the IUPQC connection. At feeder 2 before IUPQC the THD ratio is 29.34V, then it is reduced to 10.80% because of the IUPQC connection

### Comparison analysis

In the sub section, the comparison analysis is done for the above three cases. The comparison is done with the existing control techniques of the ALO and FA algorithms. The dc link voltage and generated power are compared with the existing method. This analysis is used to know about the performance of the proposed method.

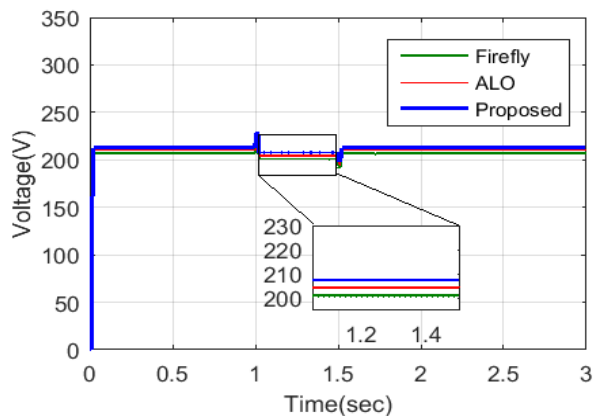


**Figure 15: Comparison analysis of Dc-link voltage (a) Case 1, (b) Case 2 and (c) Case 3**



The proposed method effectiveness is calculated based on the settling time to reach the reference value. Based on the figure 15(a), the proposed technique settling time is  $t=0.7-0.8$  sec at 420V. The FA method settling time is  $t=0.5-0.7$  sec at 390V. The ALO method rise time is  $t=0.8-1.0$  sec at 370V has been performed.

The dc link voltage analysis is compared with two existing algorithms of FA and ALO. In comparison of the proposed algorithm have a higher efficiency; it is proving the pictorial representation. In figure 15 (b) the proposed technique settling time is  $t=0.6$  sec at 420V. The FA method settling time is  $t=0.5$  sec at 390V. The ALO method settling time is  $t=0.6$  sec at 380V has been performed. In figure 15 (c) the proposed technique settling time is  $t=0.5$  sec at 420V. The FA method settling time is  $t=0.6$  sec at 390V. The ALO method settling time is  $t=0.6$  sec at 380V has been performed. The dc link voltage is 420V, the proposed method only meet the level of voltage and maintain at constant but the existing methods are not meet the constant value of the dc link voltage. Based on the voltage level, the proposed method is having high efficiency with comparing existing methods.



**Figure 16: Comparison analysis of case 1**

The sag condition comparison analysis is illustrated in figure 16. Here, the graph is zoomed in the particular portion of analysis the efficiency of the proposed controller. The sag mitigation process, the proposed method rise time is 1s at the voltage level is 210v and its stable in 210v at 1.5s. The FA method rise time is 1s at the voltage level is 205v and its stable in 205v at 1.5s. In same, ALO rise time is 200v and its stable in 200v at 1.5s. Based on the analysis of the rise time and voltage level, the proposed method has a high efficiency comparing with the other existing method.

## VI. CONCLUSION

This paper has proposed the PQ improvement with the help of IUPQC, which has employed BOA based controller. The proposed controller is executed in the MATLAB/Simulink platform. The proposed method positions the optimal control pulses of the series and shunt APF depend on the source side and load side parameters through the phase angle. In the proposed method, different source side parameters, load side parameters are analyzed to calculate the phase angle for provided control signals in IUPQC. After that, the proposed BOA based controller has maintained the dc-link voltage. The control signals of the IUPQC are compensate the voltage variations and the

current perturbations. The gain of the proposed manage technique is the robustness, the reliability and the adaptability for diverse forms of problems. The proposed technique has been carried out and the overall performance has been evaluated below exceptional kinds of pq problems including voltage sag and voltage swell. The effectiveness of the proposed technique changed into tested thru a comparative evaluation with distinctive traditional techniques inclusive of fa and alo. From the assessment evaluation, it's been found that the proposed manipulate technique became very much effective in improving the pq of the gadget than the alternative techniques.

## REFERENCES

1. Bruno W. França ; Leonardo F. da Silva ; Maynara A. Aredes ; Maurício Aredes, "An Improved IUPQC Controller to Provide Additional Grid-Voltage Regulation as a STATCOM", IEEE Transactions on Industrial Electronics (Volume: 62, Issue: 3, March 2015)
2. G. Mythily, S.V.R. Lakshmi Kumari, "Power Quality Improvement by IUPQC", 2018 International Conference on Inventive Research in Computing Applications (ICIRCA)
3. Raphael J. Millnitz dos Santos; Jean Carlo da Cunha; Marcello Mezaroba, "A Simplified Control Technique for a Dual Unified Power Quality Conditioner", IEEE Transactions on Industrial Electronics (Volume: 61, Issue: 11, Nov. 2014).
4. He, Jinwei, Yun Wei Li and Frede Blaabjerg, "Interline Unified Power Quality Conditioner", IEEE Transactions on Power Delivery (Volume: 22, Issue: 1, Jan. 2007)
5. Washima Tasnin; Lalit Chandra Saikia, "Impact of renewables and FACT device on deregulated thermal system having sine cosine algorithm optimised fractional order cascade controller IET Renewable Power Generation (Volume: 13, Issue: 9, 7 8 2019)
6. More Raju; Lalit Chandra Saikia; Nidul Sinha, "Load frequency control of a multi-area system incorporating distributed generation resources, gate controlled series capacitor along with high-voltage direct current link using hybrid ALO-pattern search optimised fractional order controller", IET Renewable Power Generation (Volume: 13, Issue: 2, 2 4 2019)
7. Oliver Cwikowski; Joan Sau-Bassols; Bin Chang; Eduardo Prieto-Araujo; Mike Barnes, "Integrated HVDC Circuit Breakers With Current Flow Control Capability", IEEE Transactions on Power Delivery (Volume: 33, Issue: 1, Feb. 2018)
8. Guoqing Li; Jing Bian; He Wang; Zhenhao Wang; Yechun Xin; Jiabin Guan, "Interline dc power flow controller with fault current-limiting capability", IET Generation, Transmission & Distribution (Volume: 13, Issue: 16, 8 20 2019)
9. Farheen Chishti; Shadab Murshid; Bhim Singh, "Development of Wind and Solar Based AC Microgrid With Power Quality Improvement for Local Nonlinear Load Using MLMS", IEEE Transactions on Industry Applications (Volume: 55, Issue: 6, Nov.-Dec. 2019)
10. Nantheera Anantrasirichai ; Wesley Hayes; Marco Allinovi; David Bull; Alin Achim, "Line Detection as an Inverse Problem: Application to Lung Ultrasound Imaging", IEEE Transactions on Medical Imaging (Volume: 36, Issue: 10, Oct. 2017)
11. Ligang He; Huanzhou Zhu; Stephen A. Jarvis, "Developing Graph-Based Co-Scheduling Algorithms on Multicore Computers", IEEE Transactions on Parallel and Distributed Systems (Volume: 27, Issue: 6, June 1 2016).

# Power Quality Improvement in DG System using BOA based Interlined Unified Power Quality Conditioner

## AUTHORS PROFILE



**M. Anitha (Mallipeddi Anitha)** obtained her Bachelor's degree in Electrical and Electronics Engineering from University of JNTU. Master's degree in Power system from university of ANU, currently pursuing PhD degree in Electrical and Electronics Engineering At Andhra University. Currently, she is an Assistant professor at the Faculty of Electrical and electronics engineering, at

RVR&JCCE, Chowdavaram, Guntur. Research Area of Interest: power systems



**Dr. T.R. Jyothsna (Tummala Radha Krishnan Jyothsna)** Received the Bachelor's degree, master's degree and Ph.D. Degree from Andhra university. She is currently **Professor** in the Department of Electrical and Electronics Engineering at Andhra University, Visakhapatnam, Research Areas of Interest: Power System Analysis, Power System Dynamics and Stability,

Renewable Energy, Power Electronics, Power Electronic Devices and Controllers, Application of Power Electronic Devices to Power Systems