

11-level Multilevel Inverter for Medium Voltage High Power ID and FD Fan Drives in Power Plant



B. V. Pranav, Y. Mohana, Mule Sai Krishna Reddy, K.V. Siva Reddy, S. Ravi Teja

Abstract: Multi-level inverter technology has emerged recently as a very important alternative in the area of medium-voltage high-power energy control such as ID and FD fans which runs with the help of these megawatt power drives and renewable energy integration to grid such as solar energy integration which requires pure sinusoidal voltage with less than five percent THD to synchronize to grid. For the requirement of large voltage sources(DC) in number, reduced electromagnetic interference, utilization of power electronic devices having less voltage blocking capability, less percentage of total harmonic distortion in output voltage, reduced stress on insulation they are mostly used. Various topologies are used for multilevel inverters. Among them the most commonly used is cascaded H-bridge (multi-cell). A 3-phase 11-level reduced H-bridge topology is proposed and is controlled by level shift carrier PWM in this paper. The considered topology and controlled algorithm is implemented in MATLAB/SIMULINK. The simulation results show a reduction of THD to a greater extent which will be useful in renewable areas and mega watt power drives.

Keywords: H- Bridge, Multilevel, Inverter, level shift carrier PWM, THD, ID and FD fan.

I. INTRODUCTION

The photovoltaic process has acquired exceptional significance in these modern days in the development of pollution-free electricity. Using solar stages the photovoltaic device transforms the sun's light energy into electrical energy. The electricity generated is in the form of direct current (DC). A photovoltaic network connected to the grid often includes a two-level inverter to transform DC-to-AC.

Yet it is unable to generate a waveform similar to sinusoidal, and thus contributes a high level of harmonic material in current and voltages, rendering the inverter bulky in length [1-4]. In the high-power sector, it is not appropriate with conversion purposes, thus, two level inverters have been substituted by multilevel inverters ideal for high-power conversion. The increased level decreases the harmonic content and brings the waveform of output voltage similar to the sinusoidal [5]. The multilevel inverter (MLI) has thus attracted tremendous interest in the high-voltage sector. There are traditional multilevel inverters with three forms, diode-clamped MLI, MLI moving capacitor and cascaded H-bridge MLI. For diode-clamped MLI, the bulk of diodes are used and the number of diodes decreases with the level increment. In diode clamped MLI has been discussed with lesser number of diodes. The count of capacitor is dominant in flying capacitor MLI, and the number of capacitor decreases with a rise in MLI level, it is addressed the modified flying capacitor. In cascaded MLI, as the level of the cascade increases, the quantity of switches and sources will certainly increase [6-8]. To obtain 11-level output five H-bridge cells are required, but the same 11-level output can be obtained from three H-bridge cells with unequal voltage rating of dc sources. For example for 11-level with three H-bridge cell configuration V_{dc} , $2V_{dc}$ and $3V_{dc}$ level sources are required. Although reduction in no. of H- bridge cells is achieved, but this type of configuration is compromising modularity, equal voltage sharing capability, simplicity in selection of switches [9-10]. Hence the regular configuration with five H-bridge cells of equal source voltage rating is considered with a source voltage of V_{dc} . In the power plants ID and FD fans play a major role and they work under megawatt power drives. If trouble arises with a single draft fan the entire plant unit generation would be stopped. In this paper the proposed configuration is a modular multilevel inverter which would drive the ID and FD fans. Even if a single H-Bridge is failed it acts as a low level inverter and power generation would not be interrupted energy wastage is will be monitored [11-12]. Section-II discusses the proposed converter switching logic and operation. Section-III dedicated to simulation results and analysis and finally comparison with other shifted PWM schemes is done and represented in Section-IV.

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* Correspondence Author

B. V. Pranav, B.Tech, Department of Electrical and Electronics Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, AP, India.

Y. Mohana, B.Tech, Department of Electrical and Electronics Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, AP, India.

Mule Sai Krishna Reddy, Asst.Professor, Department of Electrical and Electronics Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, AP, India.

K. V. Siva Reddy, Asst. Professor, Department of Electrical and Electronics Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, AP, India.

S. Ravi Teja, Asst. Professor, Department of Electrical and Electronics Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, AP, India.

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II. PROPOSED 11-LEVEL INVERTER

A. Proposed Topology Operating Principle

The proposed topology is developed by considering the conventional H-bridge. The stage of proposed topology consists of five H-Bridges in each phase.

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The switching table of proposed topology is shown in Fig 2.1. In the figure only a single bridge in a phase is represented. Five H-Bridges are connected in each phase. The switching table for obtaining the 11-level is hereby shown under in table 2.1.

The switches S1 and S3 are complimentary to the switches S2 and S4. If switch S1 is on it gives an output voltage of V_{dc} in that bridge. If switch S3 is on it gives an output voltage of $-V_{dc}$.

Table 2.1: Switching table for designed inverter

Voltage Levels	B1-S1	B1-S3	B2-S1	B2-S3	B3-S1	B3-S3	B4-S1	B4-S3	B5-S1	B5-S3
0	0	0	0	0	0	0	0	0	0	0
V_{dc}	1	0	0	0	0	0	0	0	0	0
$2V_{dc}$	1	0	1	0	0	0	0	0	0	0
$3V_{dc}$	1	0	1	0	1	0	0	0	0	0
$4V_{dc}$	1	0	1	0	1	0	1	0	0	0
$5V_{dc}$	1	0	1	0	1	0	1	0	1	0
$4V_{dc}$	1	0	1	0	1	0	1	0	0	0
$3V_{dc}$	1	0	1	0	1	0	0	0	0	0
$2V_{dc}$	1	0	1	0	0	0	0	0	0	0
V_{dc}	1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0
$-V_{dc}$	0	0	0	0	0	0	0	0	0	1
$-2V_{dc}$	0	0	0	0	0	0	0	1	0	1
$-3V_{dc}$	0	0	0	0	0	1	0	1	0	1
$-4V_{dc}$	0	0	0	1	0	1	0	1	0	1
$-5V_{dc}$	0	1	0	1	0	1	0	1	0	1
$-4V_{dc}$	0	0	0	1	0	1	0	1	0	1
$-3V_{dc}$	0	0	0	0	0	1	0	1	0	1
$-2V_{dc}$	0	0	0	0	0	0	0	1	0	1
$-V_{dc}$	0	0	0	0	0	0	0	0	0	1

Considering a single phase the levels of the output voltage are as follows:

B. Switching Algorithm

1. First level (1L): When all the switches in all the Five bridges are off it gives an output voltage zero.
2. Second level (2L): When the switch S1 in the bridge -1 is on and the rest other switches are off then it gives an output voltage of V_{dc} .
3. Third level (3L): When the switch S1 in the bridge -1, switch S1 in the bridge 2 are on and the rest other switches are off then it gives an output voltage of $2V_{dc}$.
4. Fourth level (4L): When the switch S1 in the bridge -1, switch S1 in the bridge 2, switch S1 in the bridge 3 are on and the rest other switches are off then it gives an output voltage of $3V_{dc}$.
5. Fifth level (5L): When the switch S1 in the bridge -1, switch S1 in the bridge 2, switch S1 in the bridge 3, switch S1 in the bridge 4 are on and the rest other switches are off then it gives an output voltage of $4V_{dc}$.
6. Sixth level (6L): When the switch S1 in the bridge -1, switch S1 in the bridge 2, switch S1 in the bridge 3, switch S1 in the bridge 4, switch S1 in the bridge five are on and the rest other switches are off then it gives an output voltage of $5V_{dc}$.

7. Seventh level (7L): When the switch S3 in the bridge -5 is on and the rest other switches are off then it gives an output voltage of $-V_{dc}$.
8. Eighth level (8L): When the switch S3 in the bridge -5, switch S3 in the bridge 4 are on and the rest other switches are off then it gives an output voltage of $-2V_{dc}$.
9. Ninth level (9L): When the switch S3 in the bridge -5, switch S3 in the bridge 4, switch S3 in the bridge 3, are on and the rest other switches are off then it gives an output voltage of $-3V_{dc}$.
10. Tenth level (10L): When the switch S3 in the bridge -5, switch S3 in the bridge 4, switch S3 in the bridge 3, switch S3 in the bridge 2 are on and the rest other switches are off then it gives an output voltage of $-4V_{dc}$.
11. Eleventh Level (11L): When the switch S3 in the bridge -5, switch S3 in the bridge 4, switch S3 in the bridge 3, switch S3 in the bridge 2, switch S3 in the bridge 1 are on and the rest other switches are off then it gives an output voltage of $-5V_{dc}$.

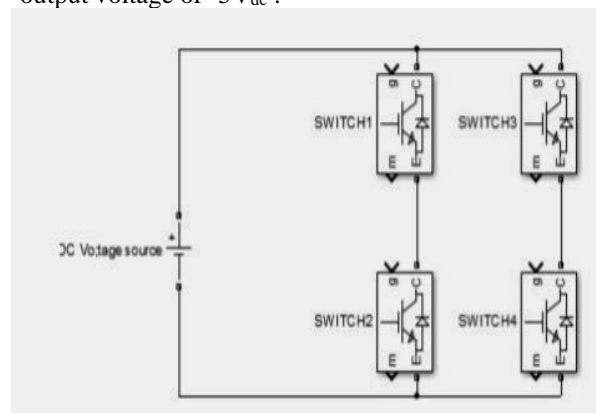


Fig. 2.1 H-Bridge

The proposed system has implemented the carrier based level shift PWM for 11-level cascaded H-Bridge MLI. In this topology if there are m levels $m-1$ carriers are to be generated. Initially first level carrier is generated depending on the carrier frequency and the number of carriers. Remaining carriers are generated by adding dc -offset to the first level carrier. All these carriers are bounded in the range of -1 to 1 . These carriers are compared with m value which depends on the amplitude of the reference wave (sinusoidal) having maximum value of 1 .

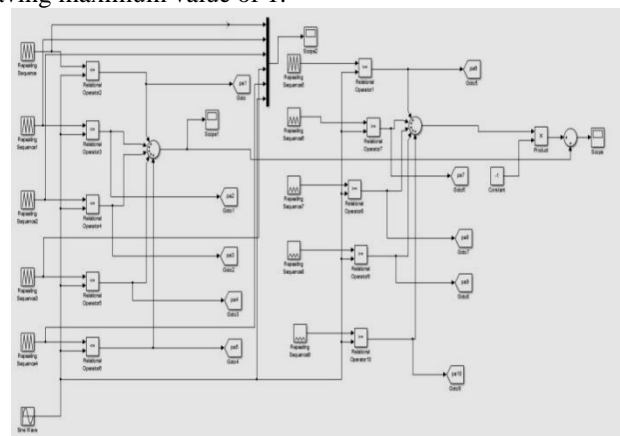


Fig 2.2 PWM Generation Module

The proposed configuration used level shift carrier PWM technique. For 11-level inverter one needs to have ten carrier signals. It is compared with sine wave and pulses are generated with respect to that and those are given to switches.

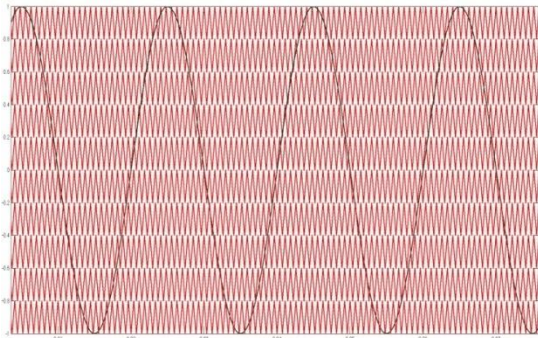


Fig 2.3 Comparison of reference with carrier

Level shift methods are based on the amplitude modulation (ma). To attain different levels by changing the value of ma. The levels are generated when their respective level carriers are compared with the reference wave (sinusoidal). The different types of level shift modulation are phase disposition PWM, Phase opposition disposition PWM, Alternative Phase opposition Disposition PWM.

III. SIMULATION RESULTS

The proposed Multi-cell configuration is simulated and verified using MATLAB/SIMULINK. The obtained results are for ma=1 and with each H-bridge DC source voltage of 100Volts to obtain a maximum value of 500Volts approximately. The results were obtained under the consideration of specifications as shown in the below table 3.1

Table 3.1 -specifications of proposed topology

S.No	Specification	Rating
1	H-Bridge Voltage	100 Volts
2	Induction machine power rating	1000Watts
3	Value of m_a	1
4	Carrier Frequency	1.35kHz
5	Nominal Voltage of the induction machine	415Volts

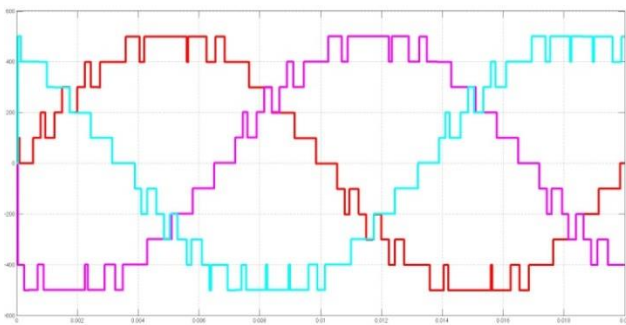


Fig 3.1-Output Voltage of 11-level cascaded inverter

The figure 3.1 represents the output voltage of the 3 phase 11-level cascaded H-bridge multilevel inverter .It can clearly observed the 11-levels in the output voltage which is almost sinusoidal. Filter requirement is also not there as the output voltage is almost sinusoidal which can be used for megawatt power drives.

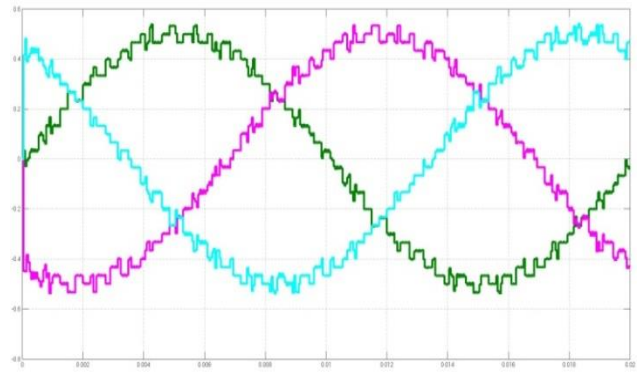


Fig 3.2-Output current waveform of 11-level cascaded inverter

The figure 3.2 shows the output current of the inverter. The current is almost sinusoidal having a slight ripple with a peak current value of 0.5Amps induction motor load.

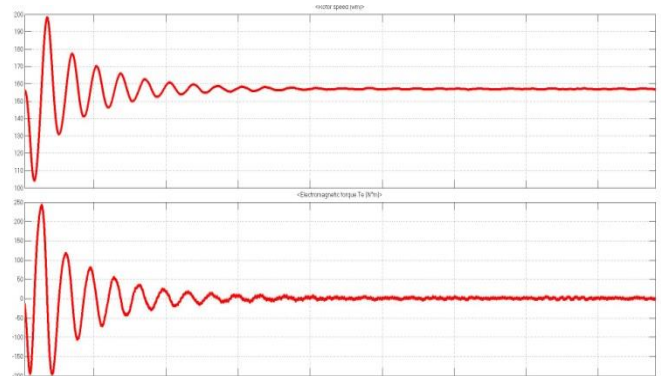


Fig 3.3-Torque and Speed characteristics of induction motor drive

It can be clearly observed that smooth torque and speed characteristics. Torque ripple is even less when operated by the output of this multilevel inverter. The drive operation is very effective when operated under this modular inverter.

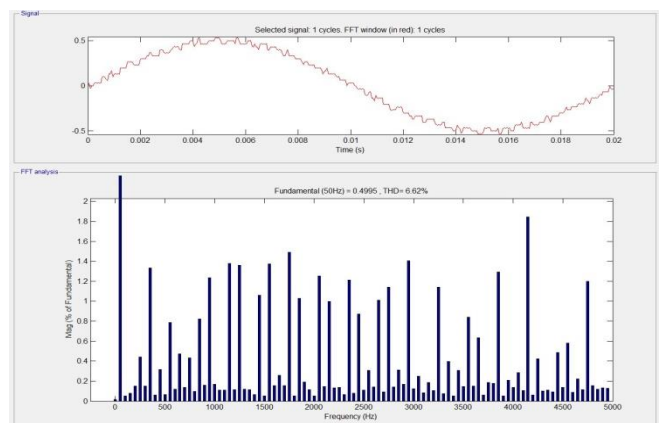


Fig 3.4- THD of the output current

IV. COMPARISION WITH OTHER TOPOLOGIES

It is observed that reduced THD while using phase disposition in level shift carrier PWM technique.

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The resulted THD is comparatively less to that of phase opposition and alternative phase opposition disposition technique. The THD results of those are shown in the fig 4.1 and 4.2

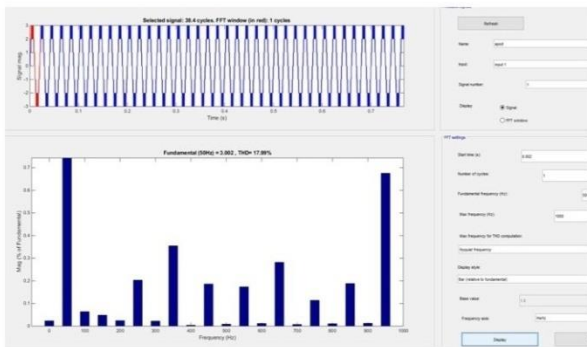
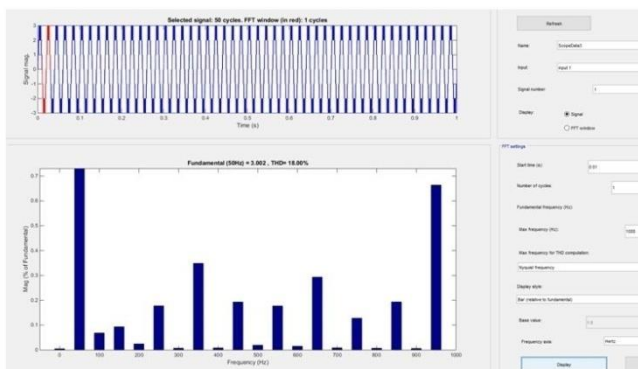


Fig 4.1- THD of phase opposition technique

The figure 4.1 represents the the percentage of THD obtained for an 11-level inverter with phase opposition technique.



The figure 4.1 represents the the percentage of THD obtained for an 11-level inverter with alternate phase opposition disposition technique.

Fig 4.2- THD of alternate phase opposition and disposition technique

Table 4.1- THD comparison of different topologies

S.No	Topology	THD
1	Proposed Topology	6.62%
2	Phase opposition	17.99%
3	Alternate Phase opposition and disposition	18.00%

The various THD values obtained for the different topologies are compared in the above table with the proposed topology THD. It is observed that proposed topology THD is comparatively less than that of the other existing ones.

V. CONCLUSION

To validate the topology the MATLAB/SIMULINK model is done, where carrier frequency f_c is take as 1.35 kHz, single level voltage V_{dc} is taken as 100 volts. The output is shown in figure above. Megawatt power drives are used to run FD and ID fans in thermal power plants. Megawatt power drives can be run only with the help of multilevel inverters. So, these inverters should run with greater efficiency and any mislead leads to the stoppage of power generation. Implementation of cascaded inverter will be very helpful in these areas with greater efficiency and reduced THD. In the implemented inverter even if there is any failure in one of the bridges it

would act as a low level inverter because of its modular structure. Modularity plays a key role here. If this is used to run a drive its speed and torque characteristics settles well and it can be observed the ripple in the torque.

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AUTHORS PROFILE



B. V. Pranav is born in Andhra Pradesh, India. He is pursuing his Bachelor's degree in electrical and electronics engineering from KLEF, Vaddeswaram, Guntur His research interests include electrical drives, power electronics, electric machines, renewable-energy systems, and electrical hybrid vehicles.



Y. Mohana is born in Andhra Pradesh, India. She is pursuing her Bachelor's degree in electrical and electronics engineering from KLEF, Vaddeswaram, and Guntur. Her research interests include electrical drives, power electronics, electric machines, renewable-energy systems, and electrical hybrid vehicles.