International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-9 Issue-2, December, 2019

Design and Implementation of 256 Bit Modified Square Root Carry Select Adder for Area and Delay Reduction

Agnes Shiny Rachel, Rajakumar.G

Abstract- ***This paper models the behaviour of modified Square Root Carry Select Adder and goes deep to investigate on its scope of reducing area and delay. This helps to overcome the drawback of conventional RCA by performing operations simultaneously for both C_{in} = 0 and C_{in} = 1, and the output is multiplexed to obtain the desired response. The work explores opportunities to reduce the area with introduction of BEC logic instead of second block RCA. The implementation of a 4 bit MCSLA and its capability of extending its word size to 8, 16, 32, 64, 128 and 256 bits are presented. The experimental result helps to verify the effectiveness of the approach. This provides understanding on how the reduction of area can bring vital improvements in Very Large Scale Integration.***

Keywords: RCA, BEC, MCSLA, Delay, Area

I. INTRODUCTION

Carry select is an extremely fast digital adder whose speed is increased by reducing the carry propagation to a minimum commensurate with economical circuit design [1]. Carry select adder has two sets of Ripple carry adder of which the first one is given the carry input zero and the other one is given one. A carry select adder with add-one scheme replacing one set of Ripple carry adder has been evolved [2, 12] to reduce the area with the same speed. Further improvement has been obtained by the successively incremented carry number block structure in the conditional carry select adder circuit as reported in another paper [3] by which the speed has been increased to 38% from the conventional adder. The carry select adder is replaced with an add-one circuit instead of one set of Ripple carry adder with a fast zero finding logic and multiplexer to reduce the area and delay [4]. The power delay product has been attempted to be minimized by the optimization of the global carry network with cell sharing and selection of pre-sums [5, 11]. Also a first code-disjoint totally self checking carry select adder has been proposed wherein the sum bits and inverted sum bits are simultaneously implemented to obtain reduced area and delay [6]. Another method was proposed with an area efficient square root CSL scheme based on a first zero detection logic which brought forth good improvements in power-delay and area-delay product by appropriate exploiting of the logic structure [7].

Revised Manuscript Received on December 30, 2019.

* Correspondence Author

Agnes Shiny Rachel, Assistant Professor (ECE) in Sri Krishna College of Technology,Coimbatore.

Rajakumar.G, Professor (ECE) in Francis Xavier Engineering College,Tirunelveli

Later another carry select adder was introduced with fast all one finding circuits and low delay multiplexers [8,13] that required fewer transistors and 16 % shorter delay as compared to the original dual ripple carry select adder. Owing to the rapid growth in system on chip industry, effective power utilization has become a major design constraint in large scale integration. To achieve this, a novel method has been proposed which makes use of universal NAND [9] gates in the conventional carry select adder by which the area, delay and hence the power delay product PDP has been reduced to a larger extent.

The prime motive of this proposed work is to reduce the area and delay by proper manipulations in the carry select block. The First step that is done to reduce the area is the replacement of the second set of ripple carry adder with the Binary to Excess-1 Converter logic [10]. Also the word size has been increased from 128 bit to 256 bit which ensures fast operation of processors at a comparatively less area. This helps to a great extent to reduce the area but the pavement to large scale integration would also require steps to reduce delay for which the carry skip adder would be a good choice.

II. CARRY SELECT ADDER WITH RCA AND BEC:

The ultimate aim of the work is to model area, delay and power efficient carry select adder.

The work has been divided into two parts

(i) First the system has been extended to perform the operation of 256 bit which helps to a large extent when the applications are to be integrated in large scale.

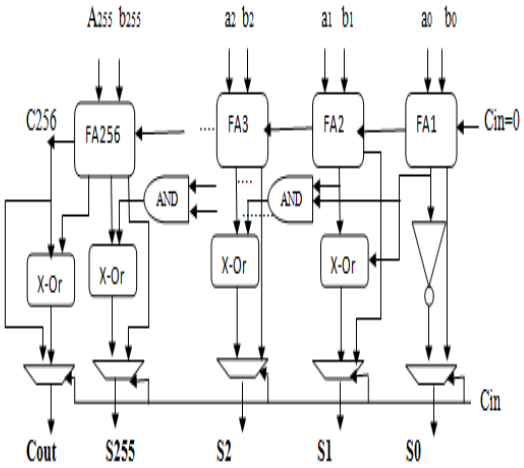

Fig1. 256 Bit Modified CSLA with BEC

(ii) Later the upper set of RCA is replaced with a

(iii) Carry Skip Adder to reduce the delay.

The block schematic for the proposed 256 bit Modified Square Root Carry Select Adder (MCSLA) is shown in Fig 1

The n-bit RCA is replaced by the n+1bit BEC. The number of gates used in BEC is less when compared with RCA. The structure of 256 bit Modified carry select adder is shown in the Fig 1 It has several blocks of full adders and binary to excess-1 convertors.

The prime objective of this method is to bring the delay to control by replacing the upper block of RCA another fast adder the Carry Skip Adder. In this paper the Regular and modified 256 bit CSLA has been compared with the modified CSLA with CSKA focusing their Area and Delay. The system has been implemented in Xilinx 9.1i and the results were verified.

The area calculation of MCSLA is derived from the following steps. From the structure of MCSLA, 8 bit, 16 bit, 32 bit, 64 bit, 128 bit, 256 bit area is calculated. The number of gates utilized by the basic digital elements is given in Table 1.

Table –I: Number of gates

FA	13
HA	6
MUX	20
BEC	24

The removal of Multiplexers would help to a great extent in putting the delay into control. Removal of multiplexers no doubt reduces the delay but the efficiency could be maintained only when they are replaced with an appropriate logic namely Common Boolean Sharing Logic. Also the delay can be reduced equivalently by replacing the RCA at the top with a fast adder like Carry Look Ahead adder.

The total area and Delay of the MCSLA from theoretical evaluation is given in Table 1.

Table-II: Comparison of Regular CSLA (RCSLA) and Modified CSLA (MCSLA) Area

Word Size	Adder	Area(no of gates)	Reduction in no of gates
4 bit	RCSLA	124	
4 bit	MCSLA	96	28
8 bit	RCSLA	244	
8 bit	MCSLA	212	32
16 bit	RCSLA	484	
16 bit	MCSLA	372	112
32 bit	RCSLA	964	
32 bit	MCSLA	740	224
64 bit	RCSLA	1924	
64 bit	MCSLA	1476	448
128 bit	RCSLA	3844	
128 bit	MCSLA	2948	896
256 bit	RCSLA	7684	
256 bit	MCSLA	5892	1792

From the above results it is clear that the area has been significantly reduced with a slight increase in delay. So the future enhancement that is simple and also efficient would be to replace RCA with Carry skip adder which can reduce delay by some significant amount.

III. CSLA WITH CARRY SKIP ADDER AND BINARY TO EXCESS-1 CONVERTER:

In a carry skip adder the bits to be added are divided into blocks of equal length. In each block the bits are compared for un-equivalence by doing the X-OR operation between the bits by which a comparison string is produced. This comparison string is multiplied together using AND within itself. This is done to ensure that the comparison bits of each block are unequal and it can hence propagate the carry to the next block. A multiplexer is used to select either the generated carry or the propagated carry by the help of its select line. If the input bits A_i is not equal to B_i then the carry is skipped over the block. Else if A_i is equal to B_i then the carry is generated in the block.

The delay of an n-bit carry skip adder could be expressed as follows

$$t = t_{setup} + mt_{carry +} (n/m-1)\ tcarry + t_{sum}$$

Where n is the adder length
And m is the length of the blocks.

Comparing to the Ripple Carry Adder, the Carry Skip Adder has slightly improved the speed but with the addition of an extra bypass circuit.

So when compared to the regular Carry Select Adder with two sets of Ripple Carry Adder, the Carry Select Adder with a Carry Skip Adder and Binary to Excess-1 Converter logic stands top in both area and delay . This overcomes the limitation that has been identified in the previously proposed modified square root carry select adder. Also increasing the bit size to 256 bit helps greatly in comparing the improvements achieved, in each step of increase in word size, with also enabling it to perform complex arithmetic operation in a very small area with considerably less delay. This efficient system has been given below Fig 2

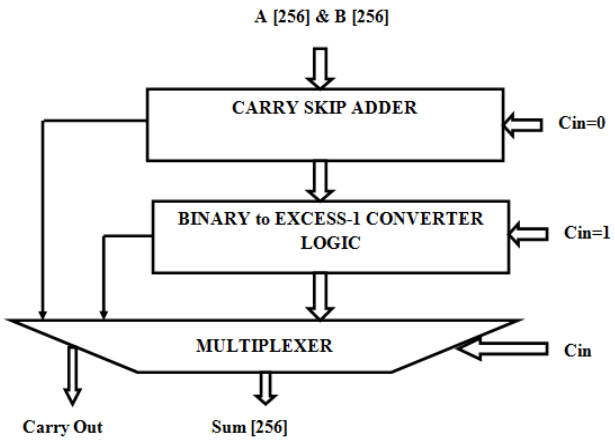

Fig 2. CSLA with CSKA and BEC logic

The carry skip adder which replaces the ripple carry adder reduces the delay greatly by bypassing the carry signal from going through unnecessary propagation inside the full adder block when the carry output of the block remains the same as that of the input.

IV.RESULTS AND DISCUSSIONS:

The 256 bit proposed adder is implemented in both Xilinx and Cadence and the output has been verified. The simulated output of the 256 bit adder with CSKA and BEC logic is shown below in Fig 3.

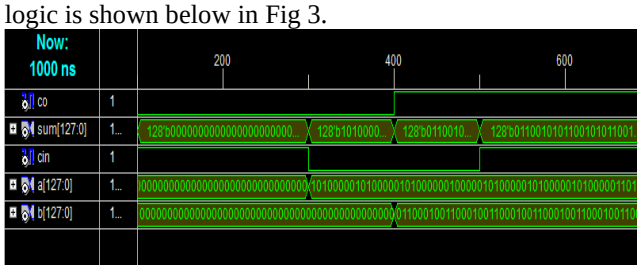

Fig 3. 256 Bit CSLA with CSKA and BEC

The addition of 128 bit binary numbers when implemented in a Carry Select Adder with Carry Skip Adder and Binary to Excess-1 Converter is shown in Fig 4.

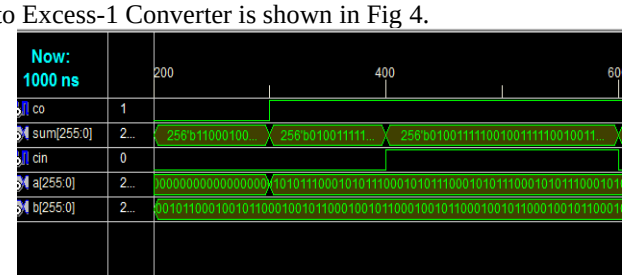

Fig 4. 128 Bit CSLA with CSKA and BEC

The simulation results depict the appropriate and perfect operation of the Carry Select Adder circuit. Also the area and delay have been calculated to ensure the fact that the circuit stands high when compared to the conventional adder. The results as obtained from Cadence has been tabulated below in Table 3

Table 3: Comparison of Delay in CSLA with RCA and CSLA with CSKA

No of Bits	Delay(ns)		
	CSLA with RCA	CSLA with CSKA	
8 bit	1.596	1.528	0.068
16 bit	3.021	1.847	1.174
32 bit	5.871	2.574	2.297
64 bit	11.570	3.982	7.588
128 bit	22.968	6.799	16.169
256 bit	23.754	12.432	11.322

From the above table it is clear that the replacement of Ripple Carry Adder with the Carry Skip Adder has brought about significant reduction in delay. This reduction gains much importance as the word size is increased.

The delay reduction for 128 bit and 256 bit goes beyond 10ns which proves that the proposed Carry Select Adder with Carry Skip Adder and Binary to Excess-1 Converter logic is highly efficient. The output as viewed from Cadence for the 256 Bit CSLA with CSKA and BEC circuit's delay is shown in Fig 5.

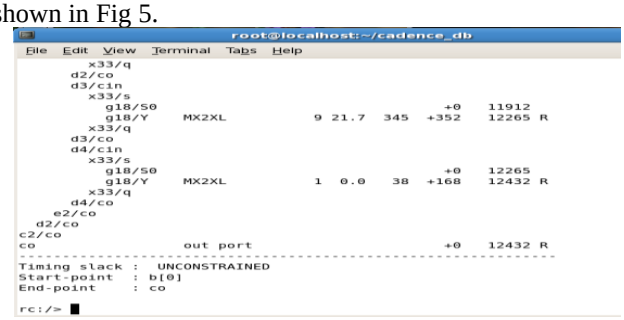

Fig 5: Delay calculation for a 256 Bit CSLA with CSKA and BEC

The delay value in microseconds is shown in the above Fig 5 which is taken as a snapshot from the Cadence tool.

V. CONCLUSION:

The proposed system aims to reduce the area and delay of CSLA. The reduction of the number of gates and the replacement on RCA with Carry Skip Adder in this work offers a great advantage in the reduction of area and delay. The proposed Modified CSLA architecture therefore has low area, low delay and is simple and efficient for VLSI hardware implementation. This system is used in various applications like multipliers, in digital signal processors to execute various algorithms like FFT, FIR and IIR. The result shows that the proposed Carry select adder would become more efficient by the removal of multiplexers which would facilitate much more reduction in delay.

REFERENCES:

1. Bedrij O. J, "Carry-select adder", IRE Transaction on Electronic Computers, pp.340–344, 1962.
2. T.Y.Chang and M.J.Hsiao, "Carry Select Adder using Single Ripple Carry Adder", Electronics Letters, Vol 34,No 22.
3. Yen Mou Huang and James B.Kuo, "High Sped Conditional Carry Select Adder Circuit with SICNB structure for low voltage VLSI implementation" IEEE Trans, Vol 47,No 10.
4. Youngjoon Kim and Leesup Kim, "A low power Carry Select Adder with reduced area", IEEE Trans.
5. Amaury Neve, Helmet Schettler, Thomas Ludwig, "Power Delay Product Minimization in High Performance 64 bit Carry Select Adders" ,IEEE Trans ,Vol 12,No3.
6. E.S.Sogomonyan, D.Marienfield, "A new self checking Sum bit duplicated Carry Select Adder", IEEE Trans, pp 1530-1591.
7. Yajuan He,C.H.Chang and J.Gu, "An area efficien 64 bit square root carry select adder for low power applications",IEEE Trans, pp 7803-8834.
8. Yan Sun, Xin Zhang, "High Performance Carry Select Adder using Fast All One Finding Logic",IEEE Trans.
9. Romana Yousuf and Najib-Ud-Din, "Synthesis of Carry Select Adder in 65nm FPGA".
10. H.G.Tamar, A.G.Tamar, "High Speed Area Reduced 64 bit Static Hybrid CarryLookAhead/Carry Select Adder", IEEE Trans.
11. R. Udaiyakumar, Senoj Joseph, Sundararajan TVP, Vigneshwaran D, R. Maheswar, AmiriIraj, "Self Clock-Gating scheme for Low Power Basic Logic Element architecture", Wireless Personal Communications (October 2018, Volume 102, Issue 4, pp 3477–3488) (Springer US), ISSN 1572-834X,DOI : 10.1007/s11277-018-5385-2

12. MI Niranjana, M Vignesh, K Gayathree, B Banuselvasaraswathy "Design Of Multilayered Ripple Carry Adder Using 5-Input Majority Gates In QCA ," International Journal of Advance Research in Science and Engineering, Vol.6,Issue 11, November 2017
13. R. Udaiyakumar, Senoj Joseph, Sundararajan TVP, Vigneshwaran D, R. Maheswar, AmiriIraj, "Performance analysis in Digital Circuits for Process Corner Variations, Slew-rate and Load Capacitance", Wireless Personal Communications (November 2018, Volume 103, Issue 1, pp 99–115) (Springer US),ISSN 1572-834X, DOI : 10.1007/s11277-018-5428-8

AUTHORS PROFILE

Agnes Shiny Rachel ,ME,(PhD) is working as Assistant Professor (ECE) in Sri Krishna College of Technology,Coimbatore.She has an academic experience of 5 years.Her area of interest is VLSI sytems. She has published her papers in 5 international journals and 1 international conference.

Dr.Rajakumar.G ,
B.E.,M.B.A.,M.E.,Ph.D.,D.Litt.,
is working as Professor (ECE) in Francis Xavier Engineering College,Tirunelveli.He has an academic experience of over 15 years.His area of interest is Nano Scale VLSI sytems. He has published his papers in 23 international journals