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CDMA design for on-Chip Communication Network

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Abstract--Network on chip is used to implement the communication features on a Silicon chip. To increase the performance of Code Division Multiple Access (CDMA) Network On Chip (NOC) ,a Standard-basis (SB) Method is Proposed.In this Method, a source code from various transmitters are encoded separately using an orthogonal code . These coded data are Combined together by an Exclusive-OR operation and it is then sent to their destinations through the communication interface.By Performing AND operartion between original coded data and their Orthogonal code, chip sequence can be obtained. The Standard basis (SB) encoding and decoding technique is compared with the Walsh Based (WB) code in terms of power, area and throughput and the Proposed Standard basis encoding and decoding technique is proven to be more efficient.

Index Terms-- CDMA,CODEC,SOC,NOC,Encoder,Decoder, Walsh Code

I. INTRODUCTION

Code Division Multiple Access (CDMA) is a technology used for radio communication and can be used as tool for designing Network On Chip (NOC). CDMA is a multiple access technology, by which many users can transmit data in a single channel. Here a particular bandwidth can be shared between several users. System on chip (SOC) is a better solution for combining more functionality into a single chip. Network on chip technology can be considered as a "Front end solution to a back end problem".

The SOC has advantages like low power consumption, low area, and high speed operation and low cost per gate. The implementation of the SOC is reliable. The complexity araised due to combining many components into a single chip and interconnection between them is the drawback faced by the system on chip .The noiseless communication cannot be a possible solution for this. Hence network on chip (NOC) concept was introduced.

It reduces the complexity involved in designing and also provides better power, speed and reliability. Network on a chip (NOC) is considered as the best integrated solution for high-end system-on-chip designs.

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II. NOC STRUCTURE FOR CDMA

The Network structure of CDMA NoC is shown in Fig.1. In this figure, a Processing Element (PE) will execute the functions. The network interface (NI) will convert the data into packets. These packets are converted into streams of bits through a parallel-to-serial (P2S) bus. The Encoding module E encodes this bit stream with an orthogonal code.

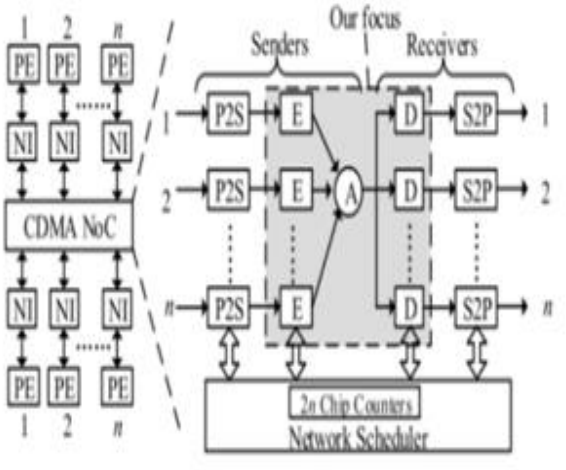


Fig.1. Structure of CDMA NOC

A. Power Consumption

The power consumption of CODEC is related to the complexity of logic block. Complicated modules are used in sequential CODECs which led to high power consumption.The bit synchronization module is needed to ensure the orthogonal property. Each decoder needs minimum of one accumulator. Hence these Combinational logics consume more resources which brings huge penalty in area and power.

B. Transfer Latency

The encoding in sequential CODECs is processed bit-by-bit and it takes k cycles, where k is the codeword length.But Whearas in the Standard-basis CODEC module, the encoder encodes the message with a codeword, so that the codes from different encoders are orthogonal. Hence the speed of the Standard-basis CODEC module is improved.

III. STANDARD BASIS CODEC

A. Standard Basis Encoder

Orthogonal code is used in the the Standard-basis based (SB) codec. AND operation is performed in the encoding module for the input data and orthogonal code.

The resultant is EX-OR data with the orthogonal code and it results in binary sum (BS).

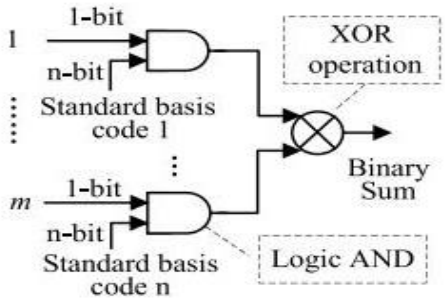


Fig. 2. Standard Basis Encoder

B. Standard Basis Decoder

In the Standard basis decoder, the AND operation is performed for the orthogonal code and Binary Sum.The resultant is EX-OR with each bit. The result is stored in the one bit accumulator . Original data can be reconstructed after the simple accumulation of these chips. The Design is implemented using Modelsim software. This result in overall area and power reduction compared to existing method.

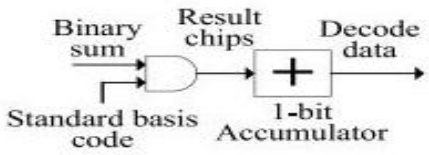


Fig. 3. Standard Basis Decoder

C. Working of Standard Basis Encoder

The Message from the source is given as input to the AND gate on a chip basis. This will give rise to n number of encoded data along with an orthogonal code of a standard basis. The encoded data from various source are combined through an EXCLUSIVE-OR operation. A Output signal is generated which is in binary and it is transferred to the destination serially as shown in Fig. 3.

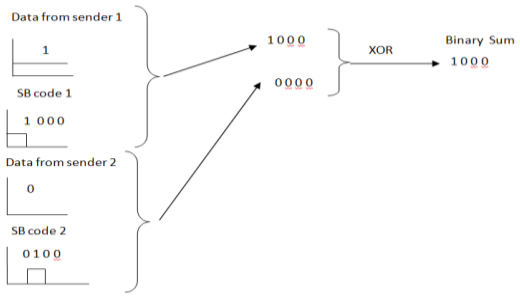


Fig.4. Working of Standard Basis Encoder

D. Working of Standard Basis Encoder

At the receiver the output binary sum and its orthogonal code are ANDed on the chip-by-chip basis and it is sent to an accumulator .The Message data is retrived from the accumulator after n number of chips are accumulated. It is to be noted that there is always only one chip equal to 1 and rest are equal to 0 for one particular orthogonal code. This accumulated value is maximum 1 and it can be stored in a 1-bit accumulator. Therefore, in the Standard Basis decoding module, one AND gate and one 1-bit accumulator is used. It results in fewer logical resources at the Standard Basis Decoder

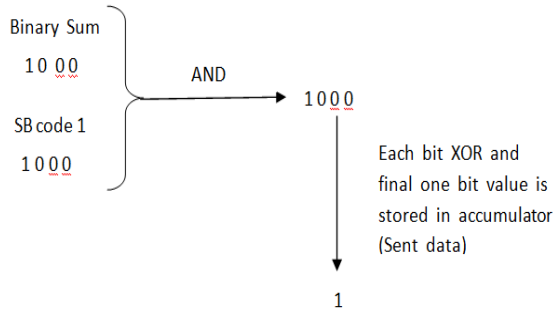


Fig. 5. Standard Basis Encoder

IV. RESULTS

The Simulation results for Walsh and Standard Basis CODECs are taken and the area , power and speed are compared. In this project , existing method (Walsh Basis Codec) and proposed method (Standard Basis Based Codec) is implemented using modelsim software.

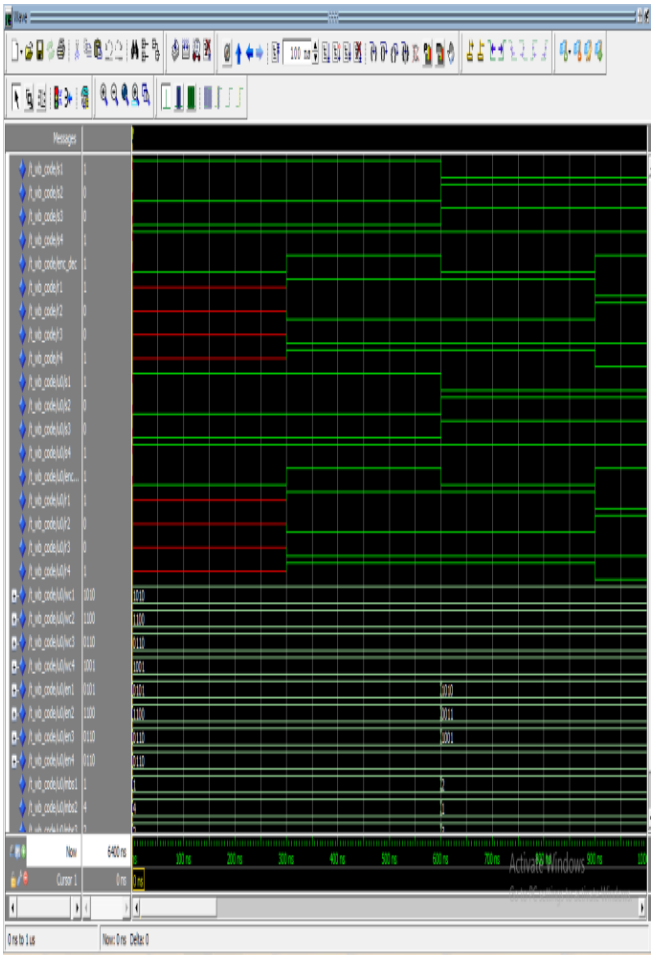


Fig. 6. Simulation of Walsh Based Code

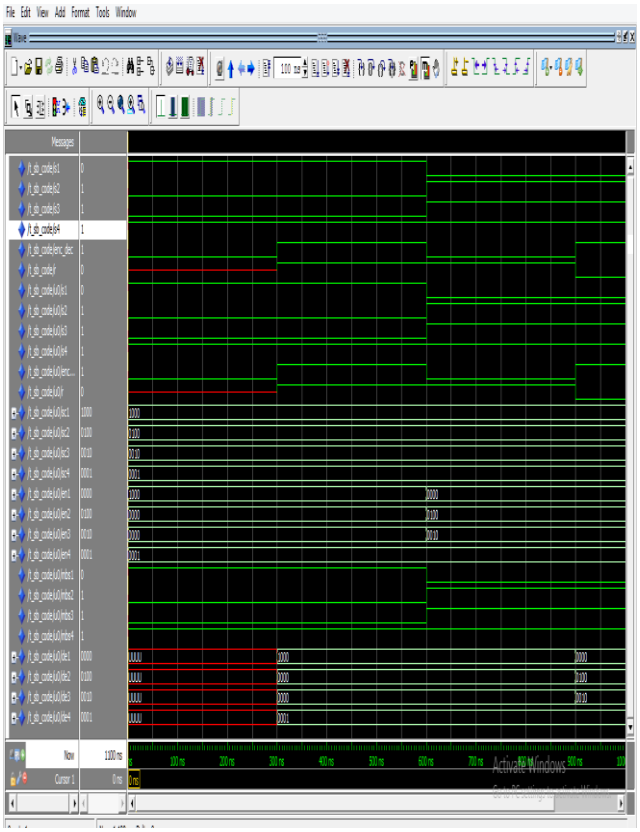


Fig. 7. Simulation of Standard Basis Based Code

The simulated results shows that the standard Based Codec has less area , low Power and hih speed.

V. ANALYSIS

A. ANALYSIS OF WALSH BASIS METHOD

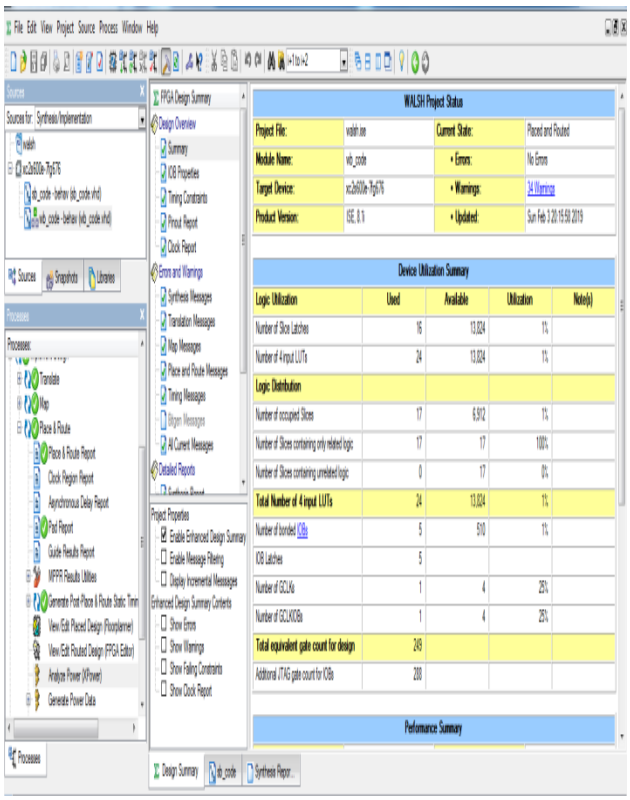
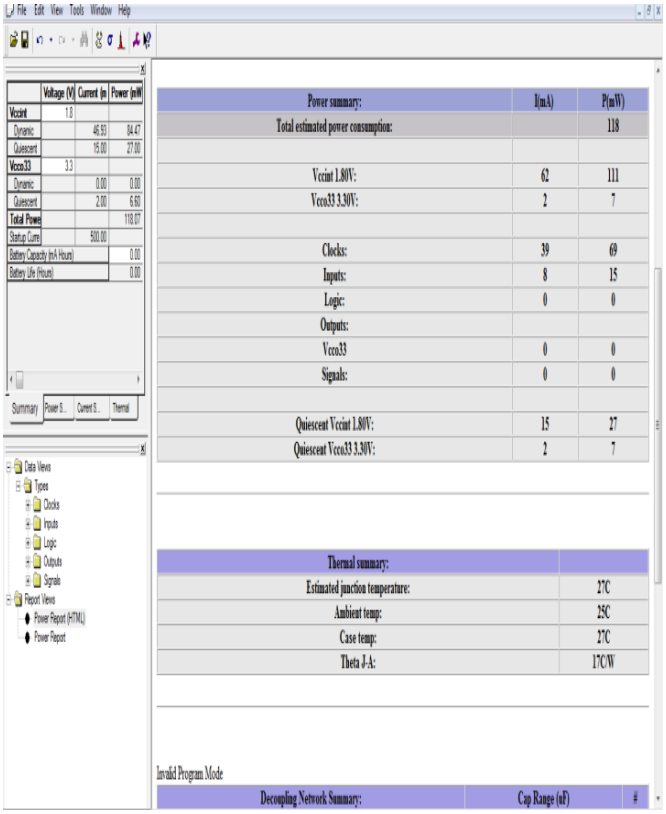


Fig. 8. Walsh Method Area Analysis



Power summary:	I(mA)	P(mW)
Total estimated power consumption:		118
Vccint 1.80V:	62	111
Vcco33 3.30V:	2	7
Clocks:	39	69
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Thermal summary:	
Estimated junction temperature:	27C
Ambient temp:	25C
Case temp:	27C
Theta J-A:	17C/W

Fig. 9. Walsh Method Power Analysis

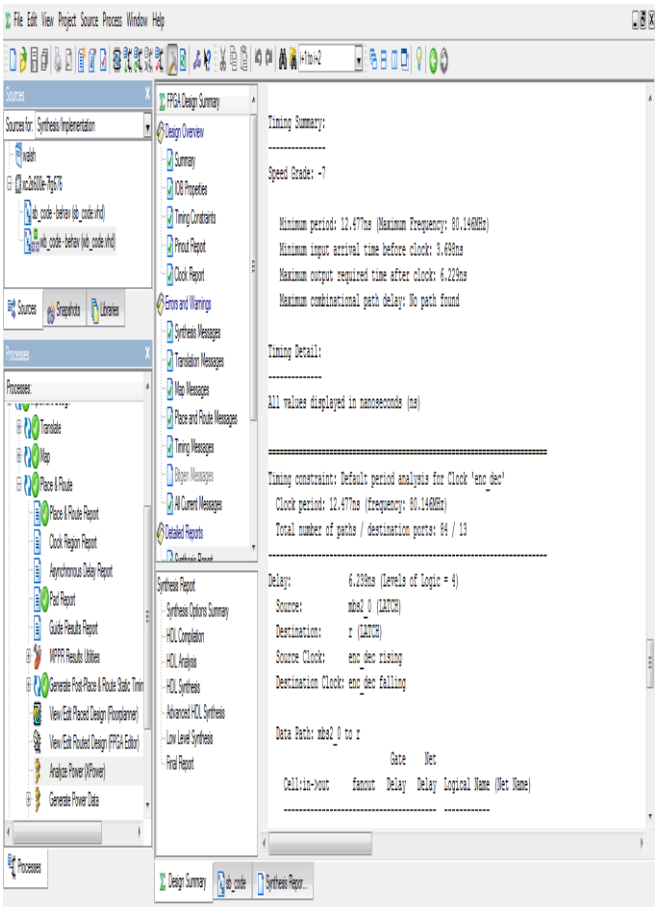


Fig. 9. Walsh Method Delay Analysis

B. ANALYSIS OF STANDARD BASIS METHOD

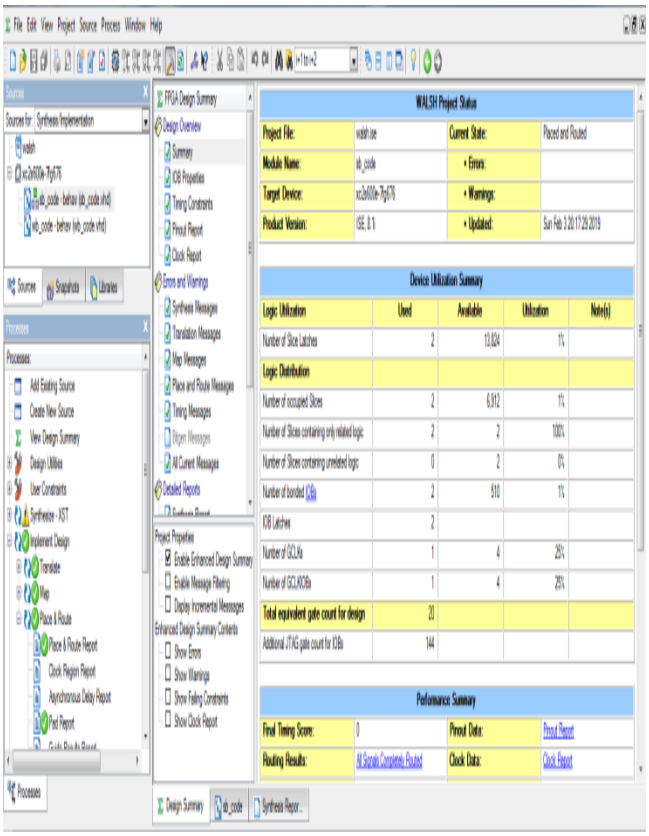


Fig.10. Standard basis Method Area Analysis

Fig. 11. Standard basis Method Power Analysis

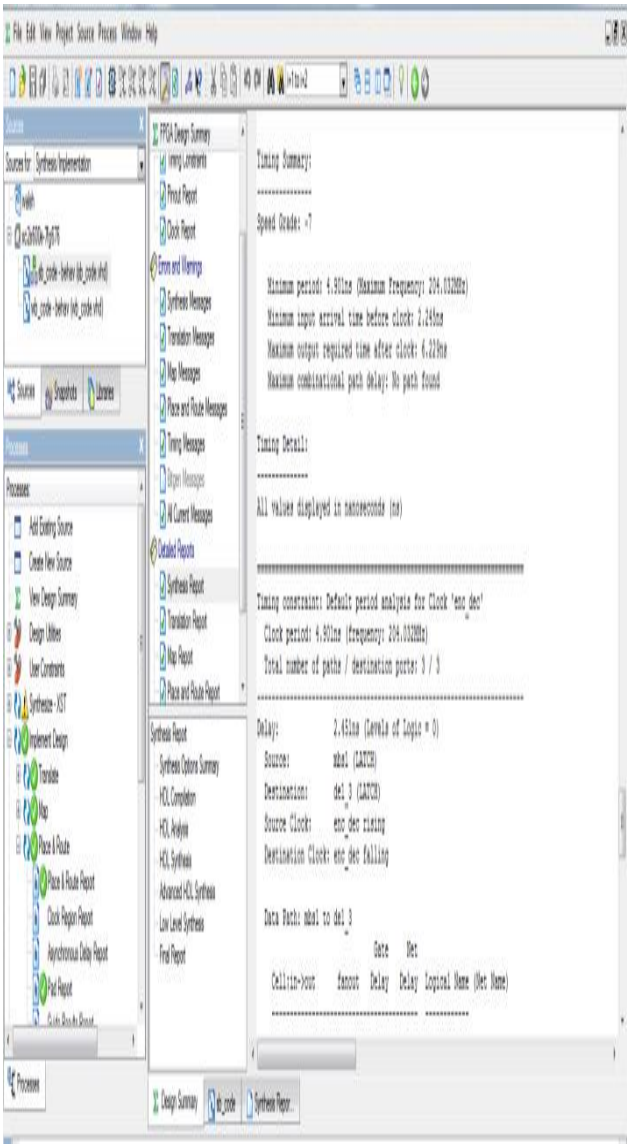


Fig. 12. Standard basis Method Delay Analysis

The total logic cost of the SB method is lesser than that of the WB method, since each operation needs less logical resources. We compared the performance of CDMA NoC's using the two encoding/decoding schemes. Besides the encoder module and decoder module, other on-chip modules, such as network scheduler, parallel to- serial modules, and serial-to-parallel modules, are all included in the NoC's.

Table I Analysis Of Sb And Wb Methods

Design method	Power (mW)	Area (gate count)	Delay (ns)	Frequency (MHz)
Walsh codec	118	249	6.23	80.146
Standard basis based codec	111	20	2.451	204.03

VI. CONCLUSION

Each operation in SB method requires only few resources hence the logic cost is lesser than that of the WB CODEC. The performance of CDMA NoC's such as serial-to-parallel converter , parallel to- serial converter and network scheduler are Compared.

The proposed Standard Basis CDMA NOC method can be designed by using simple design with Low power , low cost and less area.The delay is decresed and the throughput of NoC's is increased in this proposed method. From the simulated results, it is found that this method has improved performance than the previous methods.

Thus the latency, chip area and power are reduced in the proposed Standard basis based method when compared to the existing Walsh method.

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