International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-9 Issue-2, December, 2019

Hardware Implementation of 15-Level Cascaded Multilevel Inverter using Pic16f877a

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Abstract*: Multilevel inverters can manufacture a high- power, high- voltage inverter with a multilevel structure to control the voltage of the device. A symmetrical multilevel cascaded standard inverter requires 'n' DC sources for' 2n+1' levels that require isolated DC sources for power conversions. The objective of this paper is to increase the number of levels by reducing the number of dc sources. The proposed scheme is to use a multilevel asymmetrical inverter with a separate DC power supply. The analysis is extended to the use of the single DC power source with the remaining ' n-1 ' DC source being a capacitor and simultaneously maintains the capacitor 's DC voltage level and selects a fundamental frequency switching pattern to produce an almost sinusoidal output. Matlab simulink simulation is performed to verify the performance of the Asymmetrical Multilevel Inverter using isolated Dc source. The results of simulation and hardware are presented and discussed in this paper.

Keywords* : MATLAB, Optimization Angle Control, Asymmetrical Multilevel Inverter, Symmetrical Multilevel Inverter

I. INTRODUCTION

A multilevel inverter is an all the more dominant inverter that does likewise as an inverter, with the exception of in higher power circumstances. multilevel inverters are a powerful source that is frequently utilized in modern applications and can utilize sine or changed sine waves. Rather than utilizing a single converter to change over an AC current to a DC current, a multilevel inverter utilizes a scope of semiconductor control converters (typically a few) to produce higher voltage. While with an inverter can move vitality with the flip of one switch, with a multilevel inverter flip a few switches, each switch requiring a circuit. These various switches and circuits as a rule cost more multilevel inverters than inverters. multilevel inverters incorporate a scope of intensity semiconductors and dc voltage sources with voltages created by ventured waveforms [1]. The multilevel

Revised Manuscript Received on December 30, 2019.
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VSI incorporates yield voltages with decreased consonant contortion and lower electromagnetic impedance [2] contrasted with a two level voltage source inverter (VSI). Expanding the quantity of levels in the multilevel inverters implies that the yield voltages have more strides to make a staircase waveform that decreases consonant contortion. A more noteworthy number of levels, in any case, increment the quantity of gadgets to be controlled and the unpredictability of the control [3][4].

The multilevel inverter creates normal mode voltage, diminishes engine stress and avoids harm to the engine. multilevel inverters can draw low bending information current. The multilevel inverter can work at both essential and higher frequencies[5]. It ought to be noticed that the lower recurrence of exchanging brings about a lower exchanging misfortune and more prominent effectiveness [9][10]. Specific consonant evacuation system together with the multilevel topology brings about a low complete symphonious bending in the yield waveform without utilizing any channel circuit.

There are as of now three surely understood business topologies of multilevel voltage source inverters [4]. They are the multilevel neutral point clamped(NPC) inverter, the multilevel flying capacitor(FC) inverter and the multilevel cascaded H- bridge(CHB).In the CHB multilevel staggered inverter, arrangement associated H-connect cells with disengaged dc voltage sources associated with every cell are utilized [4]. Contrasted with other multilevel inverters, the fell multilevel control technique is simple since it requires no bracing diodes or massive capacitors. The CHB multilevel inverters can be isolated into two gatherings as indicated by the balanced and uneven topology of the dc voltage sources. The qualities for all dc voltage sources are equivalent in balanced topology. This component gives the topology great measured quality. Be that as it may, the quantity of exchanging gadgets is expanding quickly by expanding the voltage level of the yield. To build the quantity of yield voltage levels, no multi - level uneven sort switches are utilized. The dc voltage sources are chosen by the twofold and ternary proportions [8][9].

II. ASYMMETRICAL CASCADED MULTI LEVEL INVERTER

A multi- level cascade inverter is an electronic power gadget intended to integrate the ideal AC voltage from a few DC voltage levels. In a multi- level cascade even inverter with " n" no. We can acquire (2N+1) level from sources.

As we increment the quantity of steps THD diminishes and the necessity of dc source increments. With Asymmetrical Cascaded Multi Level Inverter, the too much huge number of massive transformers required by traditional multi- level inverters can be killed. The clasping diodes and cumbersome condensers required by the diode cinch and flying condenser MLI can likewise be disposed of. 1-stage H-connect inverter number is utilized and associated in arrangement. This technique presents that independently delivers a practically sinusoidal AC voltage waveform. Separate DC source is given or associated with every inverter for the H-connect. A staircase type yield voltage waveform is delivered by falling the yield voltage of every H-connect inverter. The no yield voltage levels are controlled by the no. Utilized in ACMLI of H spans [13]. The subsequent yield voltage is equivalent to the summation of the scaffold yield voltage as appeared in equation (1).

If CMLI has N number of H-Bridges, than output voltage is:

$V_o(t) = V_{o1}(t) + V_{o2}(t) + ... + V_{oN}(t)$ ……..(1)

Where, $V_{o1}(t)$,$V_{o2}(t)$, ... $V_{oN}(t)$ is the output of individual H-bridge.

III. PROPOSED SCHEME

Fig. 1 shows the fundamental association chart for the 15-level inverter in 1 stage. To work a multilevel cascade inverter with a solitary DC source, the capacitor can be utilized as a DC hotspot for every single assistant extension rather than a confined voltage source. In this examination, a plan is suggested that permits the utilization of a solitary DC control source (for example battery or energy component stack) and the remaining n−1 DC sources are condensers. It is demonstrated that the DC voltage level of the capacitors can be kept up all the while and a central recurrence exchanging example can be chosen to deliver a practically sinusoidal yield.

To work a course multilevel inverter utilizing a solitary DC source, it is proposed to utilize capacitors as the DC sources related to single DC source. The DC hotspot for the primary H-connect (H1) is a DC control source with a yield voltage of Vdc. The DC hotspot for the subsequent H-connect (H2) has a capacitor voltage to be held at Vdc/2 and the DC hotspot for the third H-connect (H3) is a second capacitor voltage held at Vdc/4. The yield voltage of the main H-connect is meant by V1, the yield of the subsequent H-connect is meant by V2 and for the third H-connect is signified by V3 so the yield of this DC source course staggered inverter is V(t)=V1(t)+V2(t)+V3(t).

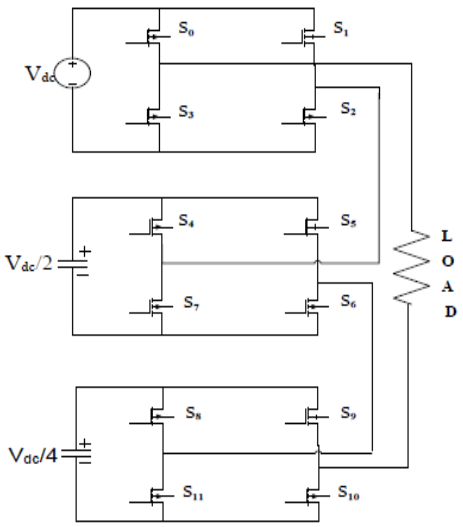

Fig 1.Hardware of 15-level inverter

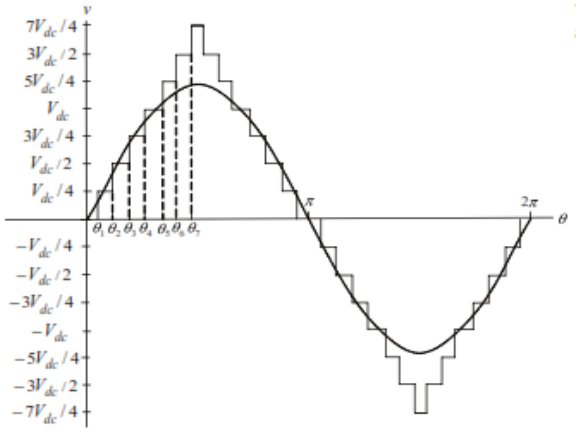

Fig 2. Output voltage waveform for a 15-level inverter

IV. SIMULATION AND THEIR RESULTS

A fifteen-level multilevel inverter simulation shown in figure 3. The primary H-bridge DC source (H1) is a DC power source with an input voltage of 18 V. For the second H-bridge(H_2), a DC power source with an input voltage of 9V and a DC power source with an input voltage of 4.5V of the third H-bridge(H3). The 12 MOSFET switches are used for 15-level inverters, and the load is connected between the H1 and H3 bridges as shown in the figure. Voltmeter V1 and V2 are measured throughout the C1 and C2 capacitor, respectively, with voltages of 9V and 4.5V [14]. A voltmeter V3 measured load voltage. Note that the fifth level is constant at 25V because this level is not used only because the power supply source with condenser voltage. The first, second, third, fourth, six, seven levels, however, require the capacitor voltage and note that the capacitor voltage is not constant. Figure 4 shows the 15-level inverter output voltage form with a single dc source.

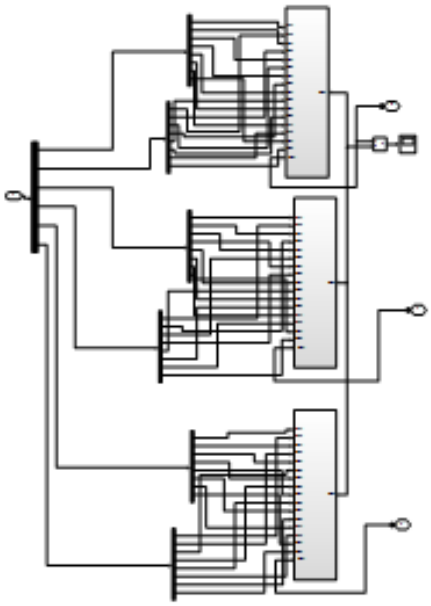

Fig 3. Circuit diagram for 15-level inverter

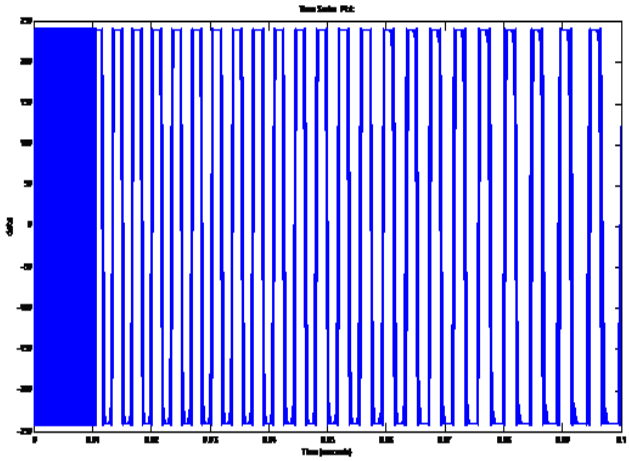

Fig 4. Waveform for 15-level inverter (Using single DC source)

V. HARDWARE AND RESULTS

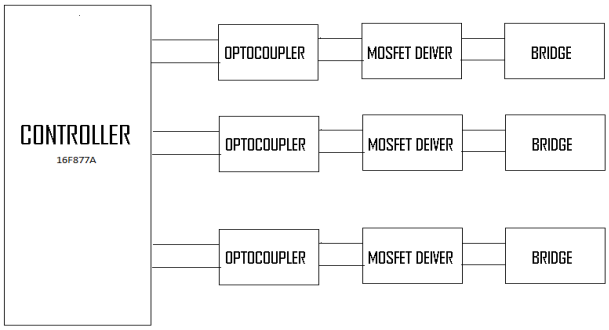

Fig 5. Block diagram of cascade H-bridge Multilevel Inverter

A basic H-bridge cascade block diagram Multilevel Inverter shown in fig 5. It is a control system that generates gate pulses for switches. PIC16F877A microcontroller, a low cost and efficient controller, is used in this control circuit. MOSFETs (IRF840) are used as switching devices in the power circuit [4]. Control and power circuit must be separated from each other. 6n137 opto-coulper is used to provide isolation. The 0-5V square wave is fed to the driver circuit inputs. The correct choice of a MOSFET driver depends on whether a positive or a negative supply is used by the device. International rectifier recommends its independent IR2110 high and low side drivers with a floating channel for bootstrap operation. Each gate driver circuit operates two MOSFETs with a power inverter in opposite leg. The main purpose of the gate driver is to convert the square wave signal from the microcontroller to a level with which the MOSFETs can operate. Here we use IR2110 MOSFET driver with Voffset=500V max and Vout=10- 20 V and 2A output current. The single phase inverter has a maximum input of 325V DC and consists of 4 MOSFET drivers. Each MOSFET is exposed to a maximum voltage of 325 V and a current of 1A [13]. For safety purposes, however, the MOSFETs have been chosen to have a minimum breakdown voltage of 500 V DC and a maximum current of 8A, so that we use IRF840 MOSFET [14].

Fig 6. Hadware Implementation

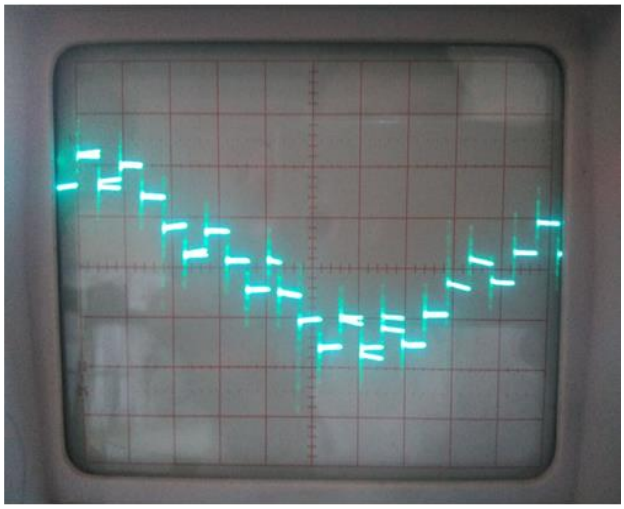

Fig 7. Output waveform of 15-level using a single DC source

Figure 6 shows the hardware setup for 15-Level Multilevel inverter with a single Dc source.

A 3-phase multi- level inverter using MOSFET IRF840 as the experiment's switching device. A power supply with V_{dc}= 18V and 4700 micro-farad(25V) condenser was used as the second and third Dc source as a DC source [9][10]. The main components for this inverter are: uncontrolled single phase rectifier, filter condenser, single phase inverter, inverter control card(Gate driver and opto-coupler) and power supply of 5v and 15v. For this inverter, one single Dc source of 18v is connected to one bridge and for two other bridges the voltage source is condensers, one of the condensers is charged up to 9v and the other up to 4.5V [13]. The use of a microcontroller (PIC16F877A) gives gating signals to the MOSFET for three bridges. A resistive load connects the first and the last terminals of the connected series bridges [14]. The output is measured over the resistive load shown in Fig CRO. Spikes of voltage are seen in the waveform. These spikes occur immediately when both the sources (power supply and capacitor) are simultaneously switched on or off. This is due to the difference in the dead time of the H-bridge switches and the time between the three H-bridges to turn the switch on and off.

VI: THD Analysis Result

Number of level	%THD
15 level (With single DC source)	21

VI. CONCLUSION

The entire research presented in this paper focuses on multilevel inverters with only one supply of DC. And, by increasing no, it was concluded the THD can be reduced from output voltage levels. By increasing the number of MLI bridges, the number of levels can be increased. This paper simulates and implements the H- bridge multilevel inverter on hardware [9]. The H- bridge Multilevel Inverter with a single DC source has some advantages over the conventional H- bridge Multilevel Inverter, because it is used with a single DC source, thus reducing the total size of the required DC source number [10]. As the sources are also reduced, the cost also decreases and the complication is somewhat reduced.

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