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A Novel Delay Based System for Type1 Diabetes using Xilinx System Generator 14.5

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Abstract*: *In this paper an enhanced delay based system is proposed with a parallel execution of PID and Pseudo PID controllers using a Xilinx System Generator14.5. This paper presents simulation results on Direct synthesis, IMC and lambda based designs in both PID and Pseudo PID separately and parallel. The control methodology is suited for the people under Type 1 Diabetes Mellitus and it will maintain a glucose insulin homeostasis.

Keywords* : *Diabetes Mellitus, Pseudo PID controller,Pancreas.

I. INTRODUCTION

Diabetes Mellitus is a devastating, metabolic disorder glucose regulatory system, chronic disease. Type I and Type II are the two types of Diabetes Mellitus. 5-10% of all the cases belong to Type I or juvenile diabetes. These involves autoimmune attack of beta cells. Type 2 Diabetes Mellitus is associated with obesity, early mortality, family related and aged. Traditional methods of treatment involves diet, physical activity, blood glucose testing at home, taking insulin shots daily. Newer technologies involves Pancreas transplantation, pager sized device with tube called insulin pump inserted into the body, fully automated system called pseudo pancreas with an outer supply of insulin. Body receives glucose into the blood stream through food. Addition of glucose increases calcium ions. These calcium ions stimulates insulin to break glucose into useful particles.

After taking meal the glucose level of a healthy person is (120-140mg/dl).When insulin is released from pancreas the glucose level becomes (80-120mg/dl). By Bergman *etal.*, (1981)[1],several glucose insulin dynamics was proposed.The model includes (i)metabolic processes (Pacini, *etal.,* 1985)[2](ii)Pharmakinetic equations based on some non linear effects(Parker *et al.;* 2000)(iii)compartmental physiological equations (Sorensen; 1985). Lenart & Parker,2001[4] had included the mathematical equations for the exercised effects also. (Lehmann, & Deutsch, 1998; Halim *et al.; 1993),*gave predictions based on the diabetics and care. (Parker *et al.,* 2000)[8] proposed a system for glucose regulation comprising of the hepatic glucose intake and production, insulin & glucagon effects on hepatic glucose uptake,with a single pool modeling structure.

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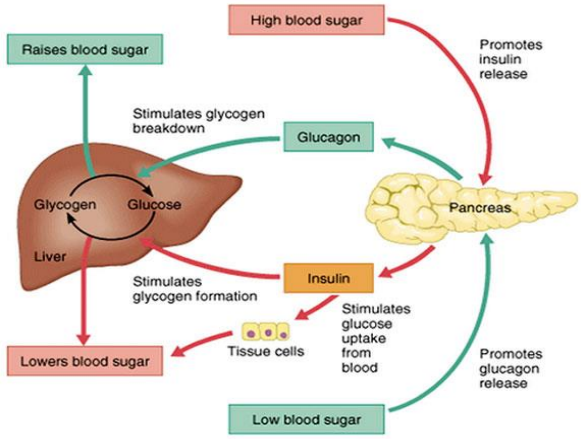

Fig.1.Blood glucose control system

Diabetes Mellitus is caused due to the intake of unhealthy food. Retinopathy, Nephropathy,[peripheral neuropathy, Blindness, Kidney failure, foot ulcers, stroke, are the complications of Diabetes Mellitus.High blood sugar stimulates insulin secretion whereas low blood sugar stimulates glucagon production as in fig 1.

II. PSEUDO PANCREAS SYSTEM

Pseudo Pancreas is a helpful tool for the prevention of diabetes and attempts to use control system tools for the design.

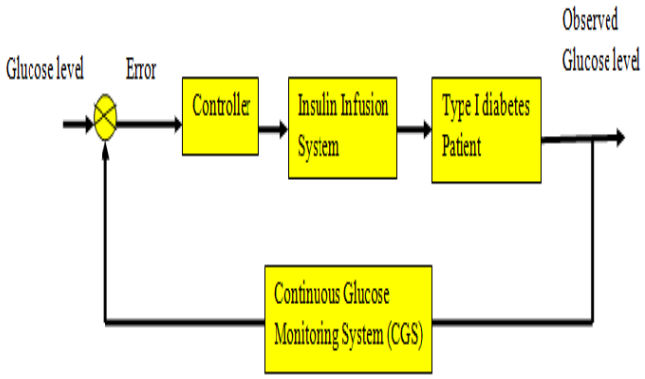

Fig.2..Pseudo Pancreas system

Pseudo Pancreas system (Artificial Pancreas System or APS) helps to maintain normal glucose homeostasis. Pseudo Pancreas consists of Continuous Monitoring System (CMS), insulin pump and controller to calculate the required amount of insulin infusion rate.

Artificial Pancreas or Pseudo Pancreas regulates blood glucose concentration using continuous glucose monitoring sensor continuously at a sampling time of every 5 minutes. The automatic control system adjusts to every modifications depending on meal, exercise, illness etc based on the patient model. Pancreas consists of mainly three types of cells namely alpha cells, Beta cells, Delta Cells.Alpha cells, present at the periphery of islets of Langerhans are responsible for Glucagon production. Beta Cells, present at the centre of islets of Langerhans produce insulin which regulates macromolecules,Amylin which helps in gastric emptying.Delta Cells produce Sumatostatin helpful in regulation of other pancreatic hormones. Artificial Pancreas response to every minute changes in the blood glucose level and release as much insulin based on the nature of the body as in the fig.2.

III. MATHEMATICAL MODEL

$$\frac{dG(t)}{dt} = G_\gamma - h_2(G(t)) - h_3\{G(t)h_4(I(t-\tau_2)) + h_5(I(t-\tau_0)\} \quad (1)$$

$$\frac{dI_p(t)}{dt} = bh_1(G(t-\tau_1)) - \frac{I_i}{t_i}\frac{dI_i(t)}{dt} \quad (2)$$

For the possible calculation and ease of analysis,we prefer mathematical models[Mountcastle, 1968] as per equation (1) and (2) with the following considerations:
1.Blood insulin and blood glucose increase are in equal proportions
2.The regulated variable is always blood glucose.
Expansion of equation (1) and (2) are

I(t)-Concentration of Insulin in cellular fluids
G_γ-rate of absorption of glucose in the blood stream.
G(t)-blood glucose concentration
τ_1, τ_2, τ_3 -delays corresponding to the liver and intercellular space,beta cells and intercellular space,glucose and liver respectively.

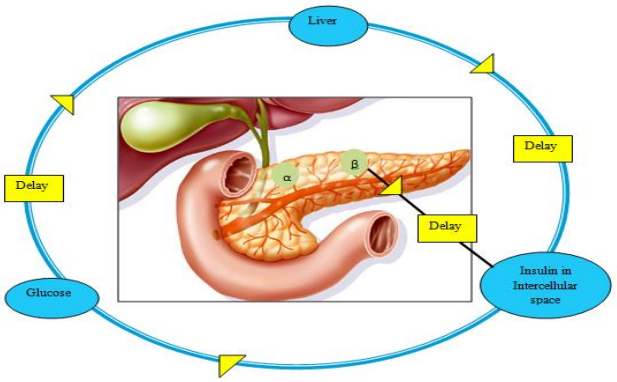

Fig.3 Delay based glucose insulin homeostasis

A. PID Controller

PID controller consists of three basic modes namely:Proportional(P),Integral (I)and Derivative(D).The use of proportional, Integral,Derivative controller stabilizes the gain ,reduces the steady state error and reduces the rate of change of error respectively.The output of PID controller on taking laplace transform with zero initial conditions is

$$U(s) = k_p\left[1 + \frac{1}{T_i s} + T_d s\right] \quad (3)$$

Where K_p -Proportional gain, T_i-Integral time,T_d-Derivative time

B. PSEUDO-PID Controller

Pseudo-PID gives a platform for FPGA, DSP and any other hardware platforms with single tuning parameter K_c. Ziegler-Nichols tuning rules develops an efficient control algorithm.
The PID controller can be represented as

$$U(t)=K_c\,[e(t)+\frac{T_s}{T_i}\sum_{i=1}^{t} e(t) + \frac{T_d}{T_s}[e(t)-e(t-1)]] \quad (4)$$

Incremental PID can be represented as

$$U(t)=U(t-1)+K_c[e(t)-e(t-1)]+\left[\frac{T_s}{T_i}e(t)+\frac{T_d}{T_s}[e(t)-2e(t-1)]+e(t-2)\right] \quad (5)$$

In order to avoid loop saturation,
(i)Substitute proportional,integral and derivative terms with e(t)=-y(t)
(ii)Integral term can be denoted as $e(t)=y_r(t)-y(t)$

Pseudo-PID improves stability and regulates closed –loop performance proposed by H. A. Fertik (Seborg et al., 1989) and J. G. Ziegler and N. B. Nichols (Visioli, 2006).
We obtain the relations

$$\left.\begin{aligned}\frac{T_s}{T_d} &= 0.4\\ \frac{T_i}{T_d} &= 4\\ \frac{T_s}{Ti} &= 0.1\end{aligned}\right\} \quad (6)$$

Thus the Pseudo-PID controller contains a single tuning parameter and is represented as
$U(t)=U(t-1)+K_c\{0.1y_r(t)-3.6y(t)+6y(t-1)-2.5y(t-2)\}$
These involves autoimmune attack of beta cells.

IV. PROCEDURE FOR IMPLEMENTATION

The proposed work is done in a MATLAB-SIMULINK based platform. The laplace transform of the model is reduced using half rule. Delay is calculated on each parameters of the model considering all initial conditions.PID and PSEUDOPID controllers are developed for the model with controllers of direct synthesis, IMC based controllers and lambda based controllers. Execution is done on parallelly with a prudent support of all controllers. Xilinx simulink blocks help in simulation of glucose insulin control metabolism. System generator help in the conversion of files to hardware description language.

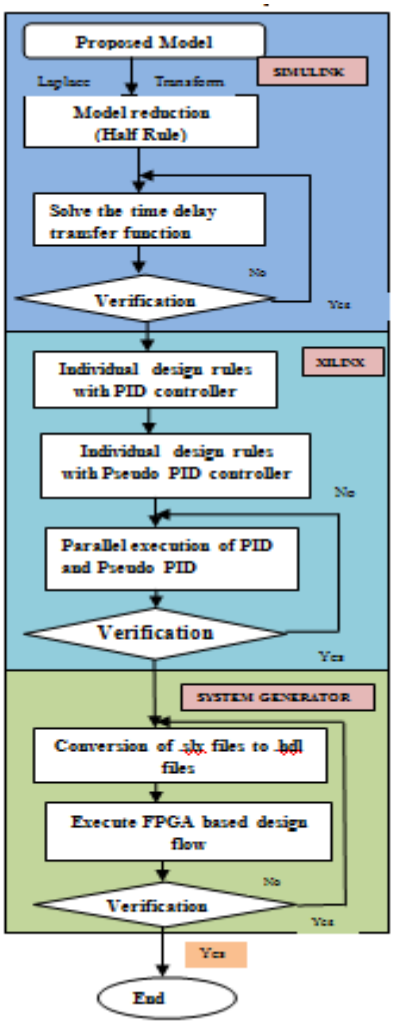

Fig.4 FPGA implementation for the proposed model.

V. PROPOSED WORK

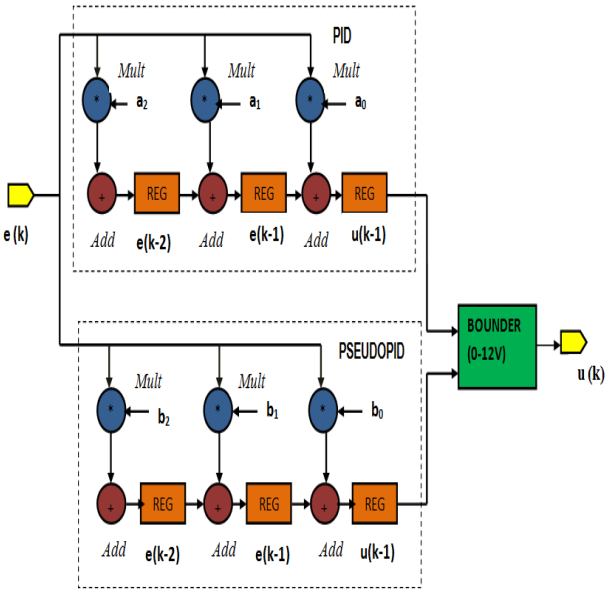

Fig.5 Mathematical implementation strategy

Mathematical model includes the parallel execution of PID and Pseudo PID controller based on FIR filter design methodology with a bounder of (0-12V).The transfer function of each system is given by D(z)=(Y(z)/U(z))

$$D(z)=\frac{a_0+a_1z^{-1}+a_2z^{-2}}{b_0+b_1z^{-1}+b_2z^{-2}} \quad (7)$$

a_0, a_1,a_2,b_0,b_1, b_2 are determined by the process of tuning.

The system input can be predicted in the format of

$$U(k)= u(k-1)+a_0e(k)+a_1e(k-1)+a_2e(k-2) \quad (8)$$

C. IMC based PID Controller

IMC based controller has a single tuning factor K_c which determines the speed of the system.IMC design procedure involves

(i)Design the internal model controller with an equivalent controller in standard form.

(ii)Use a Padé approximation for time-delays in order to find a PID-type control law.

(iii)Compare the IMC-based PI, PID and improved PI controllers for first-order + timedelay processes.

The values of a_0,a_1,a_2 for PID controller is 27.2,-28.34,1.6 repectively and for Pseudo PID controller is a_0=32.88,a_1=-37.42,a_2=6.512.

D. Lambda based PID Controller

Lambda based design rules provide a sound nonoscillatory response.Tuning of parameters on model based method are mainly due to λ while K_c,T_i are not considered.

E. Direct Synthesis based PID Controller

Direct Synthesis deals with the desired closed loop transfer function. Incorporation of performance requirements are done directly. The values of a_0,a_1,a_2 for PID controller is 25.41,-25.43,0.0259and for Pseudo PID controller is a_0=39.433,a_1=-50.495,a_2=13.05 repectively.

VI. IMPLEMENTATION

A. Simple Glucose transfer function Evaluation

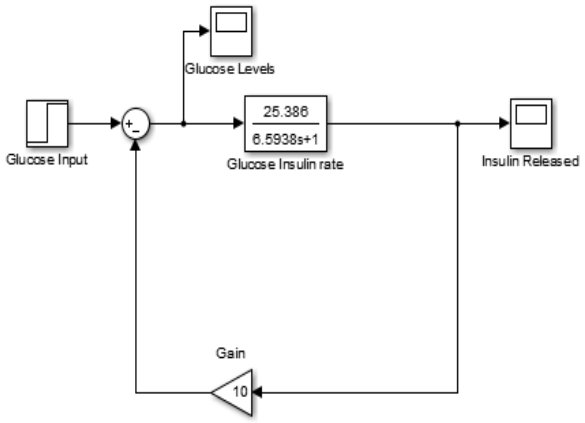

Fig.6 Transfer function evaluation for the entire system

The transfer function evaluation of the entire system is defined using the transfer function as $\frac{25.386}{6.5938s+1}$.

B. Parallel Execution of delay model using Xilinx System Generator

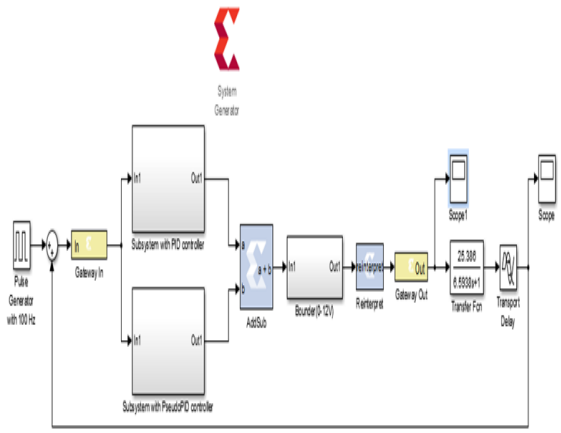

Fig.7 Xilinx system generator for entire system

Xilinx system generator generate core for Xilinx FPGAs to generate HDL codes. This rapid prototyping of FPGA design is used to find number of flipflops,slices,datapath delay etc.

VII. RESULTS AND DISCUSSIONS

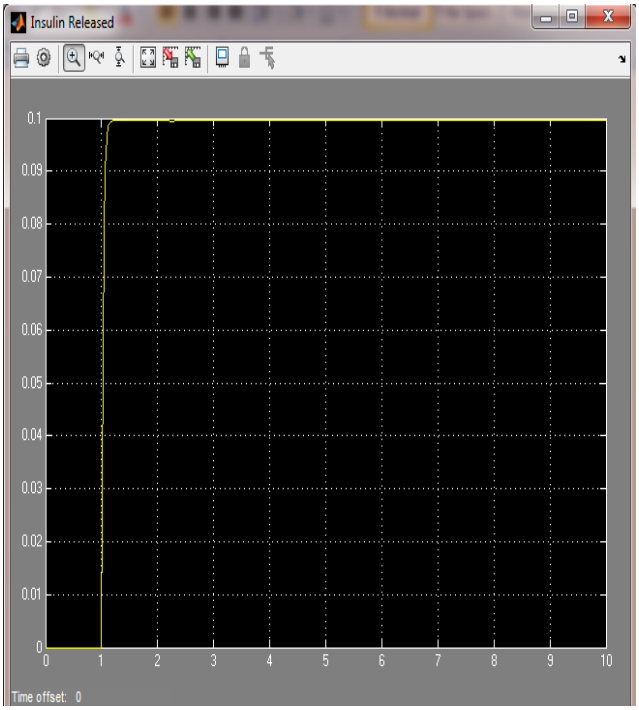

Fig.8 insulin released

Fig.8 shows the amount of insulin released per time for the delay based system.Fig.9 shows the raise in glucose value as per the insulin variation.Fig.10 shows the comparison of direct synthesis,IMC,Lambda with and withoiut feedbacks.IMC based controller shows some minor oscillations in the control action.Here the insulin infusion rate varies depending on the time in seconds.As the bounder varies from (0-12V), the values are restricted to 12V.The oscillated voltage ranges between (0-4)V.

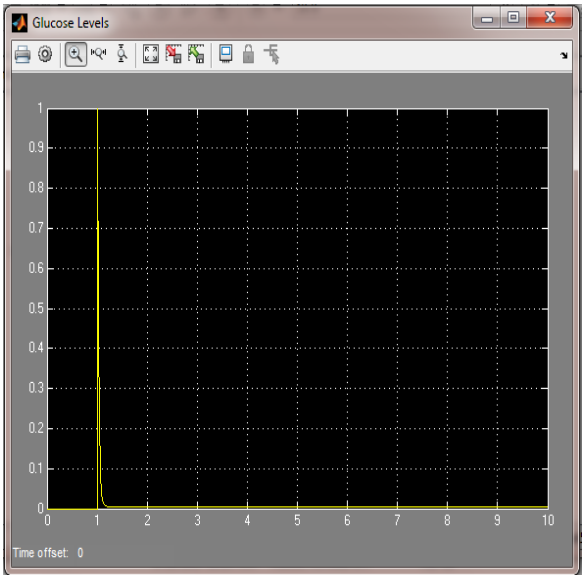

Fig.9 Glucose Produced

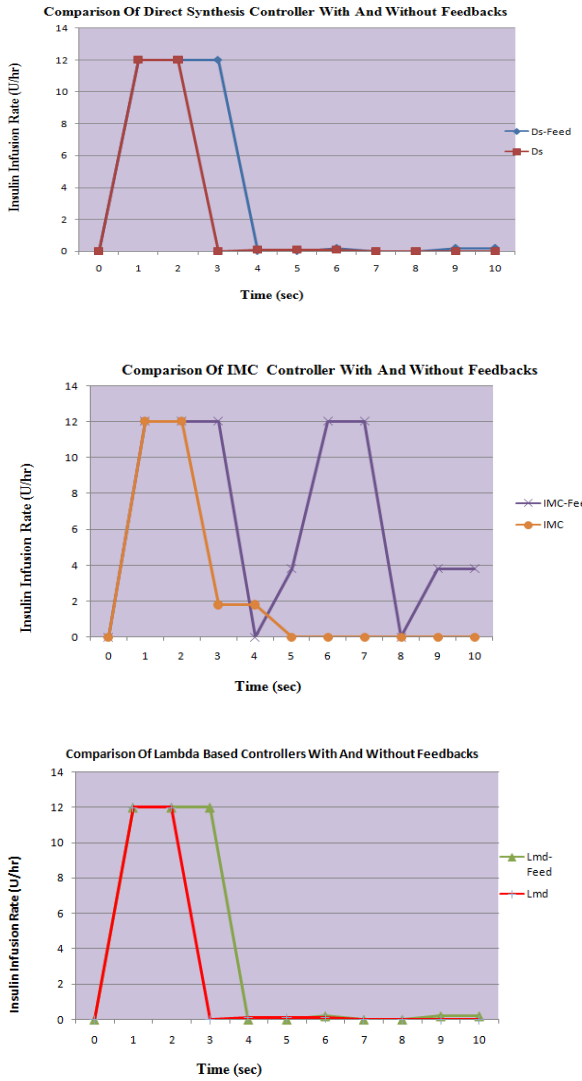

Fig.10 Comparison of various controllers with and without feedbacks

INDIVIDUAL PERFORMANCE ANALYSIS						
Comparison	**Direct Synthesis with PID**	**Direct Synthesis with Pseudo-PID**	**IMC with PID**	**IMC with Pseudo-PID**	**Lambda Based PID**	**Lambda Based Pseudo-PID**
Number of Slice Registers	108	117	117	115	117	117
Number used as Flip flops	106	114	116	114	116	116
Number of Slice LUTs	344	392	404	402	391	418
Number used as logic	317	357	368	368	355	382
Number using o6 output only	280	311	327	327	309	345
Number using o5 output only	3	5	2	2	1	6
Number using o5 and o6	34	41	39	39	40	36
Number used exclusively as route thrus	27	35	36	34	36	36
Number with same slice carry load	27	34	36	34	36	36
Number of occupied slices	124	136	145	145	111	145
Number of LUT Flip flops	344	392	405	403	391	418
Number used as unused Flip flop	236	276	288	288	274	301
Number of fully used LUT-FF Pairs	108	116	116	114	117	117
Number of Slice register sites cost to control set restrictions	6	6	4	6	4	4
Number of bonded IOB's	55	57	57	57	57	57
Average Fanout of Non-clock Nets	3.54	3.37	3.54	3.55	3.38	3.59
Total Memory Usage	146308Kb	147268Kb	147012Kb	146500Kb	147528Kb	147524Kb
Number of External IOBs	55 out of 200(27%)	57 out of 200(28%)	55 out of 200(27%)	57 out of 200(28%)	57 out of 200(28%)	57 out of 200(28%)
Slack/set up path	6.308ns	6.469ns	6.463ns	6.534ns	6.652ns	6.652ns
Data Path Delay	3.586ns	3.510ns	3.509ns	3.439ns	3.348ns	3.278ns
Clock Path Skew	-0.071ns	0.014ns	0.007ns	0.008ns	-0.035ns	-0.035ns
Minimum Period	3.692ns	3.531ns	3.537ns	3.466ns	3.348ns	3.348ns

Fig.11 shows the comparison of Direct Synthesis with PID and Pseudo PID,IMC with PID and Pseudo PID,Lambda based synthesis with PID and Pseudo PID respectively with the effective analysis on the model individually.Average Fan out,number of bonded IOB's,number of external IOB's,data Path delay,clock path skew,minimum period etc.

PARALLEL DESIGN ANALYSIS									
COMPARISON	**DIRECT SYNTHESIS**			**IMC**			**LAMBDA BASED DESIGN**		
	Used	**Available**	**Utilization**	**Used**	**Available**	**Utilization**	**Used**	**Available**	**Utilization**
No. of Slice Registers	235	106,400	1%	240	106,400	1%	239	106,400	1%
Number used as Flip-flops	230			234			238		
Number used as AND/OR logics	5			6			1		
Number of Slice LUTs	731	53,200	1%	754	53,200	1%	798	53,200	1%
Number used as logic	677	53,200	1%	693	53,200	1%	732	53,200	1%
Number using 06 output only	627			649			688		
Number using 05 output only	16			18			21		
Number using 06 and 05 output only	34			26			23		
Number used Exclusively as route Thrus	54			61			66		
Number with same slice carry load	54			61			66		
Number of occupied Slices	222	13,300	1%	247	13,300	1%	252	13,300	1%
Number of LUT Flip -flops pair used	731			754			798		
Number of fully used LUT FF pairs	235	731	32%	240	754	31%	239	798	29%
Number of Slice Register sites lost to control set restrictions	2	106,400	1%	6	106,400	1%	2	106,400	1%
Number of bonded IOB's	58	200	29%	60	200	30%	60	200	30%
Average Fan out of Non-Clock Nets	3.45			3.49			3.54		
Total Memory Usage	149252KB			149572 KB			149252 KB		
Number of External IOB's	58 out of 200			60 out 200			60 out of 200		
Number of Slices	222 out of 13,300			247 out of 13,300			252 out of 13,300		
Number of Slice Register	235 out of 106400			240 out of 106400			239 out of 106400		
Slack/Set up path	6.339ns			6.467 ns			6.433ns		

Data Path Delay	3.582ns	3.437 ns	3.540ns
Clock Path Skew	-0.044ns	-0.061ns	0.008ns
Minimum Period	3.661ns	3.533ns	3.567ns

Fig.11 Parallel Design Analysis

Fig.11 shows parallel design analysis of the system having PID,Pseudo PID controllers in parallel. Parallel execution is better compared to individual controllers because of the variation in system function changes.

VIII. CONCLUSION

Thus the parallel implementation performes well compared to the individual implementations in terms of time and speed.

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