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Cross Coupled Differential High Speed Comparator

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Abstract: ***Power efficiency and high speed comparator is presented. ,n-MOS transistors are used to design preamplifier stage and the latch stage. Both stages are controlled by a special clock circuit. By using clock circuit we can achieve enough pre-amplification gain. At the evaluation phase, the latch is activated with a delay to obtain sufficient pre-amplification gain and avoid extra power consumption. At this phase transistors are cross coupled to increase the preamplifier gain and to lower the input voltage common mode of the latch is used to strongly activate the n-MOS transistors (on the latch input) and reduce the delay. This circuit is designed with n-MOS transistors due to its inherent superiority over the p-MOS transistor. The proposed cross coupled comparator reduces the power and delay compared to conventional CMOS comparators.***

Keywords:Comparator,Dynamic,Latch,Conventional, Preamplifier, Evaluation phase, Reset phase, Delay.

I. INTRODUCTION

In recent times, the usage of low-power high-speed Analog to Digital Converters is increased rapidly that includes hand-held gadgets. Comparators are the key building blocks of various kinds of Analog to Digital Conversions, together with Specificpipeline designs, and flash Analog to Digital Conversion. CMOS amplifiers had been used as static comparators. In past Static comparators are used however they're lower the speed and quantity of power consumption is more.

Due to these drawbacks this sort of comparator aren't applicable for the transportable devices. The drawbacks of the static comparator are overcome by dynamic comparator. Initially come up with a singlestage dynamiccomparator, to enhance speed[2] and to reduce the power consumption.

comparator isn't appropriate for lowpower programsSmaller transistors are used due to low offset voltage[8], so the power consumption will reduce.

But speed of the comparator is A traditional two-stage dynamic comparator is high speed, but to acquire low offset voltage transistor size should be more as a result the circuit size will increase.

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So this traditional two-stage restrained due these strategies. In addition, two-stage dynamic comparator, some of them have higher speed but massive power consumption[10].

Power dissipation is high for many of the comparators. The proposed two-stage dynamic comparator has less power consumption and enhancement in speed. It consists of two stages: preamplifier stage and latch stage. Before to begin comparison, the comparator state is reset to discharge the output node of preamplifier and latch stage to ground and VDD. In next stage, the analysis clock to zero and clock to one to begin comparison.

The output of the preamplifier will increase, once the output voltage of preamplifier stage is approached to the gain voltage of input n-MOS transistor of latch, the latch stage of the comparator is activated. To regulate offset, the input transistors size, area is enhanced. However massive size of transistor will increase the facility consumption.

In pre-amplification stage the transistors are cross coupled to speed up the process. Since n-MOS transistors have some inherent performance when compared to p-MOS[3], this is because of the mobility of electrons, which are carriers in the case of an n-channel device, is about two times greater than that of holes. Thus an n-MOS inputs are used at preamplifier stage and latch stage.

II. RELATED WORK

In fig.1, the conventional dynamic comparator[1] has two stages. The first stage is called pre-amplifier stage and the second stage is Latch stage. Both pre-amplifier and latch stages are controlled by special clock generator. The pre-amplifier stage amplifies the input differential signal. The latch stage, amplifies its input differential signal up to VDD and simultaneously, it also amplifies its input differential signal up to ground.

The connection between first stage and second stage improves inspeed and area, though it has significant power consumptionThe direct connections from first stage to second stage output nodes, endure a large voltage swing which results in kick-back noise[5][6]. To perform comparison in two-stage comparators, we require both clock and inverted signal. So, to overcome this problem, the comparator is proposed to activate the latch by common-mode voltage of the output nodes of the pre-amplifier.

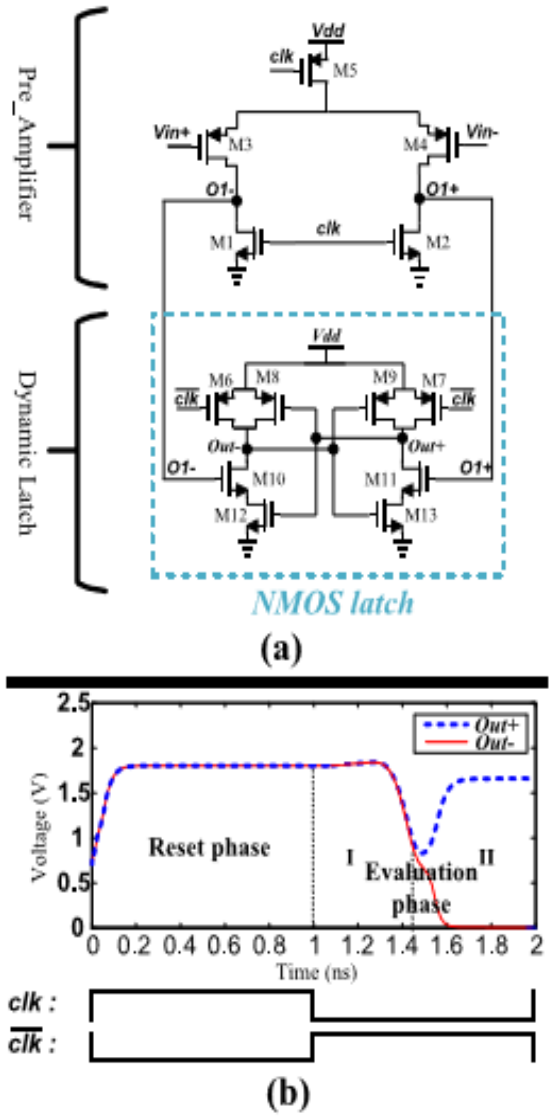

Fig. 1. (a) Conventional two-stage dynamic comparator. (b) Its typical output waveform and clock signal.

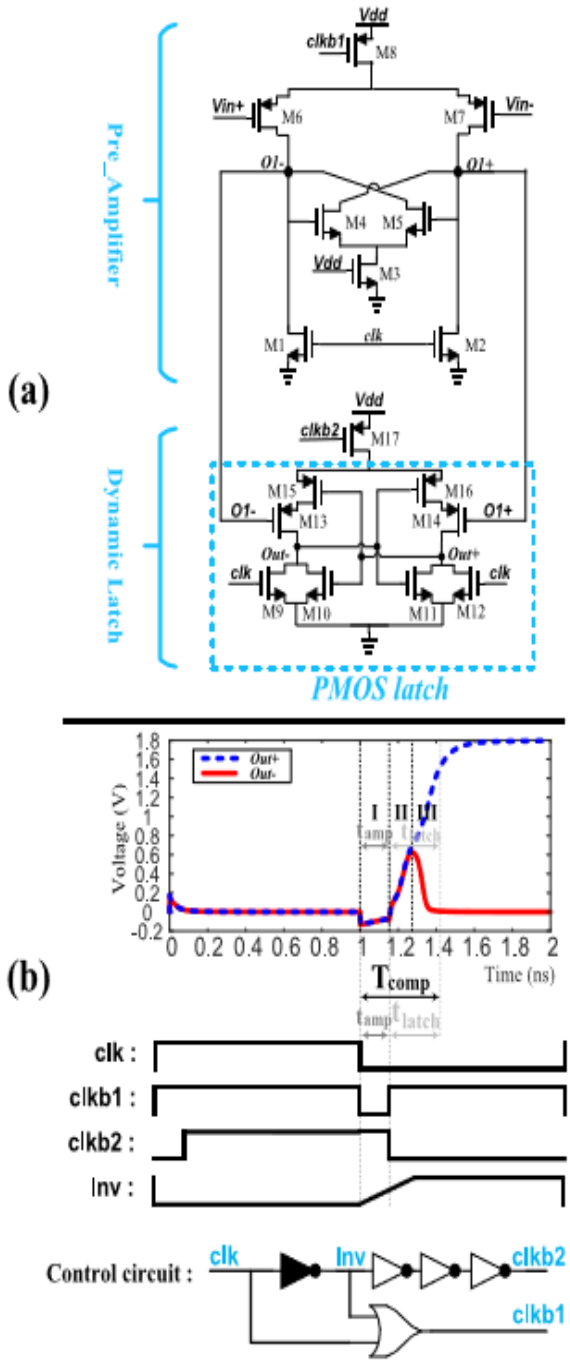

Fig. 2. (a) cross coupled two-stage dynamic comparator. (b) Its typical output waveform and clock signal.

In dynamic conventional two-stage comparators, which is comprised of two phases namely reset phase and evaluation phase. The latch is turned on ,When the common voltage at the output of the preamplifier becomes higher than the threshold voltage[7] of an nMOS transistor (M10,11 in Fig. 1).

Latch employees postive feedback inorder to provide fast amplification. To achieve pre-amplification gain the input size of transistors (M3,4) are high. Considering the large sizing of M3 and M4 transistors which causes large parasitic capacitors at O1+ and O1− nodes, a low-offset comparator demands a high power consumption and speed is limited to speed up the latch[9].

During evaluation phase ,the latch is not activated it remains in off state, until the output voltages of the first stage are large enough to turn on the input nMOS transistors of the latch. Initially latch starts with a speed zero and takes time to increase.

In the fig.2, the p-MOS latch with p-MOS transisitors as input is activated during evaluation phase. The cross-coupled circuit increases the differential voltage (Vidl =[VO1+−VO1−]) slowly (since M4,5 are mostly in subthreshold region) and reduces the commonmode voltage (Vcml = 0.5 ×[VO1+ + VO1−]) to provide a strong drive for the input pMOS latch stage.In the second stage the cross-coupled circuit increases the differential voltage (Vidl =[VO1+−VO1−]) slowly to provide a strong drive for the input n-MOS latch stage.

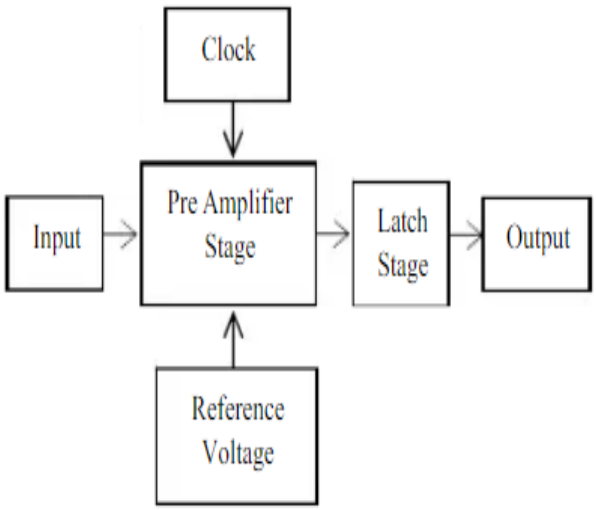

Fig:3 Pre amplifier and latch stage block diagram

In fig.3,it shows the over all block diagram of the pre-amplifier and latch circuit. It consisits of input, pre-amplifier block, referencevoltage, clock signal, latch stage and output blocks.

The very last output of comparator depends upon at the polarity of the clock signal block. By converting the clock signal of the output of comparator may vary in line with the inputs respectively.

In fig.4, the structure of the comparator which consists of ranges are the selection levels and maintain stages. Comparator operation has three exceptional levels. Phase 1 is reset, phase 2 is selection or assessment and phase 3 is preserve section which stores the evaluation result for a specific time.

In reset segment while high, transistors M9 and M10 are off even as M7 and M8 are on. As a result, nodes Vi-n and Vi-p are shorted to ground through M7 and M8.

In this phase, input signals Vi-n and Vi-p sound the node voltages Vo-n and Vo-p. Considering the sign tiers of Vip - Vref+ and Vin – Vref-, output voltages Vout+ and Vout- may have different speeds. Power is the main limitation of designing a dynamic latch comparator.. As a result, Power can be reduced with pre-amplification stage during the design process before the latch[12].Off set voltages, one which processes the edge voltage of the n-MOS transistor in advance connects to Vdd through move-coupled inverters and different node may be connected to ground.As end result, one of the Vo-p and Vo-n are related to Vdd or Gnd.

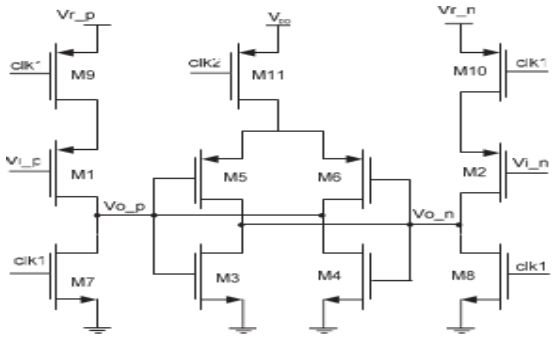

Fig:4 The struc ture of the basic dynamic comparator.

After this section (evaluation time), input signal fluctuations cannot exchange the output signal except output nodes are reset for the next comparison.

In this shape, input offset can be managed through the timing of the clock pulse clk2. In this shape, electricity is dissipated in hold phase while CMOS inverters do not want power consumption at this segment[13]. First level has strength dissipation with enhancing the structure, power consumption in hold phase can be reduced.

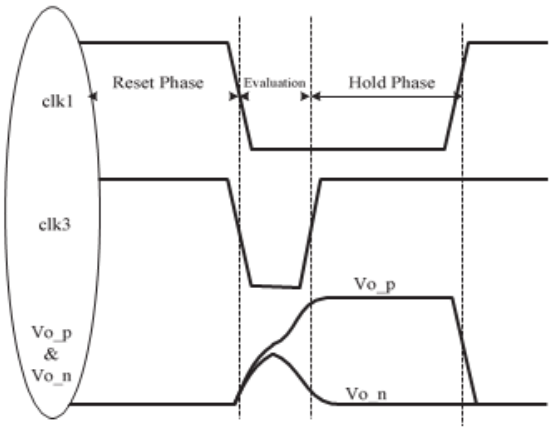

Fig:5 o/p waves of Fig.4

In this research, a fully differential dynamic latch comparator is presented inspired by the design of ‘Lewis-Gray’ dynamic comparator, which is based on cross-coupled differential pairs[11].

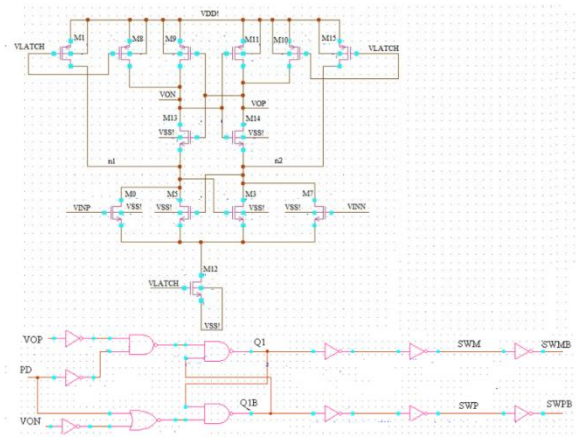

Fig:6 Lewis-Gray dynamic comparator.

The dynamic latch comparator shown in figure is most widely used because it has many advantages such as high-speed, zero static-power consumption, high input-impedance and full swing output.

During the pre-amplification phase both the output nodes are charged to power supply voltage and during the evaluation phase the output of the comparator depends on the differential input.

In the second stage the cross-coupled circuit increases the differential voltage (Vidl =[VO1+−VO1−]) slowly to provide a strong drive for the input n-MOS latch stage.

The main advantage of this comparator is, it will deliver larger load currents and operate at lower power. The most downside of this comparator is, it takes long to reset the output nodes to produce voltage that slower the method of comparison that successively limits the speed of comparator.

To avoid this we tend to use cross coupled transistors within the pre amplification stage to hurry the method.

In the second stage the cross-coupled circuit will increase the differential voltage (Vidl =[VO1+−VO1−]) slowly to produce a powerful drive for the input n-MOS latchstage.

III. METHODOLOGY

The proposed comparator shown in fig(3), is the combination of n-MOS latch and cross coupled pre amplifier .We propose a dynamic latch comparator with a separated input stage and two cross-coupled pair (nMOS and pMOS) stages in parallel instead of stacking them on top of each other as the previous works, as shown in Figure 1.

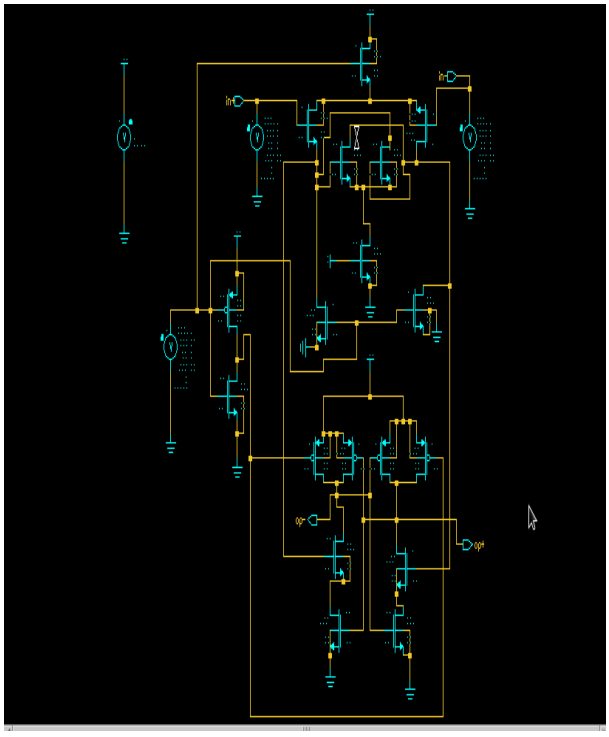

Fig:7 proposed comparator

This circuit topology makes it suitable to work at very low supply voltage and achieve faster speed compared to the conventional dynamic comparators at low supply voltage. And it is a fully dynamic circuit without any static power consumption.At the reset phase, when the clk is ‘1’then pre-amplification stage will activate and the voltage will drive to latch. At this stage the parasitic capacitors will charge. When clk=’0’,the evaluation phase will activate or start. During this phase the voltage will increase due to cross coupled transistors.When clk=’1’,the input voltages will charge the capacitors and transfer it to latch. Due to cross coupled circuit the power will be reduced. In the latch stage the output of the capacitors are given as input to the transistors of n-MOS latch.

The voltage difference at the first stage outputs has a profound effect on latch initial differential output voltageand consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparatorTo reduce power,the pre-amplification stage and latch stage are controlled with two different clock signals

IV. SIMULATION RESULTS

The design is simulated 0.18µm CMOS Technology in mentor graphics tools.

Finally simulation results of the comparator are shown below.

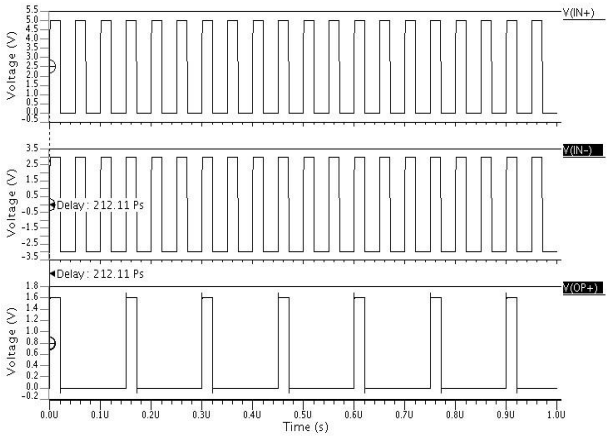

Fig:8 output waveforms for proposed circuit.

when a differential signal is applied as input to the latched comparator. is shown. The total propagation delay of the proposed comparator can be measured in mentor graphics.

V. CONCLUSION

In the proposed comparator the nMOS latch and nMOS preamplifier with cross coupled transistors are used ,to provide enough pre-amplification gain .

To reduce power special clock circuit is designed. We designed preamplification and latch stage using nMOS because inherent superiority over pMOS . This will result in high speed of the circuit.

FUTURE SCOPE

In the future we can try to further reducing the size of the comparator and subsequentreduction in power consumption and delay.

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