International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249-8958 (Online), Volume-9 Issue-2, December, 2019

Frequency Scaling Based Power Efficient Current Source Design on FPGA

Amanpreet Kaur, Keshav Kumar, Vidyotma Gandhi, Amanpreet Sandhu, Bishwajeet Pandey

Abstract: ***Power deficiency is one of the major problems that the whole world is facing now. This is happening because of the immense increase in the world's population and the global increase of industrialization. So in order to minimize the consumption of power, an energy efficient current source is designed with the help of Field Programmable Gate Array (FPGA). This work gives light on how the power variation takes place in a current source with an increase in frequency value. In this research work, the current source is implemented on 28 nanometers (nm) Airtx-7 FPGA. The work is demonstrated on Xilinx 14.1 ISE simulator. VHSIC Hardware Description Language (VHDL) is used for writing the code of current source. The frequency of current source with Airtx-7 FPGA is increased from 100MHz to 5GHz. It is analyzed that the total power consumption is less as the value of frequency is low. So it is always advisable to operate the device at a lower frequency range in order to save more energy.***

Keywords : Field Programmable Gate Array (FPGA), Artix-7, Frequency, Power and Current source.

I. INTRODUCTION

The world is having a limited amount of natural resources for power generation. The time era which is going now is facing a huge problem of energy and power crisis across the globe. The major cause of this deficiency is an increase in population and industrialization which is growing day by day in the whole world [1]. Therefore in order to overcome the problem of energy and power crisis, the concept of green communication and power-efficient devices have gained a lot of attention in today's world [2-3]. This work is done in order to promote green communication and to design power-efficient devices. In this work a power-efficient current source circuit is designed and its results are analyzed in Artix-7 FPGA when the frequency makes a transition from 100MHz to 5GHz which is shown in figure 1.The current source is one of the basic electronic circuits, that's the main work is to deliver or absorb electric current and this current must be independent of the voltage applied across the current source. It supplies the constant current to the circuit, which is independent of the voltage developed across the terminals [4].

Figure 1 Range of frequencies.

II. RELATED WORK

Earlier researchers have used FPGA to control Multilevel Current Source Inverter (MCSI) [5]. The results of the experiment are analyzed in MATLAB. With the help of Digital Signal Processing and FPGA authors have presented a current controller for voltage source inverter [6]. The authors designed a real-time maximum power point controller for photovoltaic system using FPGA. The results are analyzed on Xilinx simulator on Virtex-II FPGA [7]. Researchers used Fast Fourier Transform (FFT) [8] algorithm on FPGA to design voltage and current dual-drive systems for electrical impedance tomography. Researchers used FPGA to analyze three-phase distribution for load compensation to reduce supply power factor [9]. Authors used FPGA for real-time simulation for power converters and electric machines [10]. FIR filter using FPGA [11] for green communication is designed. Authors used Kintex, an ultra-scale FPGA to study the power consumption of FIR filter by changing its IO standards. A solution is given by authors to find an operating condition for RAM so that it consumes the least amount of power [12]. The different frequencies at which this experiment is performed lies in the range of 0.6 GHz to 1.5 GHz on Xilinx 12.1 simulator. The authors designed a power-efficient RAM using 28nm FPGA for spacecraft [13]. In this work authors worked on IO standards of FPGA to study the power consumption of Random Access Memory (RAM). By using Virtex-6 FPGA, authors interfaced RAM to minimize its power consumption [14]. For real-time simulation photovoltaic modules are designed by the authors with the help of FPGA [15]. Researchers worked on designing a low voltage and low power VLSI circuit on FPGA [16]. They used Virtex 6 FPGA and RAM-UART to analyze power reduction. Authors designed an energy-efficient Arithmetic Logic Unit (ALU) by varying the frequency of FPGA which reduces clock and dynamic power consumption [17]. A low power UART is developed by authors by varying the output load capacitance over Virtex-6 FPGA [18]. A power-efficient FIR filter is designed by authors for wireless network sensors as pre signal processing step using FPGA [19].

Revised Manuscript Received on December 30, 2019.
* Correspondence Author
Amanpreet Kaur*, Chitkara University Institute of Engineering & Technology, Chitkara University, Punjab, India (email: amanpreet.kaur@chitkara.edu.in)
Keshav Kumar, Chitkara University Institute of Engineering & technology, Chitkara University, Punjab, India, (keshav.kumar@chitkara.edu.in)
Vidyotma Gandhi, Chitkara University Institute of Engineering & technology, Chitkara University, Punjab, India, (vidyotma.gandhi@chitkara.edu.in)
Amanpreet Sandhu, Chitkara University Institute of Engineering & technology, Chitkara University, Punjab, India, (amanpreet.sandhu@chitkara.edu.in)
Bishwajeet Pandey, Center of Energy Excellence, Gyancity Research Lab, Motihari, Bihar, India (email: gyancity@gyancity.com)

An energy-efficient solar charge sensor is designed on FPGA is designed by authors. Frequency is scaled for from 0.01 GHz to 100 GHz [20]. An energy-efficient instruction register is designed by authors for promoting the ideas of green communication [22]. A power-efficient control unit is designed by authors on FPGA. In this work frequency of the FPGA is changed to optimize the power consumption [23]. With the help of different families of FPGA, a low power UART is designed by authors [24]. Effect of different logic families of FPGAs is observed on UART by the authors [25]. There is an extensive literature provided on different types of energy efficient

III. EXPERIMENTAL SETUP

The research work is implemented on Xilinx 14.1 ISE simulator for Artix-7 FPGA, and the code of the current source is written in the VHDL module. The schematic obtained from the simulator has three inputs which are clock, reset and offset value of 28-bits. There are six output wires which are as follows: -

- ✓ 8 bits offset address1
- ✓ 8 bits offset address2
- ✓ 9 bits offset data1
- ✓ 5 bits offset data2
- ✓ Offset calibration finished
- ✓ Offset.

The airflow of FPGA is 250 Linear Feet per Meter (LFM), while the ambient temperature is 25(°C). The Register Transfer Level (RTL) schematic of the current source achieved from the Xilinx design suite is represented in figure 2.

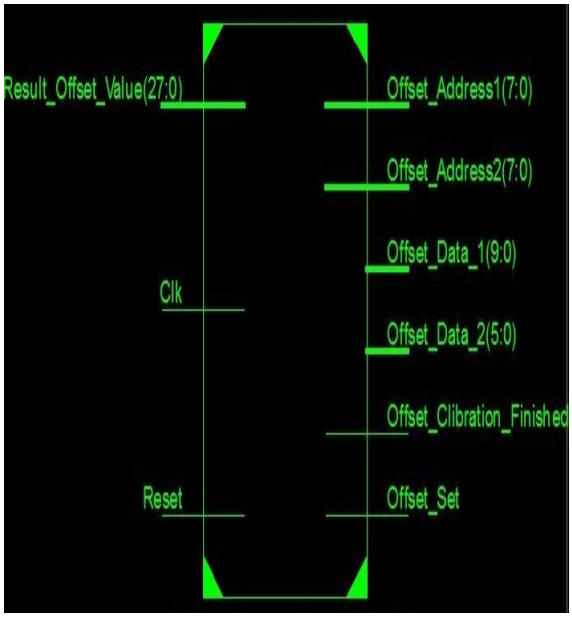

Figure 2 RTL Schematic of the current source.

IV. POWER ANALYSIS

There are two types of power for which the result has been calculated.

- ✓ Static Power– Static power is that power which is consumed when there is no supply of current. Example- Leakage Power (Lek. P) [21].
- ✓ Dynamic Power- This is the power consumed when the inputs to the circuit are active. Example – Clock Power (C.P), Signal Power (S.P), Logic Power (L.P), and Input/Output power (I/O. P).

In order to analyze the effect of different frequencies on static and dynamic power consumption of current source, the frequency range is scaled from 100MHz to 5GHz. The power analyses at different frequencies are as follows:

A. Power Analysis for 100MHz frequency.

The frequency of FPGA is tuned to 100MHz, then the S.P, L.P and I/O. P. are 0.001W. The power consumption of C.P and Lek.P is 0.001 W and 0.042 W respectively. Therefore the power consumption of FPGA at 100MHz frequency becomes 0.044 W. The different power distribution at 100 MHz is described in figure 3.

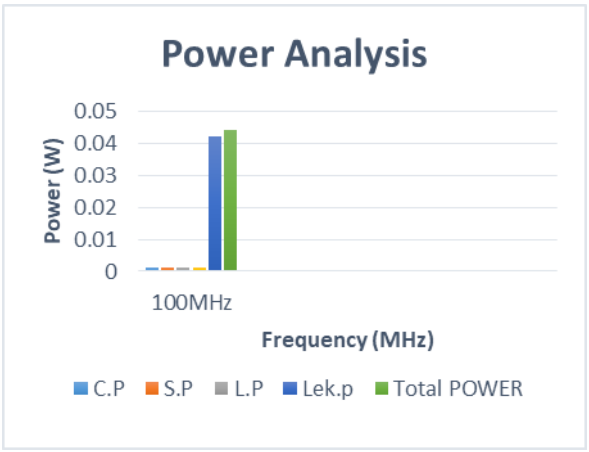

Figure 3 Power Distribution at 100MHz frequency.

B. Power Analysis for 500MHz frequency.

When the frequency is tuned to 500MHz, L.P consumption is 0.001W, on the other hand, C.P contributes 0.003W, S.P contributes 0.001W, I/O power contributes 0.002W and Lek.P contributes 0.042W. The total power consumption of FPGA is 0.048W as shown in figure 4.

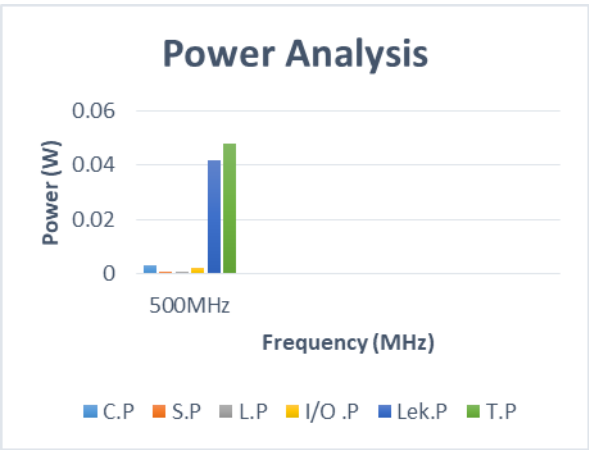

Figure 4 Power Distribution at 500MHz frequency.

C. Power Analysis for 1GHz frequency.

At the frequency of 1GHz, the Total Power (T.P) consumption is 0.054W which is sum total of C.P that is 0.006W, S.P that is 0.001W, L.P that is 0.001W, I/O power that is 0.004W and Lek.P that is 0.042W respectively.

For 1GHz frequency, logic power consumption is 0.000W. The power analysis graph is shown in figure 5.

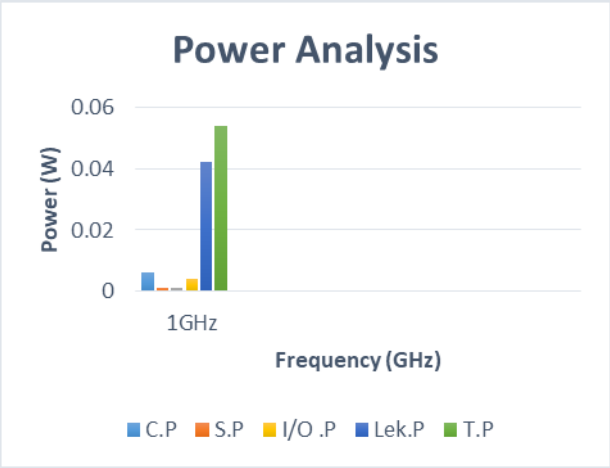

Figure 5 Power analysis graph for 1GHz frequency.

D. Power Analysis for 3GHz frequency.

When the frequency is tuned to 3GHz, L.P consumption is 0.000W. The T.P consumption is 0.077W which is sum total of C.P, S.P, L.P I/O power and Lek.P whose values are 0.017W, 0.004W, 0.001, 0.013W and 0.042W respectively. The power analysis for frequency 3GHz is shown in figure 6.

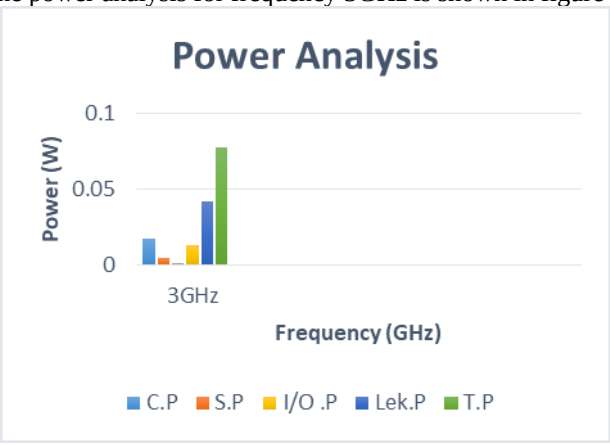

Figure 6 Power analysis graph for 3GHz frequency.

E. Power Analysis for 5GHz frequency.

When the frequency is tuned to 5GHz, the T.P consumption is the sum-up of all the on chips power which is fabricated on FPGA. At 5GHz frequency the C.P is 0.028W, L.P is 0.001W, S.P is 0.007W, I/O power is 0.222W and Lek.P is 0.043W, which sums up to the T.P consumption of 0.101W. Figure 7 represents the power distribution for 5GHz frequency.

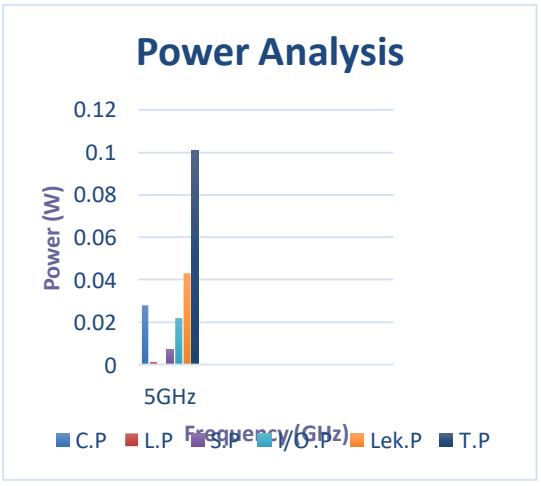

Figure 7 Power analysis graph for 5 GHz frequency.

V. RESULT ANALYSIS

It is observed from power analysis that the T.P consumption of the current source with Airtx-7 FPGA increases as there is increase in the frequency value. The T.P consumption increases by 9.09%, when frequency is changed from 100MHz to 500MHz. When frequency is tuned to 1GHz from 100MHz the power is increased by 22.73%. The T.P consumption is increased by 75% when frequency is tuned to 3GHz from 100MHz. When frequency changes to 5GHz from 100MHz total power is increased by 129.55%. The comparison of T.P consumption for different frequency ranges is represented in figure 8.

Figure 8 Total Power comparison.

VI. CONCLUSION

This research work details the implementation of current source circuit on Artix-7 FPGA. The research work is performed on Xilinx 14.1 Design suite. It is evident that the power consumption increases as the value of frequency gets increased. Therefore it is concluded that the current source design is most power-efficient at 100MHz frequency. So it is always advisable to operate the device at a lower frequency range in order to save more energy.

FUTURE SCOPE

This work highlights about the implementation of current source design on Artix-7 FPGA. New researchers can implement this design on other FPGAs like Kintex, Zynq etc. for promoting the ideas of green communication. Not only current source design, other electronic circuits can also be implemented on FPGA, to achieve power-efficient devices. Another energy and power efficient techniques like voltage scaling, capacitance scaling and I/O standard scaling can be implemented on current source in order to contribute towards green communication since the whole globe is facing the problem of power crisis.

REFERENCES

1. www.conserve-energy-future.com/causes-and-solution-to-the-global-energy-crisis.php; Accessed on: 01/10/2019.
2. B. Pandey, B. Das, A. Kaur, T. Kumar, A.M. Khan, D.A Hussain. and G.S. Tomar, 2017. Performance evaluation of FIR filter after implementation on different FPGA and SOC and its utilization in communication and network. *Wireless Personal Communications*, *95*(2), pp.375-389.
3. Vereecken, Willem, Ward Van Heddeghem, Didier Colle, Mario Pickavet, and Piet Demeester. Overall ICT footprint and green communication technologies. In 2010 4th International Symposium on Communications, Control and Signal Processing (ISCCSP), pp. 1-6. IEEE, 2010.
4. www.electronics-tutorials.ws/dccircuits/current-source.html Accessed on: 06/10/2019.
5. Aguirre, Miguel Pablo, Laura Calvino, and Maria Ines Valla. "Multilevel current-source inverter with FPGA control." IEEE Transactions on Industrial Electronics 60, no. 1 (2012): 3-10.
6. Abu-Rub, Haitham, Jaroslaw Guzinski, Zbigniew Krzeminski, and Hamid A. Toliyat. "Predictive current control of voltage-source inverters." IEEE Transactions on Industrial Electronics51, no. 3 (2004): 585-593.
7. Mellit, A., H. Rezzouk, A. Messai, and B. Medjahed. "FPGA-based real-time implementation of MPPT-controller for photovoltaic systems." Renewable energy 36, no. 5 (2011): 1652-1661.
8. Khan, Shadab, Preston Manwaring, Andrea Borsic, and Ryan Halter. "FPGA-based voltage and current dual drive system for high frame rate electrical impedance tomography." IEEE transactions on medical imaging 34, no. 4 (2014): 888-901.
9. Kandadai, Venkatraman, Moorthi Sridharan, Selvan Manickavasagam Parvathy, Raja Pitchaimuthu, and Deepa Kurup. "Performance evaluation of FPGA-controlled DSTATCOM for load compensation." Arabian Journal for Science and Engineering 41, no. 9 (2016): 3355-3367.
10. Herrera, Luis, Cong Li, Xiu Yao, and Jin Wang. "FPGA-based detailed real-time simulation of power converters and electric machines for EV HIL applications." IEEE Transactions on Industry Applications 51, no. 2 (2014): 1702-1712.
11. B. Pandey, N. Pandey, A. Kaur, D.M. A. Hussain, B. Das, and G. S. Tomar. "Scaling of Output Load in Energy Efficient FIR Filter for Green Communication on Ultra-Scale FPGA." Wireless Personal Communications (2018): 1-14.
12. R. Sharma, B. Pandey, and V. Sharma. "Analysis of frequency effect on variegated RAM styles and other parameters using 40 nm FPGA." In To, Be Send To a Conference. 2018.
13. K. Kalia, B. Pandey, and D. M. A. Hussain. "SSTL based thermal and power-efficient RAM design on 28nm FPGA for spacecraft."In 2016 International Conference on Smart Grid and Clean Energy Technologies (ICSGCE), pp. 313-317. IEEE, 2016
14. Bansal, Meenakshi, Neha Bansal, Rishita Saini, Bishwajeet Pandey, Lakshay Kalra, and DM Akbar Hussain. SSTL I/O Standard-based environment-friendly energy-efficient ROM design on FPGA. 3rd International Symposium on Environmental Friendly Energies and Applications (EFEA), pp. 1-6. IEEE, 2014.
15. E. Koutroulis, K. Kalaitzakis, and V. Tzitzilonis. Development of an FPGA-based system for real-time simulation of photovoltaic modules. Microelectronics journal 40, no. 7 (2009): 1094-1102.
16. B. Pandey, and R. Kumar. "Low voltage DCI based low power VLSI circuit implementation on FPGA." In 2013 IEEE Conference on Information & Communication Technologies, pp. 128-131. IEEE, 2013.
17. B. Pandey, J. Yadav, M. Pattanaik, and N. Rajoria. "Clock gating based energy efficient ALU design and implementation on FPGA." In Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on, pp. 93-97. IEEE, 2013.
18. P. R. Singh., B. Pandey, T. Kumar, T. Das, and O. J. Pandey. "Output load capacitance-based low power implementation of UART on FPGA." In *2014* International Conference on Computer Communication and Informatics, pp. 1-4. IEEE, 2014.
19. A. Kaur, and S. Singh. "Wireless Sensor Network-Specific Low Power FIR Filter Design and Implementation on FPGA.
20. A. Singla, A. Kaur, and B.Pandey. "LVCMOS based energy-efficient solar charge sensor design on FPGA." In Power Electronics (IICPE), 2014 IEEE 6th India International Conference on, pp. 1-5. IEEE, 2014
21. https://semiengineering.com/knowledge_centers/low-power/low-power-design/power-consumption/ Accessed on: 10/10/2019.
22. S. M T. Siddiquee, K. Kumar, B. Pandey, A. Kumar," Energy Efficient Instruction Register for Green Communication", International Journal of Engineering and Advanced Technology (IJEAT), Volume-8, Issue-2S2, January 2019.
23. K. Kumar, S. Ahmad, B. Pandey, A. K Pandit, D. Singh, D.M A.Hussain "Power Efficient Frequency Scaled and Thermal-Aware Control Unit Design on FPGA", International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol. 8, Issue-9S2, July 2019.
24. K.Kumar, A.Kaur, B.Pandey, and S. N. Panda. "Low Power UART Design Using Different Nanometer Technology-Based FPGA." In 2018 8th International Conference on Communication Systems and Network Technologies (CSNT), pp. 1-3. IEEE, 2018.
25. K.Kumar, A. Kaur, S. N. Panda, and B. Pandey. "Effect of Different Nano Meter Technology-Based FPGA on Energy Efficient UART Design." In 2018 8th International Conference on Communication Systems and Network Technologies (CSNT), pp. 1-4. IEEE, 2018

AUTHORS PROFILE

Amanpreet Kaur is a leading young scientist in the field of energy efficient designs and devoted her life to solve the problem of energy crisis. She has received B.Tech. in Electronics and Communication Engineering(ECE) from Kurukshetra University in 2012 and M.E.(ECE) from Chitkara University in 2016. She worked as a Project Trainee at CSIR-CSIO. She is pursuing Ph.D. in ECE and working on the projects of Augmented Reality /Virtual Reality based Engineering Education Systems. At present she is working as a Research Scholar in Chitkara University, Punjab, INDIA and she has also associated as a Young Scientist with Gyancity Research Labs, India. She has published a patent for Energy Efficient Unicode Reader Design on FPGA. She has also been authored and coauthored in 35 national and international SCI and Scopus indexed Research publications, 2 DRDO Book Chapters in area of low power VLSI design and Energy Efficient Green Computing, Augmented/Virtual Reality. She was also a Reviewer and TPC member of 11 International Conferences held across the globe. She is also working in collaboration with department of energy technology of Aalborg University, Denmark. The prime objective of her research is to decrease the power consumption of electronic device and appliances without increasing the power generation. Her aim is to create Augmented/Virtual labs in engineering education in order to enhance the interaction and spatial skills amongst the engineering students in a way to reduce the cognitive load. She has also got the Lifetime Membership of Institution of Engineers (IEI), INDIA and Professional Membership of Institute of Electrical and Electronics Engineers (IEEE).

Keshav Kumar is pursuing his Master of Engineering in the field of Cyber Security and FPGA from Chitkara University, Punjab, India. He did his B.Tech in Electronics and Communication Engineering from Rajasthan Technical University, Kota, India. His area of interest is the implementation of security algorithms on FPGA, power-efficient device on FPGA and green communication. He has worked with researchers of three different countries in the field of Low Power VLSI design on FPGA and Energy Efficient devices for Green Communication.

Vidhyotma Gandhi is working in Chitkara University, Punjab as Assistant Professor, Research. She has worked as an Assistant Engineer in Punjab Communication Ltd. Mohali for 17 years and has teaching experience of 12 Years. She has completed her Masters in Computer Applications from Punjab Technical University, Jallandhar. M.Tech in CSE from Chitkara University, Punjab and is currently pursuing her Ph.D. in Computer Science Engineering from Chitkara University, Punjab.

Amanpreet Sandhu received the PhD degree in electronics and communication engineering from Chitkara University, Punjab, India, in 2019 and M. Tech degree from Punjab technical University, Punjab, India in 2010. She is currently an Associate Professor with the Department of electronics and Communication Engineering, Chitkara University, Punjab, India. Her research interests include Nano Electronics, Micro Electronics, VLSI, Cadence, Xilinx, wireless and Adhoc Networks.

Dr Bishwajeet Pandey is a co-founder of Gyancity Research Lab. Gyancity Research Lab organizes three conferences (ICGCET.ORG, RTCSE.ORG, IMCES.TECH) across the globe. He has completed his PhD in CSE from GSSI, Italy. He has worked as Asst. Professor in Department of Research at Chitkara University, Junior Research Fellow (JRF) at South Asian University. He has completed Master of Technology (IIIT Gwalior) in CSE with Specialization in VLSI, Master of Computer Application, R&D Project in CDAC-Noida. He has authored and coauthored over 135 paper available on his Scopus Profile:https://www.scopus.com/authid/detail.uri?authorId=57203239026. He has 1345 Citation according to his Google Scholar Profile: https://scholar.google.co.in/citations?user=UZ_8yAMAAAAJ&hl=ens