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Performance Examination of SEPIC Based Hybrid Cascaded Single-Phase Multilevel Inverter

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Abstract*: *In the present scenario, reduced part count(RPC) multilevel inverters are become popular compared to traditional multilevel inverters(MLIs). This is mainly due to reduced size and cost and alleviates the issues of more passive components, flying capacitor voltage balancing issues and the requirement of complex switching schemes. Also, the RPC is getting attraction for various industrial and transportation applications. Therefore, in this paper, a novel 17 level inverter is proposed by cascading MLIs with the reduced part count. The complete operation, switching schemes and output are presented to evolve the performance under steady-state conditions using MATLAB software.

Keywords : Multilevel inverter, DC-DC boost converter, sinusoidal pulse width modulation (SPWM);

I. INTRODUCTION

Renewable power generation is getting popularity for distributed generations due to their benefits of reduced system installation cost and environmentally friendly nature. However, interfacing renewable energy sources demand suitable power conditioner. Single state DC/AC converter becomes popular and higher efficiency[1-5]. However, regulation in supply is critical, so these leads to develop an intermediate boost converter to enhance the voltage gain. However, increasing voltage gain can be achieved at high duty cycle leads to more looses which degrade the efficiency of the system. Recently, MLIs are promising for power generation using renewable applications with the reduced part count. Whereas the use of conventional MLIs demands more clamping diodes, flying capacitor, voltage balancing issues and more complex in control for higher level[5-9]. In this context, RPC-MLIs are getting popularity to enhance the output levels with a better quality of output voltage waveforms. The various RPC-MLIs are described in the literature [10] is for seven-level operations only. Increasing level with lower switches will enhance the performance of the system. Therefore, in this paper performance evaluation of a novel cascaded multilevel inverter is considered for the study using MATLAB software. The proposed model is capable of 17 level generation with the reduced part count. a front end boost converter is also used to balance the dc-link and the simulation results are given for steady-state conditions.

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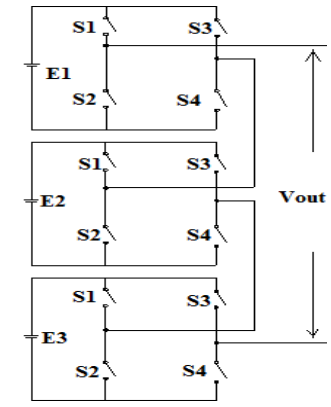
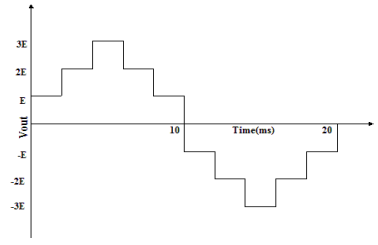
II. CASCADED H-BRIDGE MULTILEVEL INVERTER

Cascaded H-Bridge (CHB) is the most popular one among conventional MLIs. Whereas Diode-clamped and Flying capacitor MLIs have the problem for increase level. CHB is the best model for increased level of generations. It is capable to generate 2N+1 level for cascading of N modules. However, it demands identical dc sources for each H-Bridge circuits and more semiconductor devices for more output levels. Fig.1 depicts the seven-level CHB and its expected output voltage waveform.



(a)



(b)

Fig. 1(a) Cascaded 7-level H-Bridge inverter, (b)Voltage Output of Cascaded 7-level H-bridge inverter.

A. Novel H-Bridge Inverter

A novel H-bridge inverter is developed by connecting a bidirectional semiconductor device with diodes in between the H-bridge and the DC input. The single unit is capable to produce 5 level AC output. The foremost advantage of the novel H-bridge inverter compared to a conventional CHB MLIs is the reduction of the number of semiconductor devices. For a CHB multilevel inverter to generate a 5 level AC output, 8 switches are required. This results in increased efficiency and reliability of the system and reduced in device count.

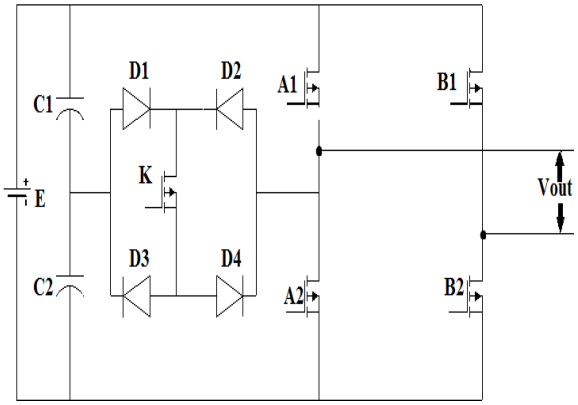


Fig. 2. Novel H-Bride inverter

Table 1: Switching Pattern of Novel H-bridge

Output voltage	K	A1	A2	B1	B2
2E	off	on	off	off	on
E	on	off	off	off	on
0	off	off	on	off	on
-E	on	off	off	on	off
-2E	off	off	on	on	off

B. Cascaded Novel H-Bridge

Here two novel H-bridge circuits are wired to produce various output levels such as 9, 13, and 17 by varying the magnitude of the input DC sources with reduced device count is the foremost advantage of this configuration. The different combinations for the output level generations are depicted in tables 1-5.

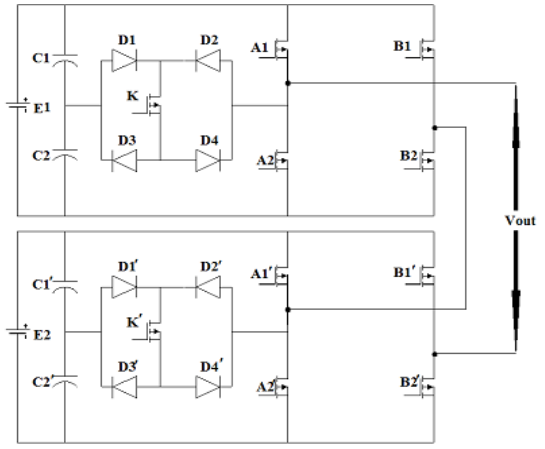


Fig.3 Cascaded Novel H-Bridge-Bridge inverter

Table 2: Voltage ratio of H-Bridge and Voltage levels can be obtained

E1	E2	Voltage Output
E	0	E
2E	0	2E
E	2E	3E
2E	2E	4E
E	4E	5E
2E	4E	6E
-2E	-4E	-6E
-E	-4E	-5E
-2E	-2E	-4E
-E	-2E	-3E
-2E	0	-2E
-E	0	0
0	0	0

Table 3: Voltage in each level of both novel H-bridge for 9 level inverter.

E1	E2	LEVELS
E	E	9
E	2E	13
E	3E	17
E	4E	21
E	5E	25

Table 4: Voltage in each level of both novel H-bridge for 13 level inverter.

E1	E2	Voltage Output
E	0	E
2E	0	2E
0	3E	3E
E	3E	4E
2E	3E	5E
0	6E	6E
E	6E	7E
2E	6E	8E
-2E	-6E	-8E
-E	-6E	-7E
0	-6E	-6E
-2E	-3E	-5E
-E	-3E	-4E
0	-3E	-3E
-2E	0	-2E
-E	0	-E
0	0	0

Table 5: Voltage in each level of both novel H-bridge for 17 level inverter.

E1	E2	Voltage Output
E	0	E
E	E	2E
E	2E	3E
2E	2E	4E
-2E	-2E	-4E
-E	-2E	-3E
-E	-E	-2E
-E	0	-E
0	0	0

C. Sepic Converter

In this study, the sepic converter is taken as front end converter to regulate the desired primary voltage and simple control scheme is built using PI converter are shown in Fig. 4 (a) and (b). Generally, it consists of a simple inductor and capacitors and one semiconductor device. Sepic is capable to boost the desired voltage from the input by sensing the voltage. The selection of design parameters is computed using the following equations [10].

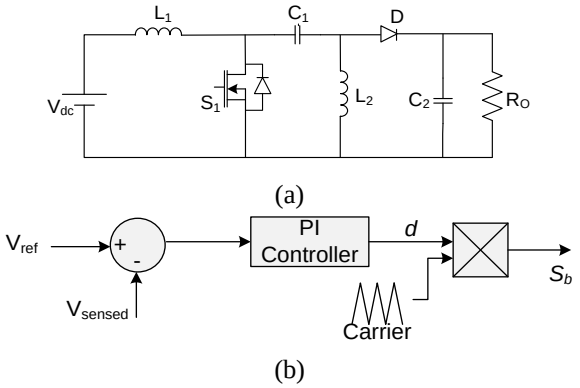


Fig. 4 (a) Sepic converter, (b) Closed loop scheme

$$\frac{V_o}{V_{in}} = \frac{D}{(1-D)} \quad (1)$$

$$L = \frac{DV_{in}}{f_s \Delta I_L} \quad (2)$$

$$C = \frac{DV_{dc}}{Rf_s \Delta V_C} \quad (3)$$

D. Proposed Topology

Fig. 5 shows the proposed topology using a sepic converter as front end converter with two cascaded five-level t-type inverters with the auxiliary circuit. The proposed circuit is capable for maximum 25 level output by proper selection of the input voltages using a multi-winding transformer with proper turns ratio selection. The single unit of five-level t-type inverter can produce 2E to -2E level with intermediate steps of E, 0 and -E voltage levels. Whereas the cascaded circuit is capable to produce 25 levels for a different combination of input voltages as discussed above.

E. PWM Technique

A simple sinusoidal pulse width modulation scheme(PWM) is used for the production of the various signal of the semiconductor devices. Sine PWM is simplest among the other PWM of State vector PWM, and Selective Harmonic Elimination PWM technique. It requires n-1 carrier signals to produce n-level output waveforms. To limit the number of carriers, a new PWM technique using carriers have been presented in this paper. This implemented jointly with a single carrier with digital encoding methods.

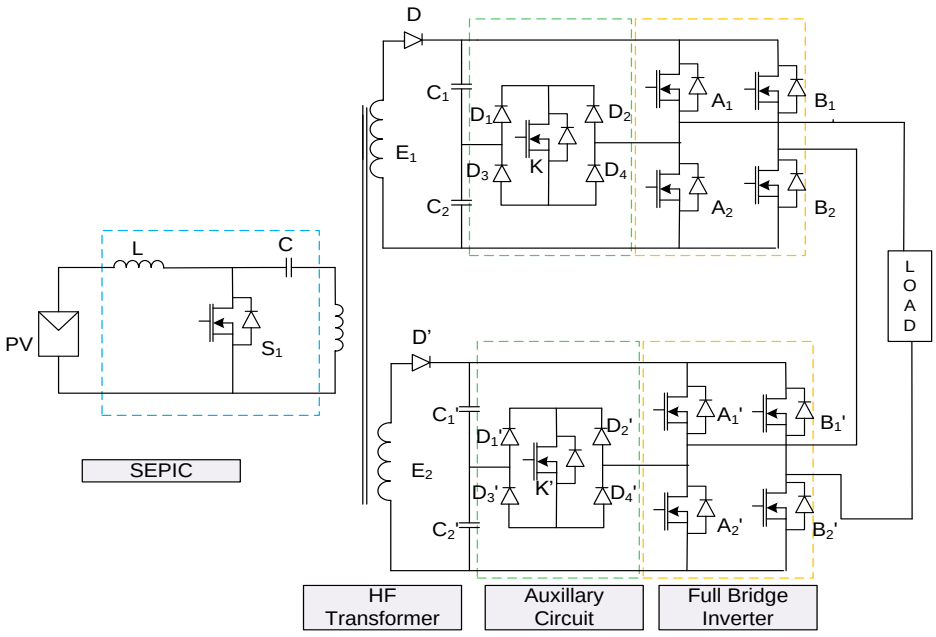


Fig. 5. Proposed topology.

Logical operation is implemented using various gates circuit to produce the pulses for all the semiconductor devices. For example, one t-type converter takes 5 level operation with the voltage levels of 2E, E,-E, -2E for both the units 8 samples of voltage can be produced. so three signals of 50Hz, 100Hz, and 200Hz are used such as A, B, and C is as follows. Here A, B and C are the various inputs of the encoder and P1 to P8 are the output of the encoder.

Table 6: 3*8 Encoder characteristic table

A	1	1	1	1	0	0	0	0
B	1	1	0	0	1	1	0	0
C	1	0	1	0	1	0	1	0
P1	1	0	0	0	0	0	0	0
P2	0	1	0	0	0	0	0	0
P3	0	0	1	0	0	0	0	0
P4	0	0	0	1	0	0	0	0
P5	0	0	0	0	1	0	0	0
P6	0	0	0	0	0	1	0	0
P7	0	0	0	0	0	0	1	0
P8	0	0	0	0	0	0	0	1

Let us take K switch of 5 level inverter. The switching sequence follows

K (binary)	1	0	0	1	1	0	0	1
K (waveform)								

If we perform logical OR operation of P1, P4, P5, P8 (refer table), we can get above Switching sequence for switch K. Likewise switching sequence for A1, A2, B1 and B2 are generated.

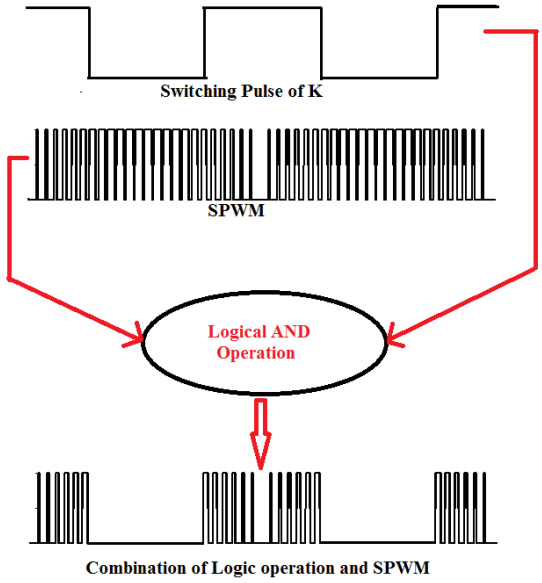


Fig. 6. Combination of Logic operation and SPWM

From Fig. 6 it can be observed that after the performance of logical operations, an AND operation is performed between the obtained switching sequence and the sinusoidal pulse width modulated signals to obtain the pulse width modulated signal for the switch K. similarly PWM signals for switches A1, A2, B1 and B2 can be attained.

III. SIMULATION RESULTS

In this study, the performance of the proposed sepic based t-type inverter is verified in MATLAB software for a resistive load of 1 kVA. The various parameter selected for the study is given in Table 7. Fig. 7 depicts the dc-link voltage of the t-type converter is well regulated by the sepic converter by adjusting the duty cycle separately, as per the desired value. Fig. 8 depicts the measured 17level output voltage waveform and their corresponding load current. To calculate the total harmonic distortion, FFT analysis is carried out and the measured THD of the simulated 17 level output voltage waveform is around 16.93% which is very lower compared to the conventional 3-level inverter. It is noticed that the results show a better performance. Further, the study shows that it can be effectively useful for PV applications.

Table 7: Parameters for 17 level inverter

Parameters	Specifications
V_{dc}	40V
F	2.5kHz
M1, M2	0.83, 0.5
C1	100 µf
C1, C2, C1',C2'	1000µf
L, L'	500µH
Load	1KVA

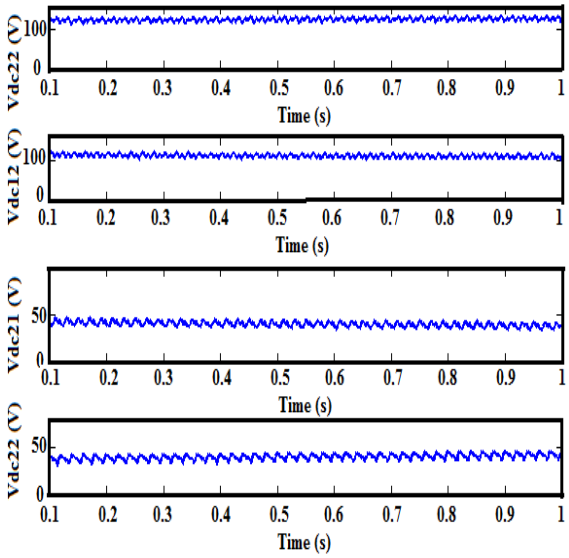


Fig. 7.Voltage output across dc-link of t-type converter

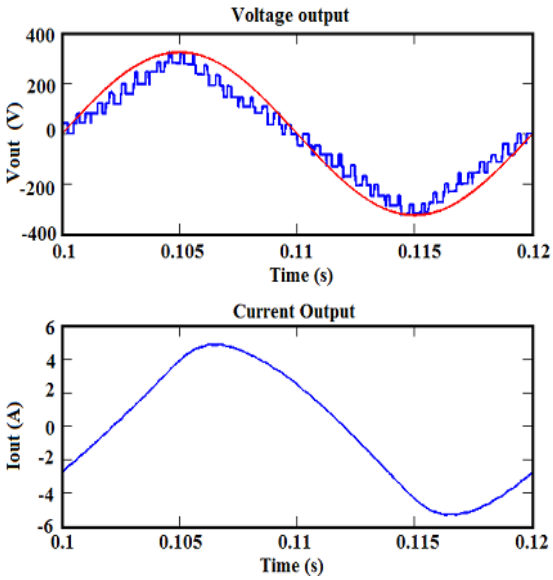


Fig. 8.Voltage output and current output of 17 level inverter

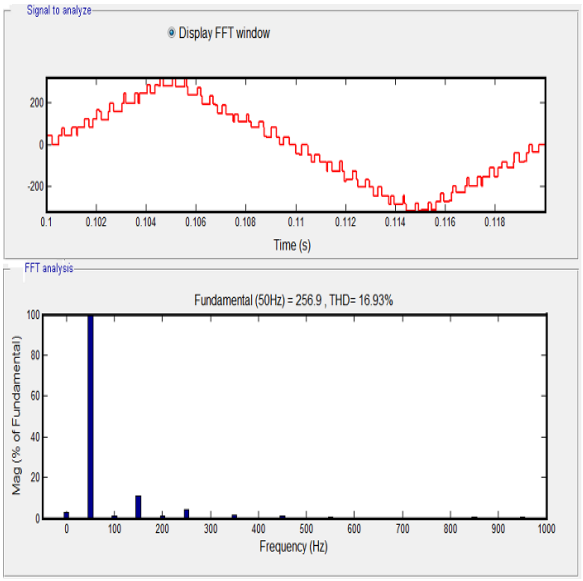


Fig. 9. FFT and THD analysis of 17 level inverter output voltage.

IV. CONCLUSION

In this study, a new structure of sepic based cascaded t-type multilevel inverter is presented. Sine PWM control with encoder logic operation is implemented to realize the 17 level output voltage waveforms in the MATLAB environment. The sepic converter effectively regulates the voltage and also performance of the converter under steady-state is presented. The proposed circuit is modular one and can be extended for further levels by cascading the H-bridge circuits.

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