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Current Starving CMOS On-Chip Oscillator for Elapsed Time Counter

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Abstract: ***This paper shows a structure of current starved inverter-based CMOS thyristor oscillator which is utilized to drive the counters that go about as a segment in the elapsed time counter. The performance of this oscillator is improved using a temperature independent biasing circuit that utilizes low power. The design incorporates utilization of trim bits at different process corners to shift the frequency. As the oscillator works with a battery supply, the output variations across supply are compromised. On – chip oscillator is implemented in a silicon area of 0.003064 mm² using UMC180 CMOS technology. Output shows a low power low frequency performance compared to a regular on- chip oscillator.***

Keywords—CMOS thyristor oscillator, trim bits, temperature independent biasing circuit, on-chip

I. INTRODUCTION

The demands of modern digital world are high performance in a compact design. The fundamental aspect is an accurate clock generation which is independent of disturbances caused by temperature & supply. Present generation in inclined towards compact devices which force the design of low power devices.

Oscillators are main component in many electronic systems. There are wide applications of oscillators like tuning circuits in audio video systems, microprocessor clock generation, mobile carrier synthesis with different designs & parameters. A high-performance robust CMOS oscillator design still poses challenges.

The oscillator proposed in this paper is used to count seconds when powered in an elapsed time counter. Continuous time tracking is done generally using a counter with an external crystal as input. On – chip oscillator is designed in place of external crystal to reduce the cost. The oscillator should be temperature & supply independent. Hence, the design should be low power & temperature independent.

The organization of rest of paper is as follows: Section II describes various architectures of CMOS oscillators. Section III gives the proposed design with principles. In Section IV, results are discussed with a conclusion in Section V.

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II. ARCHITECTURES

A. Ring Oscillator

Ring Oscillator contains of an odd number of CMOS inverters connected in cascade loop as shown in Figure 1. It is simple in design but has disadvantage that it occupies a large area. The frequency of operation is inversely proportional to the number of stages, so a lot of stages need to be cascaded which causes large variations by temperature & process corners.

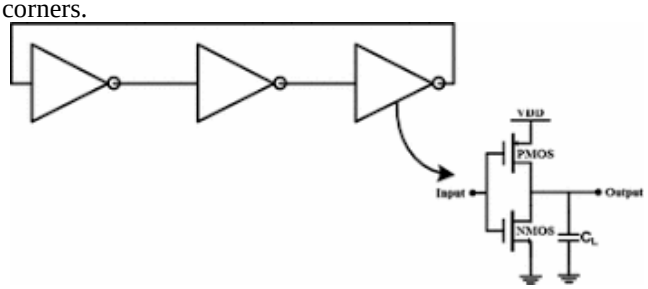

Fig1 :Ring Oscillator using CMOS inverters

B. CMOS Thyristor based Oscillator

A CMOS thyristor acts as a delay element. An odd number of CMOS thyristors when connected in cascade act as oscillator. The advantage of this circuit is it draws low power as it works on leakage currents. The disadvantage of this circuit is large frequency variation based on temperature.

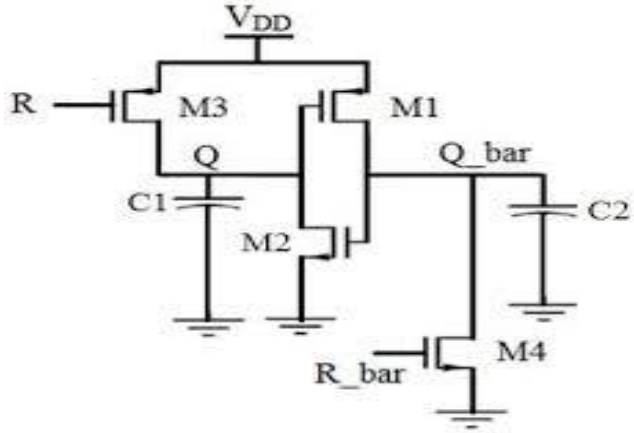

Fig 2. CMOS Thyristor Element

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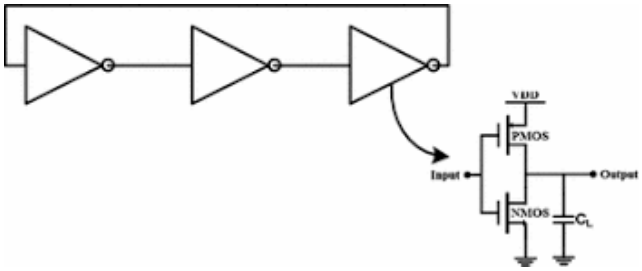

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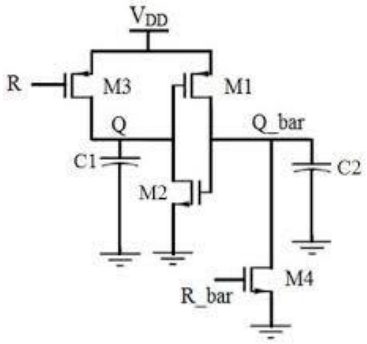

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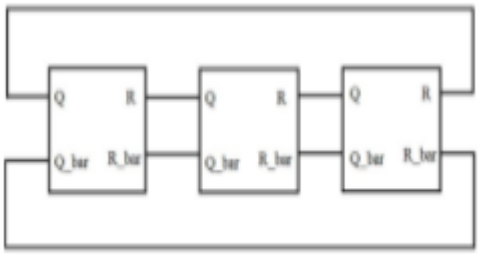

Fig 3. CMOS Thyristor based Oscillator

D. Current Starved Inverter based Oscillator

Adjustment of current course through a capacitor can be obliged by pace of charging & discharging. To diminish the current drawn by the circuit from supply extra MOSFETs with biasing at explicit voltage are stacked. This current starved inverter decreases the amount of stages. Subsequently the assortments as a result of progress of strategy corner can be decreased by tendency voltage change.

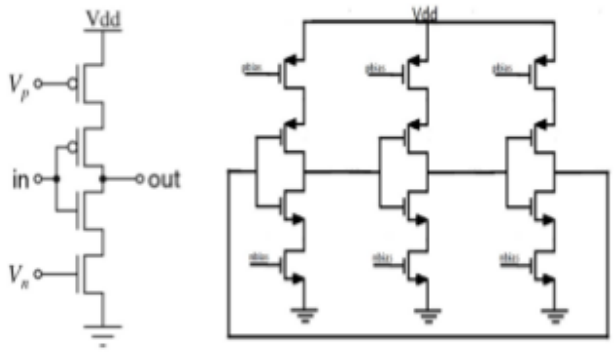

Fig 4. Current Starved Inverter based Oscillator

III. PROPOSED DESIGN

The essential piece of this arrangement is that it should draw less power & show low assortments in repeat of movements with respect to temperature. Thus, the arrangement includes a chain of current starved inverters with a temperature reimbursing biasing circuit & yield pads. The oscillator judgments are according to the accompanying:

Repeat – 22.937 – 42.598 kHz
Supply Current – 350nA
Commitment Cycle – 40-60 %
Power supply – 1.7-1.9V
Temperature go – 0-125oC
Spillage current – 100nA

A. Biasing Circuit

It is used for temperature pay in the current starved inverter plan. Biasing circuit controls the present course through oscillator plan which in this way settles the oscillator repeat. As the temperature extends, current stream in sub edge territory of MOSFET's fabricates exponentially in view of direct proportionality of edge voltage with temperature.

$$I_D = I_0 e^{\left(\frac{V_{GS}-V_T}{mKT}\right)} \quad (1)$$

To overcome the temperature dependence, in reverse association of current with temperature can be cultivated by stacking of MOSFETs in triode region.

$$I_D = \mu C_{ox}\left(\frac{w}{L}\right)\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (2)$$

I_D acts like a resistor varying linearly with V_{DS} given by

$$R_{on} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)} \quad (3)$$

If a single MOSFET is used the reduction in triode current on account of temperature isn't actually the pace of augmentation in subthreshold present as adaptability decreases with temperature. Thusly, different MOSFETs are stacked. A temperature free tendency can be delivered when increase in subthreshold current is reimbursed by decrease in triode current. Right when VT transversely over methodology corners is moved, an enormous change in caused in the biasing current which hence changes the oscillator repeat.

Trim bits are used to alter the biasing current stream. In the proposed structure, D0, D1, D2 are used as slicing commitments to move the repeat to typical estimation of action 32.768 KHz at different method corners.

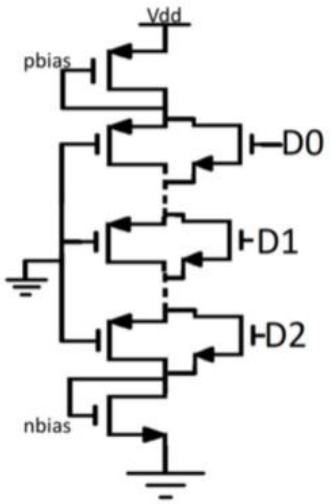

Fig 5. Biasing Circuit

B. Current Starved Inverter

The shortcoming of CMOs ring oscillator is it consumes high present & high power for high repeat timekeepers. By falling odd inverters which make ring oscillator we can deliver the regular 32.768 KHz repeat of action anyway the assortments in light of progress in process corner can't be assessed.

From now on, current starved inverter is used as the pace of charging & discharging through a capacitor can be changed by confining the present travel through it. The amount of stages in current starved oscillator are not as much as ring oscillator plan.

The current starved oscillator frequency is given by

$$f = \frac{1}{2N\tau_D} \quad (4)$$

Where N is number of delay cells in ring & $\tau_D$is delay time of each cell. 19 stages of current starved inverter cells are required to generate the 32.768 KHz.

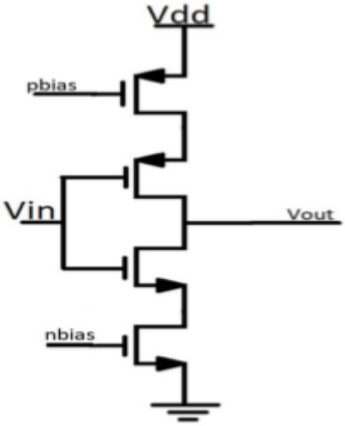

Fig 6. Current Starved Inverter

C. Output Buffer

As the current for charging & discharging of yield capacitor is limited by starving MOSFETs. This causes a colossal rising & fall delay in the current starved inverter-based oscillator. To achieve a grand rising & fall delay, the yield pad gives satisfactory proportion of current.

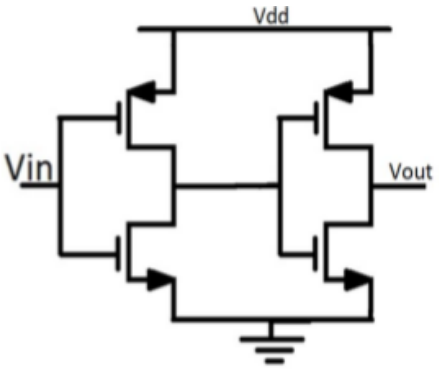

Fig 7. Output Buffer

D. Proposed Schematic of the design

Current starved inverters are fell in a shut circle. Biasing circuit added to the circle gives a biasing voltage. This voltage is then used in the current starved inverter hover by the desperate MOSFETs. Close to the end, a yield support is added to the inverter chain which gives a square wave yield.

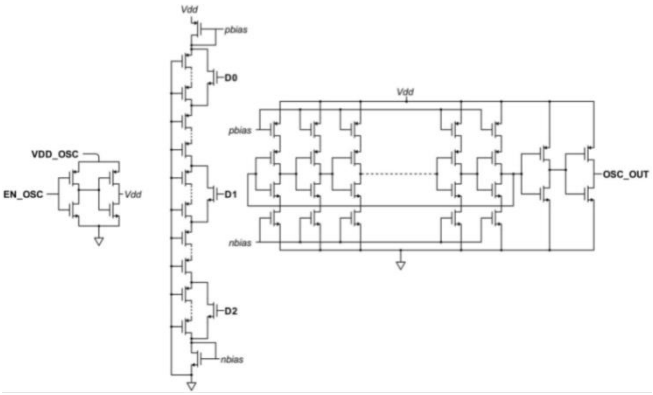

Fig 8. Proposed Schematic of Oscillator

IV. SIMULATION RESULTS

The proposed current staved CMOS inverter based oscillator is simulated using spectre simulator & the output waveforms are as shown in figure 9.

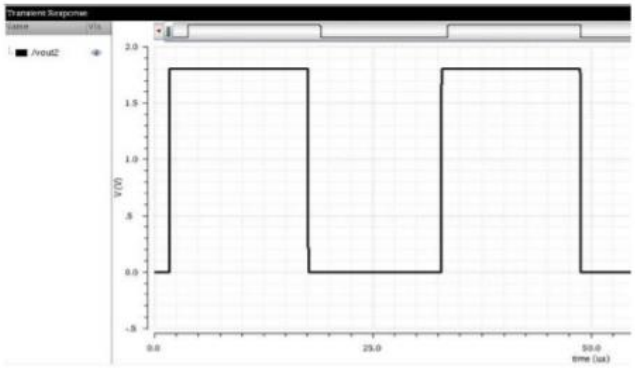

Fig 9. Oscillator Output

The repeat of faltering is resolved at temperatures from 00C to 125oC, after post position parasitic extraction, at 1.8V power supply, at different method corners, without cutting the oscillator i.e., D0 = 0, D1 = 0 , D2 = 0 as showed up in figure 10.

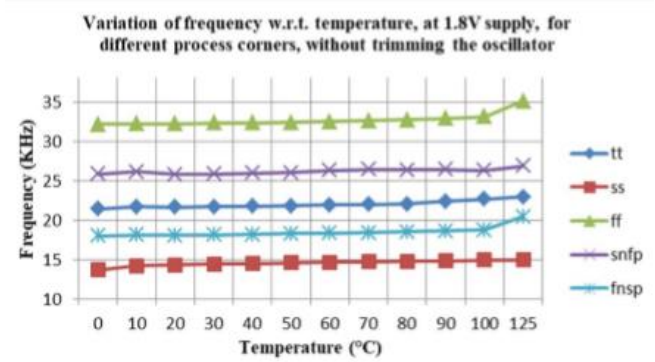

Fig 10. Oscillator frequency before trimming

By then the oscillator is cut by using trim bits(D0, D1, D2) & the biasing current , the repeat of influencing is resolved structure 0oC to 1250C, after post plan parasitic extraction at 1.8V power supply at different strategy corners.

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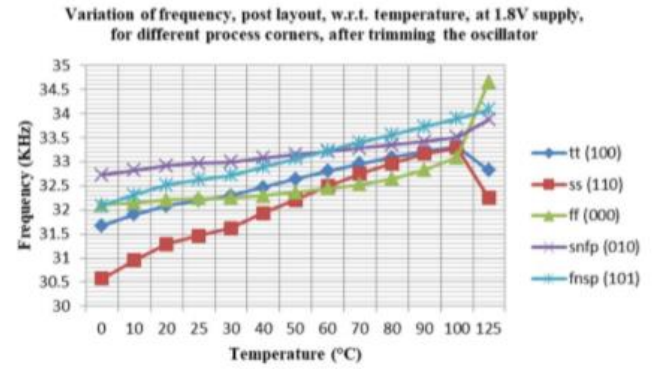

Fig 11. Oscillator frequency after trimming

Table I. VARAIATION IN FREQUENCY ACROSS TEMPERATURES

S.No	Process Corner	Trim bits D[0]D[1]D[2]	Variation of frequency in (%) w.r.t temperature from 0°C to 125°C at 1.8Vsupply w.r.t 32.768kHz
1	tt	100	-3.35% to +1.65%
2	ss	110	-6.71% to +1.59%
3	ff	000	-2.04% to +5.77%
4	snfp	010	-0.12% to +3.39%
5	fnsp	101	-2.07% to +4.00%

The average current consumed form battery supply is plotted in the temperature range from 0°C to 125°C at 1.8V supply. The average current is less than 250nA at different trim bit settings.

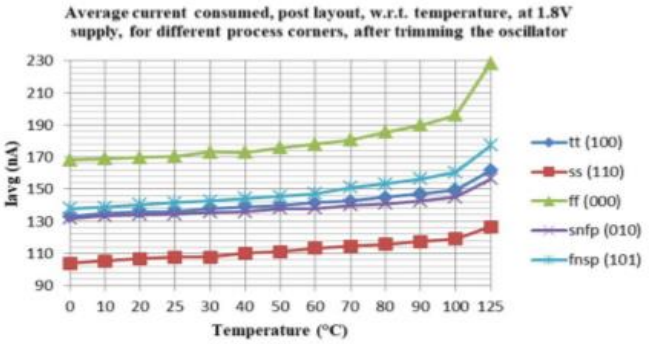

Fig 12. Average Current consumed from battery supply

Fig 13. Layout of proposed Current Starved Oscillator

V. CONCLUSION

A Current starved CMOS inverter based on-chip oscillator which operates on low frequency & low power is implemented in UMC180 CMOS technology. This circuit can be used for elapsed time counter application.

An ultralow power low frequency CMOS oscillator with biasing circuit for temperature compensation has been implemented.

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