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Design of Parity Preserving Reversible DIF-FFT using 90nm Technology

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***Abstract:** Reduction of power consumption is the major goal in modern circuit design. Reversible logic gate do not lose any information & thus have zero power dissipation. In all signal processing applications, the most important computation involved is Fast Fourier Transform (FFT). For the fault tolerance computation parity preserving logic can be used .The authors present an efficient parity preserving reversible DIF-FFT using 90nm technology. The implementation involves the design of DIF-FFT with reversible P2RG along with Fredkin gate over different combinations of adders (Carry look ahead adder (CLA), Carry save adders (CSA), Carry skip adder (CSK) & Ripple carry adder (RCA)) & multipliers (Array Multiplier (AM), Carry Save Multiplier (CM), Parallel Multiplier (PM), Wallace Tree Multiplier (WM)). DIF-FFT Architectures of different combinations were coded using Verilog & the same was simulated by Modelsim 6.3f. Parameters such as Hardware Device utilization & Power analysis were done using Quartus II 9.0 with respect to Stratix II device which works on 90nm technology. It was found that DIF-FFT Architecture designed using CSA & CM uses lesser resource utilization whereas architecture designed using CSA & AM has lesser Power dissipation by 72% & 81% respectively.*

***Keywords:** DIF-FFT, Parity preserving logic, Fredkin gate, P2RG.*

I. INTRODUCTION

Power dispersing is one of the most huge factors in VLSI circuit plan. Irreversible basis entryways scatter tremendous proportion of power paying little notice to the affirmation strategy in view of the loss of information. Reversible methods of reasoning are critical in low-control circuit plan as they spare information by un-handled bits instead of disposing of them [1]. In any sign getting ready application, the pre-treatment of the moving toward sign beginnings at the sign's repeat region which was done with the use of DIF-FFT computation. For saving huge proportion of force, DIF-FFT can be completed using reversible justification entryways. Uniformity ensuring method of reasoning can be used for the adjustment to inner disappointment computation. By differentiating the equity of data sources and yields faults in the circuit can be recognized. It is understood that reversible gateways have a proportionate number of wellsprings of information and yields from the condition 1. Along these lines, for uniformity preservation, this is satisfactory to exhibit that fairness of wellsprings of data and yields should be identical. For example, in balance preservation, 4*4 reversible entryway must satisfy the underneath condition,

$$A \oplus B \oplus C \oplus D = P \oplus Q \oplus R \oplus S \quad ..1$$

In like manner, plan of reversible correspondence ensuring DIF-FFT figuring is realized in this work.

The remainder of the bit of the paper is standardized as seeks after. Territory II talk about the composing audit. Region III courses of action with proposed framework. Territory IV analyze about generation results. Fragment V oversees Conclusion

II. LITERATURE SURVEY

Reversible method of reasoning is basic starting late considering the way that it has ability to lessen the power dispersal which is standard essential in low power plan. Non Reversible basis gateways which are used for the structure of ALU eat up more power. So there is a prerequisite for lesser power use and the reversible justification has been accepting fundamental occupation during progressing a very long time for low power VLSI Design strategies. This system helps in diminishing power usage and power dispersing [2]. An organized mapping exists among sources of info and yields for a reversible method of reasoning entryway. A stand-out yield vector is conveyed by the reversible circuit for every data vector [3]. Prashant. N. G et al., (2013) showed that a reversible snake circuit can be recognized with at any rate two junk yield and one predictable data. For organizing imperfection tolerant snake circuits these necessities are not applicable [1]. Ragani Khandelwal et al., (2015) proposed a 5*5 balance securing reversible entryway, P2RG [4]. Bhagyashree. An et al., (2016) proposed a novel balance Preserving Reversible entryway and arranged Parity Preserving Half-Adder/Subtractor circuit [5]. In perspective on the control signal the unit will carry on as snake/subtractor. Raghava Garipelly et al., (2013) discussed rapidly about the diverse reversible method of reasoning portals and their importance in low power plan [6].Umesh Kumar et al., explained the show evaluation of various justification entryways with respect to control [7].

III. PROPOSED METHODOLOGY

A. Parity Preserving P2RG & Frdekin gate

The parity preserving half adder/sub-tractor is realized using one P2RG gate & one Fredkin gate [4][9]. Here the input of the control signal is varied as either Adder/Subtractor where a single unit can be either used as Adder or Subtractor.

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The parity preserving Half adder/subtractor & Full subtractor is realized using one P2RG gate & one Fredkin gate as shown in Fig 1 & Fig 2.

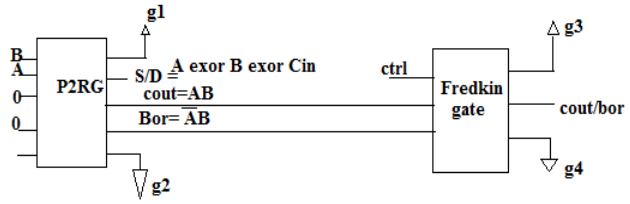

Fig.1. Half adder & half subtractor using P2RG gate & Fredkin gate

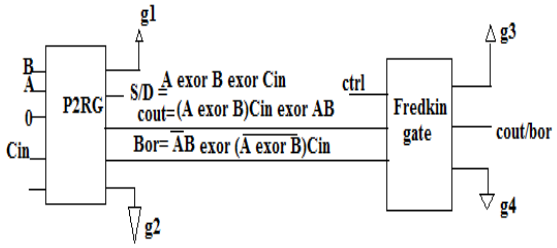

Fig.2. Full adder & Full subtractor using P2RG gate & Fredkin gate

B. 2 Point Reversible DIF FFT

In fast Fourier transform algorithms [10], the results of smaller discrete Fourier transform is combined into a larger discrete Fourier transform or viceversa through the butterfly computation. These smaller DFTs are then combined via size-r butterflies, which themselves are DFTs of size r (performed m times on corresponding outputs of the sub-transforms) pre-multiplied by roots of unity (known as twiddle factors).

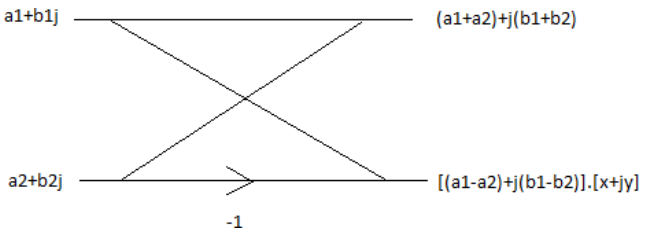

Fig.3. 2-point DIF-FFT Structure

In "decimation in frequency", the butterflies come first & are post-multiplied by twiddle factors.

The figure 3 describes the computation of 2-point DIF-FFT here a1, a2 are taken as real part & b1, & b2 are taken as imaginary part. In the first stage the sum of the real & imaginary is computed which yields in (a1+a2) + j (b1+b2). Similarly in the next stage the twiddle factor (x+jy) is multiplied with the sum of subtracted real (a1-a2) & imaginary (b1-b2) values which yields in [(a1-a2) + j(b1-b2)].[x+jy].

Adders [8] such as RCA, CSK, CLA, & CSA are replaced whenever addition operation comes into picture whereas the same adders are used as 2's complement subtractors in the place of subtraction. Multipliers such as AM, CM, PM & WM are used whenever multipliers come into picture.

C. Reversibe DIF FFT Architecture

Making use of the designed basic architecture of 2-point DIF-FFT the 8-point DIF-FFT is computed for various combinations. The general DIF-FFT architecture is shown in Figure 4.

$$W_N = \text{Phase Rotation Factor} = e^{-j2\pi/N}$$

$$W_8^0 = e^{-j(2\pi/8)0} = e^0 = 1$$

$$W_8^1 = e^{-j(2\pi/8)1} = e^{-j\pi/4} = (1-j)/\sqrt{2}$$

$$W_8^2 = e^{-j(2\pi/8)2} = e^{-j\pi/2} = -j$$

$$W_8^3 = e^{-j(2\pi/8)3} = e^{-j3\pi/4} = -(1+j)/\sqrt{2}$$

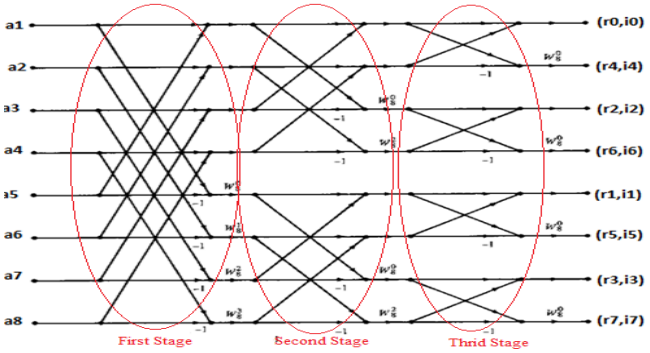

Fig.4. 8-point DIF-FFT Structure

In the Figure 4 of DIF architecture the first stage of the inputs are forced while the computation of the first four butterfly produces the sum of the input while the next four stages get multiplied with the twiddle factors such as W_8^0, W_8^1, W_8^2, W_8^3 .The outputs of the first stage are connected as wire & fetched as a input for the second stage & so on, the outputs of the third stage are the final resultant of DIF architecture in bit reversal order.

IV. SIMULATION RESULTS

The design of parity preserving reversible DIF-FFT architecture is coded using Verilog & simulated using modelsim 6.3f. Parameters such as Hardware Device utilization & Power analysis were done using Quartus II 9.0 with respect to Stratix II device.

A. Simulation output of DIF-FFT Architecture:

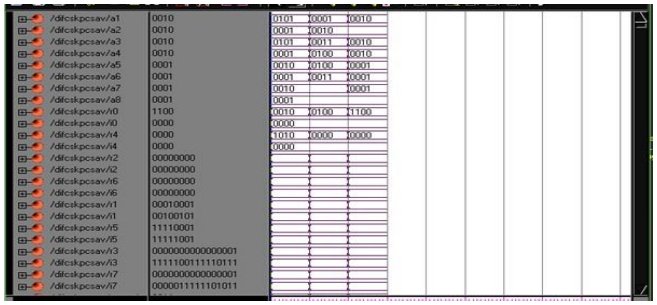

Fig.5.Simulation result of DIF-FFT Architecture.

Figure 5 shows the simulation result of DIF-FFT architecture designed using Carry save adder & Wallace Multiplier.

Input: a_1 = 0010; a_2= 0010; a_3 = 0010; a_4 = 0010; a_5 = 0001; a_6 = 0001; a7 = 0001; a_8 = 0001;

Output:

(r0, i0) = (0010, 0000)

(r4, i4) = (0000, 0000)

(r2, i2) = (00000000, 00000000)

(r6, i6) = (00000000, 00000000)

(r1, i1) = (00010001, 00100101)

(r5, i5) = (11110001, 11111001)

(r3, i3) = (0000000000000001, 1111100111110111)

(r7, i7) = (0000000000000001, 0000011111101011)

B. Hardware utilization Summary

TABLE I. Resource UTILIZATION OF DIF-FFT ARCHITECTURES

Adder	Multiplier	Combinational ALUTS	Dedicated logic registers	Total pins
RCA	AM	424	128	180
	PM	424	128	180
	CSM	380	128	180
	WM	393	128	180
CSA	AM	473	132	180
	PM	441	132	180
	CSM	370	132	180
	WM	398	128	180
CSK	AM	424	128	180
	PM	424	128	180
	CSM	343	128	180
	WM	393	128	180
CLA	AM	449	128	180
	PM	422	128	180
	CSM	361	128	180
	WM	395	128	180

Table I describes the Resource utilization for FFT-DIF architectures designed using different combination of adders & multipliers the area includes the combinational ALU's & Logic Registers.

C. Arithematic LUT comparison

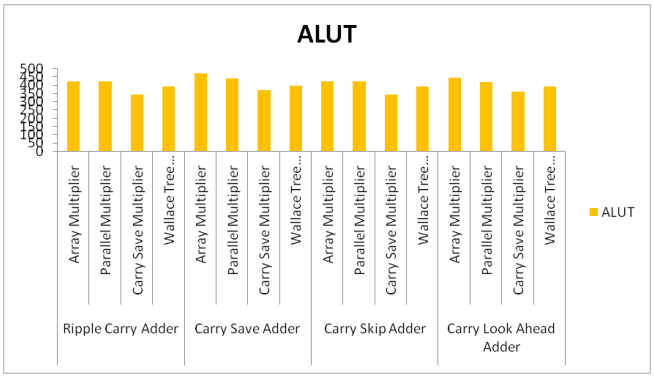

Fig.6. Comparison of Arithmetic LUT

Fig 6 shows the Comparative chart for Arithmetic utilization of DIF-FFT architectures for various combinations. From the graph it is evident that DIF architecture designed using Carry skip adder & Carry save multiplier uses lesser hardware.

D. Power Summary

TABLE II. Power disspations of dif-fft architectures

Adder	Multiplier	Total thermal power (mw)	Core static thermal power (mw)	Core dynamic thermal power (mw)	I/O thermal power (mw)	Total Power (mw)
CSA	AM	347.26	303.21	7.77	36.26	649.5
	PM	346.18	303.20	7.32	35.65	692.3
	CSM	397.71	303.74	38.7	55.19	795.4
	WM	341.97	303.16	5.10	33.72	683.9
RCA	AM	341.33	303.15	8.36	29.82	682.66
	PM	339.53	303.13	7.05	29.34	679.05
	CSM	345.91	303.20	7.18	35.53	691.82
	WM	338.98	303.13	6.16	29.69	674.96
CSK	AM	345.57	302.20	6.42	35.95	691.14
	PM	342.48	303.17	7.32	31.99	684.96
	CSM	342.14	303.16	6.50	32.08	683.88
	WM	341.06	303.15	6.23	31.08	682.12
CLA	AM	347.10	303.21	7.61	36.28	694.6
	PM	347.96	303.22	8.25	36.49	695.92
	CSM	341.12	303.15	7.42	30.54	682.23
	WM	339.50	303.13	8.04	28.33	679

Table II describes the power utilization for DIF-FFT architecture. The power utilization includes parameters such as Static, Dynamic & Thermal power consumption. These three parameters are summed up which results in total power dissipation.

E. Total Power Consumption

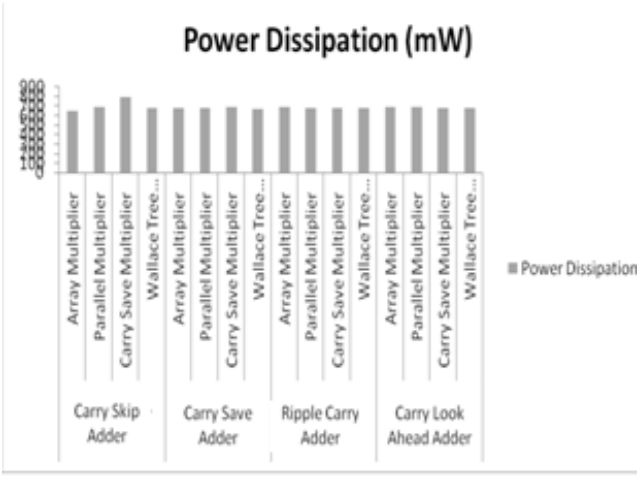

Fig.7. Comparison of Power Dissipation

Fig 7 shows the Power dissipation of different combinations. From the graph it is evident that that DIF architecture designed using Carry skip adder & Array multiplier dissipates lesser power comparing with other combinations.

V. CONCLUSION

Reversible logic will not switch over all input since all reversible gates has one- one mapping. Area & Power is a common bottleneck in many of DSP & SoC applications. Once such application DIF FFT was designed using parity preserving reversible gates namely Fredkin & P2RG gates over different combinations of adders & multipliers. The coding was done using Verilog, simulated with the help of Modelsim 6.3f & power, area & delay was obtained using Quartus II 9.0 Stratix II Device. It was found that DIF FFT Architecture designed using CSA & CM uses lesser hardware by 72% compared to worst case DIF architecture designed using. CSA & AM. Similarly, DIF FFT Architecture designed using Carry Save adder & Array multiplier has lesser Power dissipation by 81% when compared to worst case DIF architecture designed using RCA & CSM.

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