Efficient Hard Decision Fault Diagnosis using Scan Based Testing in Sequential Circuits

S.Vimal Raj, E. Nandha Kumar, V. S. Sanjana Devi, C. Sakthivel, K. Rajangam

Abstract: ***Testing in sequential circuits is extremely difficult because behavior of sequential circuits depends on both the present and past value. Nowadays, in memory applications even single bit changes in digital circuits results in serious error. This paper presents a fault-detection method for difference-set test patterns with efficient hard decision algorithm using majority logic decoder/detector. This algorithm has the ability to correct large number of faults. The proposed checksum method for fault detection and correction significantly reduces testing time. This technique doesn't require appending parity bits, which makes the area overhead minimal and keeps the extra power consumption low.***

Keywords—scan based testing; Majority logic decoder; Hard decision algorithm; parity check bits; error correction codes; memory.

I. INTRODUCTION

VLSI technology has been emerging by integrating many IC's into a chip also by scaling smaller dimensions, and lower operating voltages results in reliability of memories is put into risky and cause more failure rates, not only in extreme radiation environments like spacecraft and avionics electronics, but also at normal terrestrial environments [1], [2]. Especially, SRAM memory failure rates are increasing. In many applications, reliability of memory is not stable.

In sequential fault diagnosis is the process of fault location is carried out step by step, where each step depends on the result of the diagnostic experiment at the previous step. Scan chain is a technique used for this testing. The objective is to make testing easier by providing a simple way to set and observe every flip-flop in an IC. [3]-[5]

The basic structure of scan includes the following set of signals in order to control and observe the scan mechanism

1.Scan in and scan out define the input and output of a scan chain. In a full scan mode usually each input drives only one chain and scan out to observe one as well.

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2.A scan enable pin is a special signal that is added to a design. When this signal is asserted, every flip-flop in the design is connected into a long shift register.

The main advantage of the scan path technique is that a sequential circuit can be transformed into a combinational circuit, thus making test generation for the circuit relatively easy.[6]

This scan testing is used for fault diagnosis methods. Various fault diagnosis methods are

1. Plain Majority logic decoder (MLD)-one dimensional parity method.
2. MLD with syndrome fault detector(SFD)-One dimensional parity method
3. Majority logic decoding detector(MLDD)-Two dimensional parity method.

All this decoder uses hard decision algorithm.

II. LITERATURE SURVEY

Memory soft errors due to noise increases. To prevent these soft faults triple modular redundancy is used [7]. It is the special case of the von Neumann method. Majority voter is used for selecting the correct output from false ones. But complexity overhead is more compare to the design of majority voter which consumes more power consumption. Then comes error correction codes [8]. It eliminates soft error in minimal amount. For complicated applications it is not suitable. Majority logic decoding (MLD) with maximum fault correction using cyclic codes is introduced later [9]-[12]. Then research has been done on Low density parity check codes (LDPCs) belong to majority logic decodable codes [13], [14]. A specific type of LDPC codes is difference set cyclic codes (DSCCs). In this paper we are focusing on DSCC. These DSCCs are widely used in FM multiplex broadcasting station [15-17].

III. EXISTENT MAJORITY LOGIC DECODING SOLUTIONS

a) PLAIN MLD- 1 D PARITY METHOD

ML decoding is very easy to implement, low complexity and very practical. Schematic of memory system is shown in Fig.1. First data bits are coded and stored in memory. At the time of reading, code word is fed to the decoder before sent to the output. Data bits are all corrected from the bit changes during the decoding process.

The main disadvantage of this method is for coded N bits of data require N cycles for completing the diagnosis and decoding procedure. If there is no error no need to check all the coded data bits using N clock cycles. This increases unnecessary power consumption.

While coding the data bits 1-D parity method is used where number of parity bits is equal to number of segmented data bits. Previously simple parity method is used that is [18]

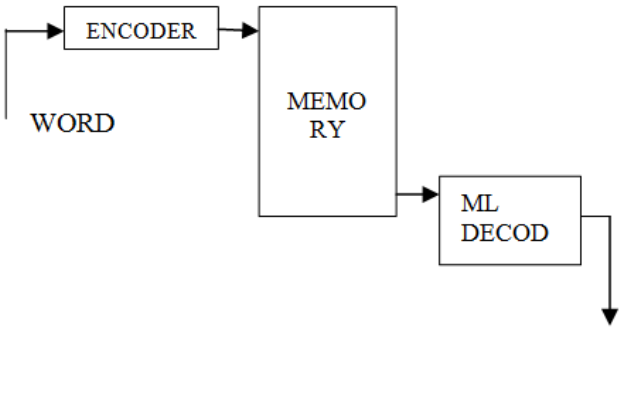
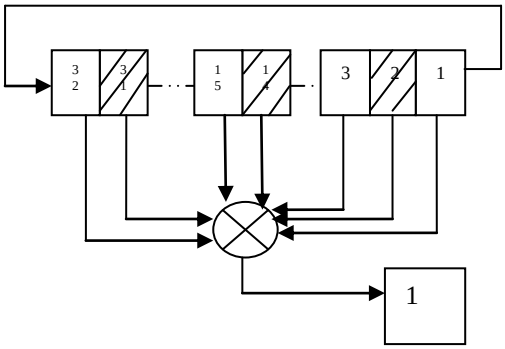


Fig. 1. Schematic of memory system with MLD

adding a single parity bit at the front of data bits by calculating even number of 1's in data bits. This type of encoding fails to detect burst errors. That is it can detect only odd number of faults. Because even number of faults also gives same parity and fault gets hided and fails to detect.

a)



b)

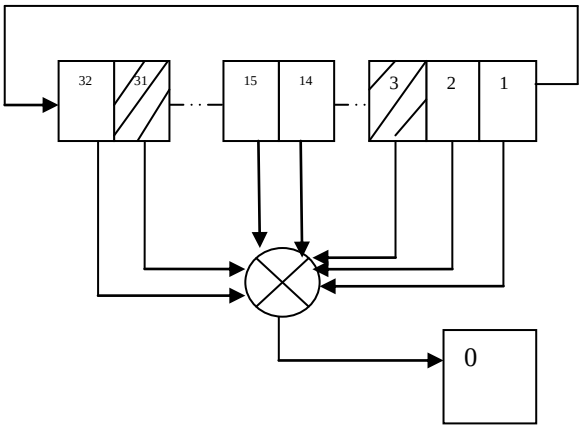


Fig. 2: Simple parity check of N=32 ML decoder. a. Three bit flips, b. Two bit flips.

For example in the above diagram shows coded word of 32 bits. Fig 2.a shows that three bit changes at 2,14,31th position. At encoding before transmitting parity bit is 0. After decoding due to noise there is three bit changes which is odd in number so parity bit is changed to 1 after XORing. Change in parity bit results presence of error. Whereas in Fig.2.b shows that two bit flips at 3 and 31. But parity bit is 0 as like fault free transmitted. Hence fault is undetectable. This indicates use of simple parity check fails to detect the fault. So that decoder part is extended with Hard decision algorithm.

ML decoder using Hard decision algorithm is powerful and ability to correct large number of faults. Schematic of ML decoder shown in Fig.3. It consists of four parts. 1) cyclic shift register, 2) XOR, 3) Decoder, 4)MUX. Input signal is initially stored in shift register and shifted. Shifting has to be done until the last bit is shifted out from the last register. At each step data bits are taken to XOR for producing parity bit. This parity bit is used for comparing with parity bit of original data. This is first level of step in fault diagnosis.

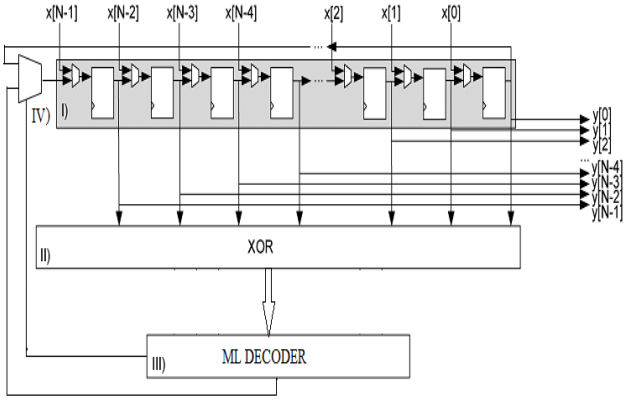


Fig. 3: Schematic of ML decoder

In the next step, hard decision algorithm comes for deep diagnosing. That is it goes for checking each bit of received data to the transmitted data. If there is any bit flip then signal is triggered to invert that bit. MUX has the responsibility of correcting the bit. If there is no fault it simply passes the data bits to the register through h first line of input. Otherwise corrected data bit goes to the second line of input

b) MLD WITH SYNDROME FAULT DETECTOR

In order to improve the performance various designs of decoder may be used. In the previous method the serious disadvantage is unnecessary checking of all the data bits to the transmitted even though those bits are fault free. To overcome going for calculating syndrome, only faulty code words are decoded. Also it reduces time taken for completing the decoding procedure.

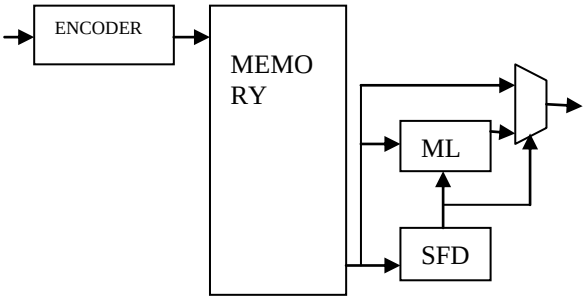


Fig. 4: Schematic of ML decoder with SFD

SFD is XOR matrix that calculates syndrome based on parity check matrix. Syndrome equation is calculated by every parity bit. Complexity gets increases when the size of code increases. If one of the syndrome bits is detected as 1 then indicates faults and decoding starts. Otherwise it directly forwarded to the output to generate the result. Disadvantage of this method is by adding extra module of SFD results in increase in complexity and leads to more power consumption compare to previous one.[19]

.

c) MLDD-TWO DIMENSIONAL PARITY METHOD

Design of ML decoder is improved and modified into MLDD (Majority logic decoder/detector). It uses difference set cyclic codes (DSCCs) that is two dimensional parity method. Two dimensional method has the ability to correct large number of errors. Two dimensional is adding two set of parity bits at encoder part that is by calculating from row wise and column wise. For example,[20]

Original data: 10110011: 10101011: 01011010:

```
10110011  1
10101011  1
01011010  0
11010101  1
----------
10010111  1
```

Data to be sent: 101100111: 101010111: 010110100: 110101011: 100101111

Decoding part is same except that by adding extra module for controlling the process.

Decoding algorithm is still the same but difference is in previous method we have to check all the N bits of data even though there is no fault. But here in first three cycles of decoding process, result of XOR matrix is same as that of transmitted data bit then no need to go for ch ecking all the remaining data bits which saves time. Thus data is forwarded directly to the output.[21] Schematic of MLDD is shown in Fig. 5

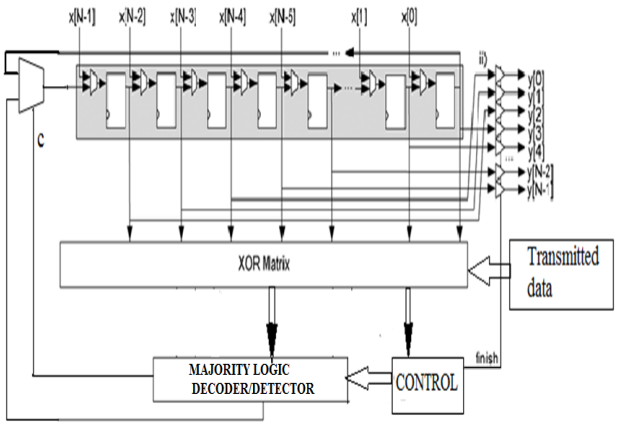


Fig.5: Schematic of Majority logic decoder/detector

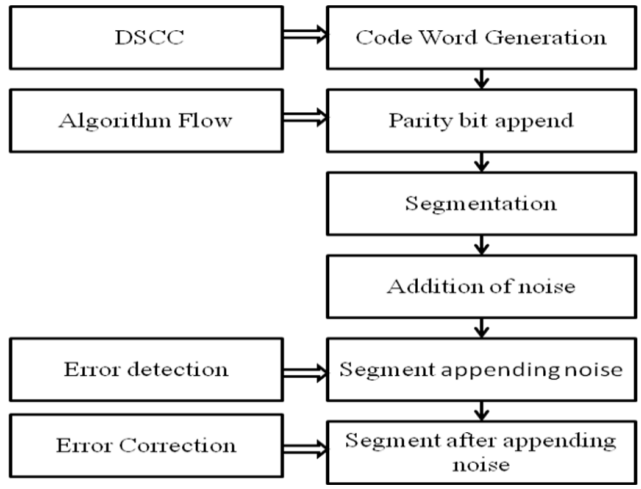


Fig.6: Design flow

Additional Hardware parts to perform error detection is 1.Control unit- It sends signal to stop the process when no fault is detected until 3 steps of shifting.

B0B1….Bj

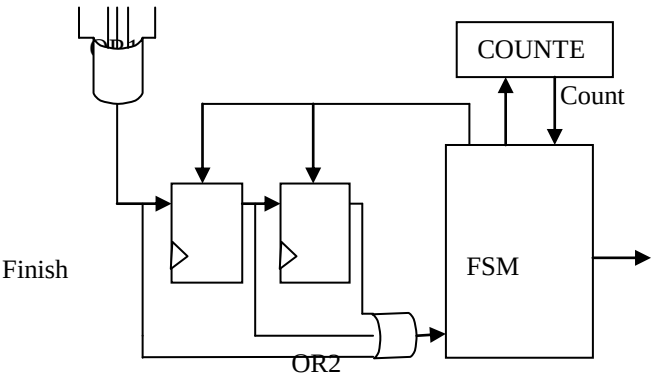


Fig.7: Control unit schematic

2. Output tristate buffers- These buffers are always in high impedance state unless control unit triggers and send the finish signal. It helps in forwarding the current values of shift register to the output y.

Control unit manages the process of detecting errors. Counter is used here to count up to three cycles. In the first three iterations, control unit evaluates the result of parity checksum from XOR matrix and the output of XOR matrix is combined with OR1 gate. [22]This output is given to three stage shift register. It holds the values of last three clock cycles. In the last cycle that is at third cycle OR2 evaluates the content of register. If content of register is 0, the FSM sends out the finish signal indicating that current processing word is fault free and output is generated through tristate buffers. Otherwise if it is 1, then decoding process continues until it reaches all the N cycles. This clearly indicates performance is improved since most of the coded data bits are no need in shifting to all N cycles. Only those with errors need to undergo full decoding process. Memory system schematic of MLDD is same as that of MLD which is shown in Fig.8.

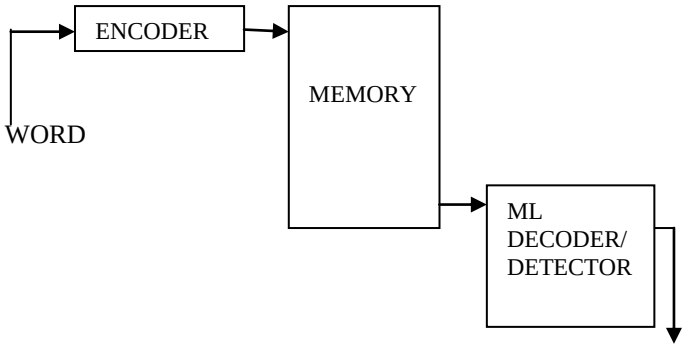


Fig.8: Schematic of memory system with MLDD

IV. PROPOSED CHECKSUM BASED DECODING SOLUTION

At encoder, data is divided into k segments each of equal number of bits. These segments are added using ones complement arithmetic to get the sum. The sum is complemented to get the checksum. Checksum segment is sent along with the data segments.

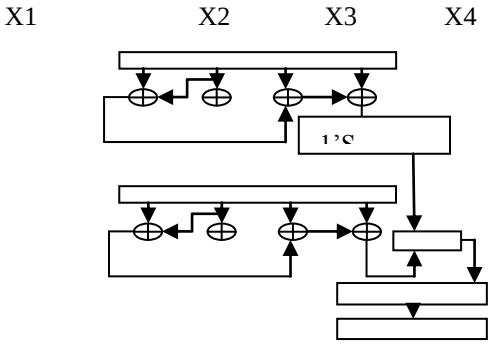


Fig.9: Checksum operation

At the decoder, all the received segments are added using 1's complement arithmetic to get the sum. [23]The sum is complemented. If the result shows all Bits as zeros then received pattern is fault free and it is accepted otherwise it indicates received pattern has error and position where the bit is received is 1 show that corresponding position of the bit in received pattern should be corrected. Remaining procedure will be done by the same Hard decision algorithm.[24] The main advantage of this checksum method is not going for adding parity bits at encoder results time taken in diagnosing fault at the decoder part is reduced. Thus it reduces power consumption. Example of checksum operation is shown below and design flow of checksum method is shown in fig 10.

EXAMPLE:

SENDER'S END:	RECEIVER'S END:
10110011	10110011
10101011	10101011
01011110	01011110
1	1
01011111	01011111
01011010	01011010
10111001	10111001
11010101	11010101
10001110	10001110
1	1
SUM: 10001111	10001111
	01110000
CHECKSUM: 01110000	SUM: 11111111
	COMPLEMENT: 00000000

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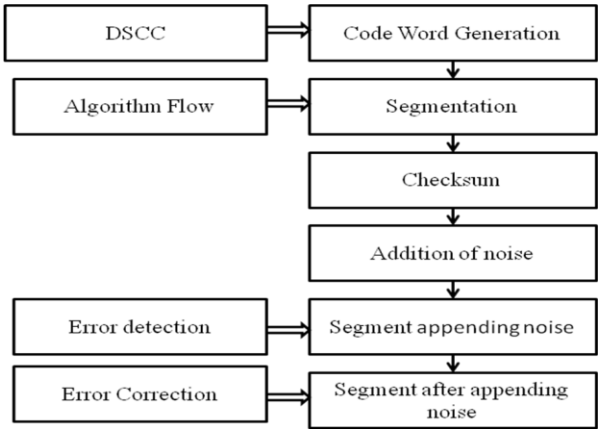
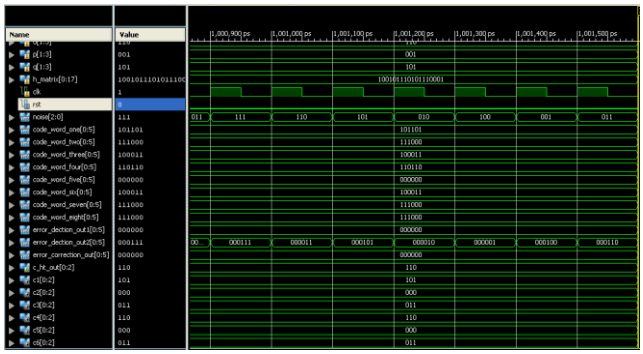


Fif.10: Design flow of checksum Method.

V. RESULTS



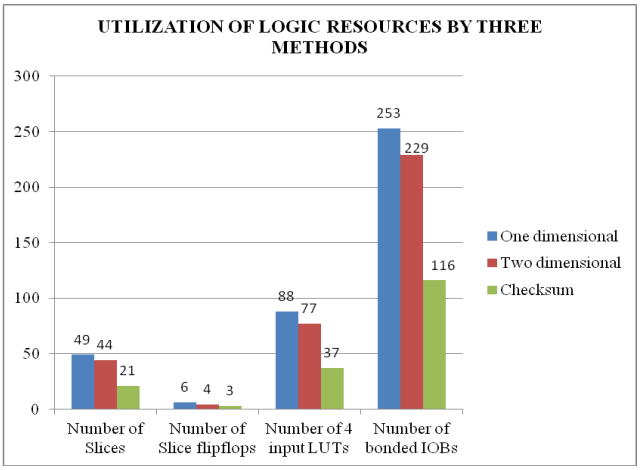


TABLE 1: TIME ANALYSIS

FAULT DIAGNOSING METHODS	TIME TAKEN
One dimensional	9.81 secs
Two dimensional	8.34 secs
Checksum	7.33 secs

Result shows that compare to three methods using checksum operation at encoder reduces time taken of CPU for diagnosing fault with equal number of input patterns. Utilization of various logic resources also reduced.[25]-[26]

VI. CONCLUSION

In this paper, a fault-detection mechanism, Checksum based Hard decision algorithm based on ML decoding using the DSCCs performance is improved compare to previous methods. Power consumption is an important issue in today's technology. In VLSI technology minimization of power is the major concern. Using checksum method we can achieve the target of reducing power consumption. Exhaustive simulation results show that that the proposed technique is able to detect any pattern up to five bit-flips in the first three cycles of the decoding process. This improves the performance the design with respect to traditional MLDD approach.

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