

Different Types of Ultra-low Power Energy-Harvesting Design Techniques for IoT Applications

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Abstract- In this paper, different type of level shifter circuits, that can able to convert the sub-threshold level to super-threshold level signals are discussed. To develop the ultra-low static power consumption circuit designs such a way to switch on the transistor for a low voltage levels. To enhance the switching speed and minimize the dynamic power consumption, by incorporating the CMOS –inverter buffer circuit at the output side to improve the energy efficiently. These energy harvesting design techniques provides endless energy supply to electronic systems that are remotely located areas. More number of devices are controlled by IoT (Internet of Things) to perform the operation by remote sensing.

Index Term: Ultra low power, IoT, energy harvesting, Power consumption

I. INTRODUCTION

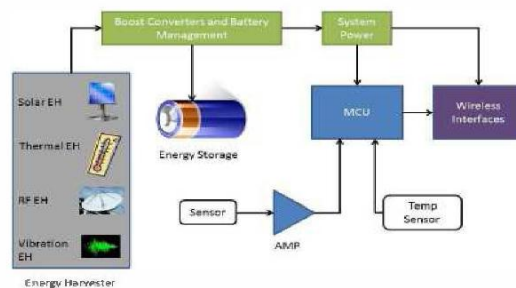
Internet of Things (IoT) is a universal term, which connect with external world by the remote[1]. The broad definition of IoT is includes “sensing and extract usable information and communicating that information through remotely located user”[1]. The concept IoT is a tremendous growth in last 10 years [1,2]. In that context, ultra-low power consumption techniques helps to increase the lifetime of battery [1][2]. The bunch of IoT devices are run by today either by battery source or source from the wall [2]. However, as the number of connected devices increases exponentially, providing the supply voltage to operate those may devices is a difficult task[1,2]. If thousands of devices are connected to internet and performing operations, we require approximately 274M batteries would be needed. Energy harvesting techniques can helps to operate IoT devices by self-sustainable and eliminate the need for battery replacement. Moreover, to increase the lifetime of the system.

A battery-less IoT device requires energy harvesting techniques to develop the energy from ambient sources [1]. However, the energy generated from the ambient sources such as solar, Thermal, RF, vibration energies are typically very low voltage levels[1,2]. Those voltage levels are not sufficient to operate the device to its rated speed and the long time. So, we a have to increase the voltage levels by adopting various energy harvesting techniques. Power consumption is the major issue in VLSI domain. To overcome these challenges and increase the life time of battery preferred Ultra- low power design techniques instead of low power designs.

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Energy harvesting systems diagram

Fig-1: Pictorial Representation of Energy Harvesting Design.

As, we know that, the renewable energy in the nature is abundant. The renewable energy which is available in the nature is in low voltage. So, we have to convert that ambient source of energy (Solar, RF, Temperature and Piezo-electric) in the form of Electrical Energy by suitable designs and techniques. IoT is a umbrella term, which is link up with billions of components, those all components are run by the battery supply voltage. Therefore, almost all the time battery should be in active mode. The power management block distributes the power to all the peripheral devices, which are connected at the output node.

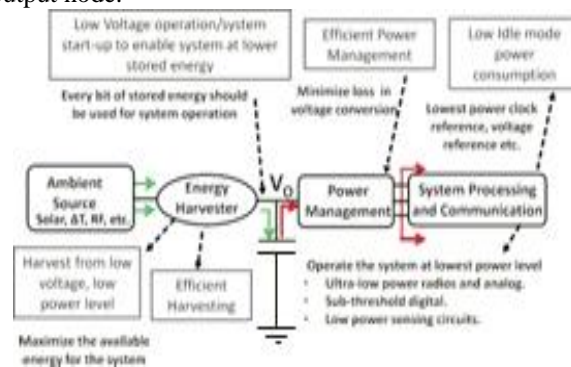


Fig-2-Block Diagram Representation of Harvesting Process

II. SOLAR ENERGY

Solar is an Ambient energy, when sunlight falls on the solar panels, those panels absorb the heat energy, thereby, potential difference exists inside the panel due to incorporating the various types of light detecting diodes. Transducers are used to convert energy from one form to another. The battery can store the energy in the form of electrical energy. The energy, which we developed from solar cells is in the form of low voltage. For that, we are using various types of level converters to boost up the energy levels. Those are used to run the system more effectively.



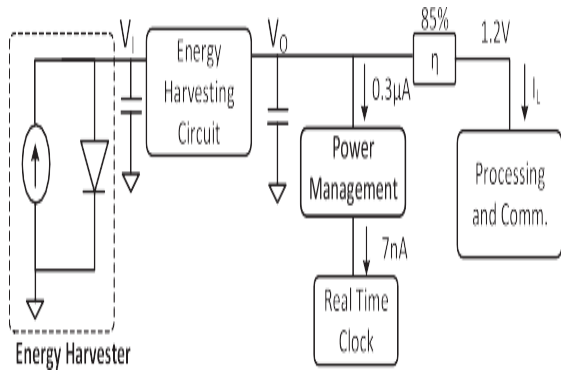


Fig-3. Functional Procedure of Energy Harvesting Design

III. LEVEL CONVERTERS

: Level converters play an important role in electronics domain, why because the voltage levels which are developed by ambient sources are not able to run the system. There by, we have to boost up the voltage levels by using different level shifter design, as shown in below fig.4 is a level converter, which converts the voltages from logic-0 to logic-1 and logic-1 to logic-0 based on the requirement of the out stage. The internal mechanism of level converter looks as a potential divider, which enables us to boost up the voltage levels

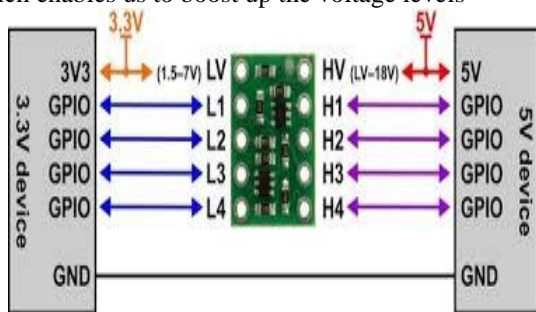


Fig-4- level converter board form 3.3v to 5v

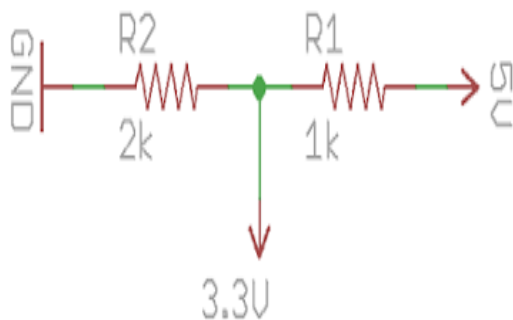


Fig-5 Internal Design as Potential Divider

We can improve the life time of the battery by applying the ultra low power designs because the devices which are connected to IoT has to stay long time in idle mode. There by energy is consumed.

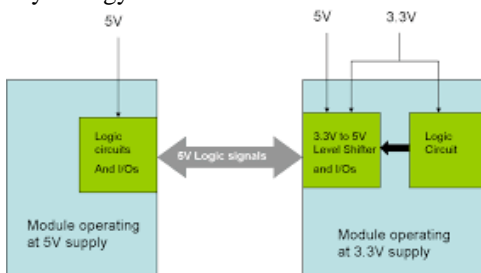


Fig-6- Conversion of Voltage levels from Low to High

1. Conventional Level Shifter Design of Cross Coupled Type: Level converter/shifter design is the basic building for changing input voltage levels to up-voltage converter and down voltage converter according to the input nominal voltage (V_{in}) as shown in the fig-9. The conventional level shifter design consists of two PMOS Transistors (M_2, M_3) connected in the form of Cross coupled. And two NMOS transistors (M_1, M_4) are connected in a parallel manner as shown below. Input signal (V_{in}) directly given to Transistor M_1 , and Inverted input Signal (V_{in-b}) given to Transistor M_4 by simultaneously. Output Signal will be observed at A, B nodes with a naming of V_{out_b} and V_{out} successively.

Working Principle: If input Signal at Logic -1, Transistor (M_1) is ON and Transistor (M_4) is OFF Mode, Due to inverted input signal. The output voltage at node A will become ground (0) due to Transistor (M_1) is ON. As we seen that, two PMOS transistors (M_2, M_3) are connected by cross coupled. If Transistor (M_2) is ON, due the voltage at node A, in contrast, Transistor (M_3) will become OFF. Finally, the voltage levels at node A, B are opposite to each other.

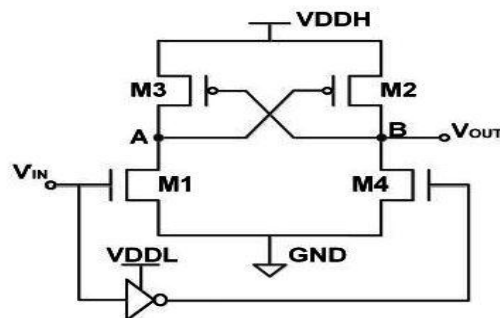


Fig-9: Conventional Level Shifter Design with Cross-Couple.

The major drawback in conventional cross couple level shifter is PUP and PDN network at 'vcc' and 'vss' terminals respectively. Which causes functional failure from low to high voltages. However, these results creates large delay and area penalty.

2. Conventional Level Shifter Design Current Mirror

Type: If V_{in} is high and V_{in-b} become low, Transistor M_1 is ON and transistor M_4 become OFF due to inverted supply Voltage. The voltage at V_{out_b} is low. There by, transistor M_2 will become on. So, that the Voltage at V_{out} is High. There is a drawback that high static current flows and output voltage drastically getting reduced.

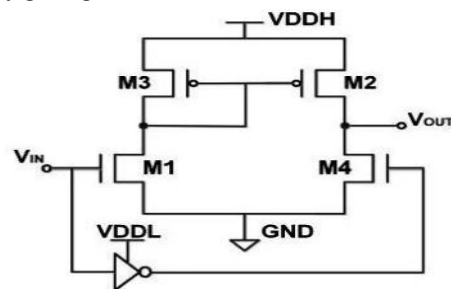


Fig-10: Conventional level shifter design with current mirror type

3. Conventional Level Shifter Design current Mirror with feedback transistor: By using the feedback transistor M2 between two transistors M1, M3, to prevent the static current. Which increases the power consumption and reduces voltage swing? In addition, moreover, the switching speed of transition fall down due to input inverter [1]. During high voltage at output stage, Wilson current mirror generates large amount of leakage current through the transistors (M3, M1). Whereas, result at output side produces the less voltage swing, and causing a high static current.

The major drawback in this design was reducing the voltage swing, by the reason of feedback transistor (M2) and high static current (I2) is developed.

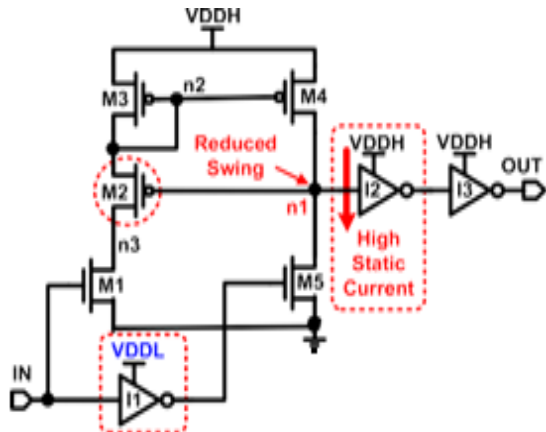


Fig-11: Current mirror type Level converter with Feedback transistor-M2

4. Level Converter Technique with Pass Transistor: In this design an input-controlled diode chain process is used in Wilson current mirror design to enhance the voltage swing levels and reduce the static current.

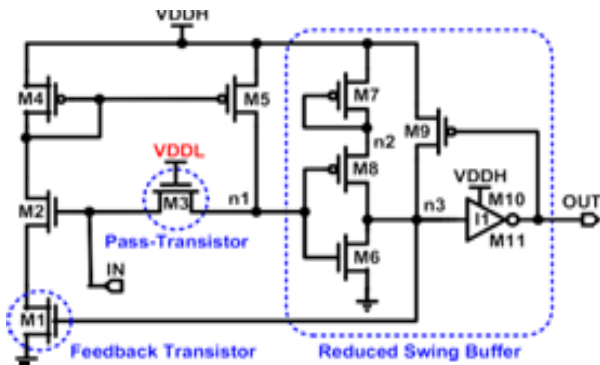


Fig-12: Current mirror type Level converter with pass transistor-M3

Where as, this design generates large delay and high power consumption. Transistor M3 enhances the speed of the fall transition and delay can be significantly improved.

Input Signals at Logic Low to High: This design depicts the operation of Level converter for Low to High transition. When the input voltage goes high, transistor (M2) is turned ON and induces the mirror current through transistor (M5). This mirror current charges at node n1, and discharge at node (n3) by transistor (M6), thereby output goes to high. We can eliminate the static current through M2 and M4; which leads voltage swing reduction at node n1.

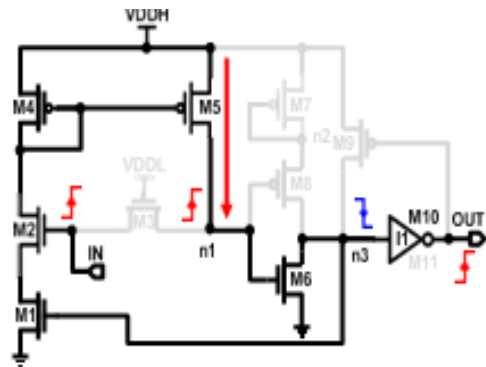


Fig-13: Current Mirror type Level Converter when input is LOW.

Input signals at Logic: High to Low: This design technique shows the operation of Level shifter from High to Low transition. When Transistor (M2) is switched off that disable the mirror current and the pass transistor M3 is turned on for quickly discharging n1. Then, node (n3) is completely charged to VDD_H with the aid of transistor (M9) and the output goes low. Based on the above mentioned principle, significantly, we can improve the delay.

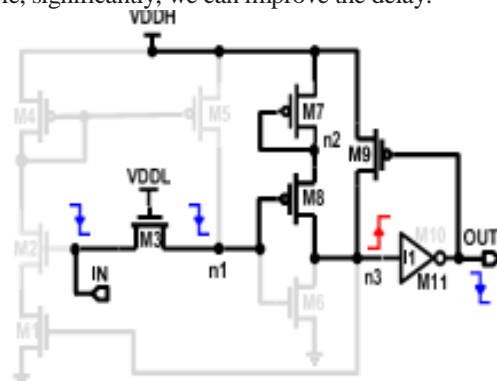


Fig-14: Current mirror type Level converter with when input is HIGH

6. Single supply level shifter

This technique consists of single Power supply to perform the operation, which converts low voltage signal to the higher voltages. The threshold drop across the NMOS transistor (M1) provides a virtual VDD_L due to ground terminal (GND), it means transistor (M2) is switched ON and output is PUP towards HIGH voltage. Therefore, when input is VDDL then output will become VDDH. This energy harvesting technique helps for better communication between once block to another block without adding any extra supply pin. There by, we can reduce the congestion in routing and minimize the overall cost of the system.

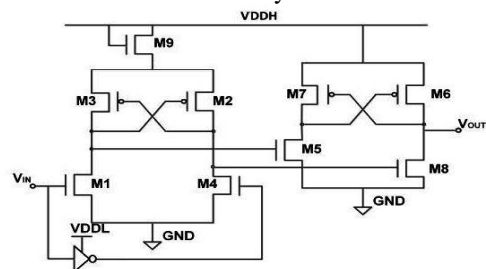


Fig-15: Multiple current mirror type- Single supply voltage

IV. RESULT DESCRIPTION

Power Distribution to peripheral devices: This block diagram

Fig no:7 depicts the power distribution from ambient source to battery. The harvested energy is stored in the battery in the form of electrical energy. The battery charge and discharge cycle depends on the amount of Power received from input. The amount of power consumption has to reduce, when systems is in idle mode. The below fig .-7,8 depicts the pictorial representation of power consumption vs devices which are connected to Internet of Things(IoT) Life time. The life time of any device depends majorly on amount of power consumed and the power radiated from the design.

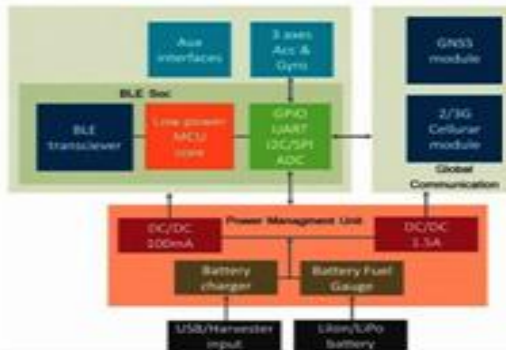


Fig no:7: Power Distribution towards Peripheral Devices

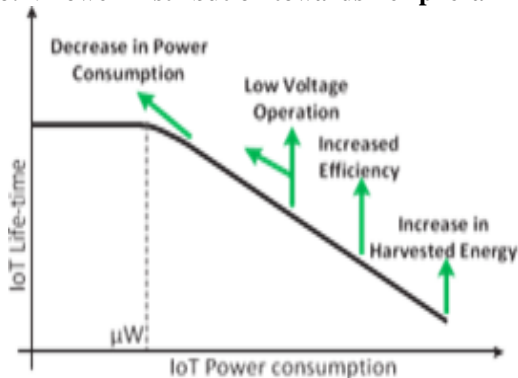


Fig-8: Graph represent the power consumption vs lifetime

V. CONCLUSION

Various types of circuit design techniques, are discussed ,which help to enhance the amount of voltages to run the device. Because, the ambient energy, which is available in nature is not sufficient to operate any electronic potable device. For that, we are using various energy harvesting designs to enhance voltages from low voltage level to high voltage levels. In contrast, power dissipation is the major concern. Thereby, we are using sub threshold and super threshold techniques to operate the design from low voltage level to ultra low levels, because, millions of devices are connected to IoT to perform the task by remotely located area. There by, we can improve the life time of the battery operated devices and reliability of the circuit.

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