Leakage Current Alleviation Techniques for SRAM Cell

Muralidharan Jayabalan, Aswini Valluri

Abstract— Due to the tremendous increase in the call of handheld devices like mobile, iPods and tablets; certain applications like space and biomedical, it is necessary to have low power consuming digital systems. As a crucial part in digital systems,Static Random Access Memory(SRAM) should consume low power since it occupies about 70% of the total chip area. As the technology is shrinking, SRAM's leakage power in standby condition is becoming a most critical concern for the low power applications. This paper gives a study of different leakage components present in SRAM and discusses about various current reduction techniques which include Gated V_{DD}, MTCMOS, Dual threshold and Transistor Stacking.

Keywords— SRAM, Leakage power, Gated V_{DD}, MTCMOS, Dual threshold, Transistor stacking

I. Introduction

In the current Electronics Industry, low power design has appeared to be a key parameter. As a single chip contains millions of transistors fabricated on it , the rate of failure also increases and thus the performance degradation takes place. The usage of portable electronic devices based on battery is increasing rapidly because of the demand of them in our daily life. Such portable devices require memory to reserve the data in the form of Static Random Access Memory (SRAM) as these are faster and also that they need not be refreshed as in the Dynamic Random Access Memory (DRAM). As the technology is growing fastly, it is needed to design a Low power, high performance as well as high speed SRAM's. Due to the expanded integration as well as the operating speeds, Power Dissipation has been a major thought especially for the battery operated devices, where the technology is scaling down. Technology scaling gives better results in providing higher density components but with an impact of increased Leakage Current[1].

Recently, power dissipation in SRAMs have grown as a key design thought as the SRAM's occupy almost of 70% of the chip area. So, while designing any memory circuit, the major issue is regarding the power dissipation. Reduction in power dissipation is a great challenge as it in turn optimizes the design to a great extent. The most important parameter of power dissipation in SRAM's is its leakage current in the stand by condition. The Paper reflects an overview of several leakage current reduction techniques. The residual part of the content in this paper is explained as mentioned: Section-II provides a basic description of conventional 6T SRAM, Section-III explains about the different leakage current components, Section-IV presents the leakage reduction techniques and Section-V ends with a conclusion.

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II. Conventional SRAM

A Conventional SRAM consists of about six transistors among which 4 of them form two inverters as shown in Fig.1. The 2 inverters are connected back to each other in a cross coupled way and the remaining 2 transistors act as access transistors. Two bitlines BL and BLbar and a Word Line (WL) are utilizes to carry on the write as well as read operations. The data is stored in the storage nodes Q and Qbar[2]. SRAM operates in three modes: Write, Read and Standby.

Write: Throughout the write operation, Word Line is being enabled to provide connection between bitlines and the cell. The data which has to be stored in the cell is applied to the two bitlines. The data thus applied is reserved in the two available Storage nodes (Q and Qbar).

Read: Throughout the Read operation, Word line is enabled. Firstly, the two bitlines should be precharged to V_{DD}. Now confiding on the stored data of the storage nodes, one bitline will be discharged and the other one will remain at V_{DD}. The voltage difference thus obtained between the bitlines is given to the sense amplifier which reflects the value that is reserved in the cell.

Standby: At the standby condition, the Word Line will be disabled, disconnecting the cell from the outside world. In such a state the two cross coupled inverters reinforces the data that is present in the two storage nodes.

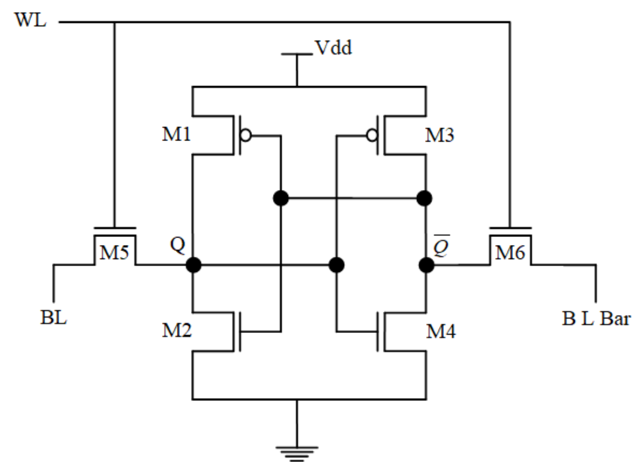

Fig 1: Conventional SRAM Cell (6T)

III. Leakage Current Components

In the SRAM's, two components are main which include Dynamic and the Static Power Dissipation.

The first one occurs by the charging and the discharging of load capacitance. Leakage current chiefly comprises of the following components[3] as shown in Fig.2.

Gate Tunneling Leakage:

The Current that flows by gate terminal of transistor is known as Tunneling. This occurs as the electrons as well as holes passes from the silicon's bulk into gate of an PMOS and NMOS respectively. It has some main components which include:

- Gate-Source & Gate- Drain overlying Current.
- Gate – Channel flowing Current.
- Gate – Substrate flowing Current.

Subthreshold Leakage:

It takes place when transistor works in the weak inverted area. This is the transistor's drain-source flowing current as the gate – the source voltage [Vgs] will be smaller than that of threshold voltage of transistor. This Subthreshold current depends on the threshold voltage, that further gives rise to large amount of Subthreshold current specifically in the devices of short channel.

Junction Tunneling Leakage:

This is due to the reverse bias condition of a PN-Junction and comprises of two chief elements which include

- The carrier diffusion of the minority charge carriers at the end of depletion zone.
- The creation of an electron - hole pair at the depletion zone of a reverse biased PN-Junction. The current of junction tunnelling is a function of doping as well as the reverse bias voltage at the junction. Such a component will be a minute one to the overall of the leakage Current.

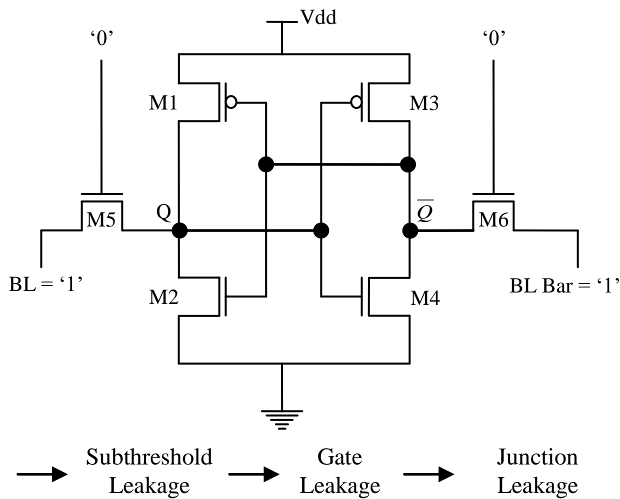

Fig 2: Leakage components in a SRAM cell

IV. EXPERIMENTS AND RESULTS DESCRIPTION

A. Gated V_{DD}

The Gated V_{DD} approach enhances a controlled method that disables the main supply voltage(V_{DD}) whenever the cell is not used and thus eliminates the leakage current[4]. Such type of mechanism minimizes the leakage power dissipation to most extent as shown in Fig.3. In order to gain this method of controlling, high threshold voltage transistor [HighVt] is used at the path of supply [V_{DD}] or in the ground way of a cell by maintaining the further transistors to the low threshold voltage [LowVt]. This control signal gated V_{DD} is utilised to switch ON or OFF the cell. Therefore, the word "Gated" is introduced to explain this approach. The transistor of Gated V_{DD} switches ON at the time of SRAM cell being in active condition whereas, it switches OFF whenever the SRAM cell is set to be in the stand by condition.

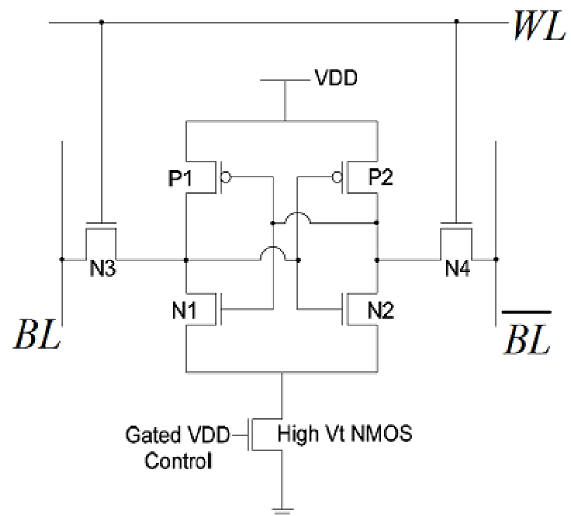

Fig.3: SRAM cell using Gated Vdd Method

B. Multi Threshold Complementary Metal Oxide Semiconductor(MTCMOS)

The approach makes use of multi threshold voltage transistors to optimize the parameters of delay and power[5]. In this approach, a High Vt pmos is attached in between V_{DD} and the memory while a High Vt nmos is placed between cell and ground path and the transistors of the cell are designed with Low Vt. Low threshold transistors(Low Vt) switches faster but tend to high static power leakage. Whereas, high threshold transistors(High Vt) reduces the static power leakage, but switches slowly. Multi Threshold Complementary Metal Oxide Semiconductor(MTCMOS) design methods make use of the circuits designed carefully in order to maintain the delay and power parameters without any penalties. The basic structure of MTCMOS, for minimizing the leakage power makes use of the Sleep Transistors. By these type of transistors, the virtual power rails have been generated that supplies logic. Such High Vt (sleep transistors) links the physical and virtual power rails as given in the Fig.4. Such transistors in the active mode are turned OFF and turned ON in sleep mode with the help of a clock. The sleep transistors reduces the Static leakage current to most extent when the SRAM cell is not used.

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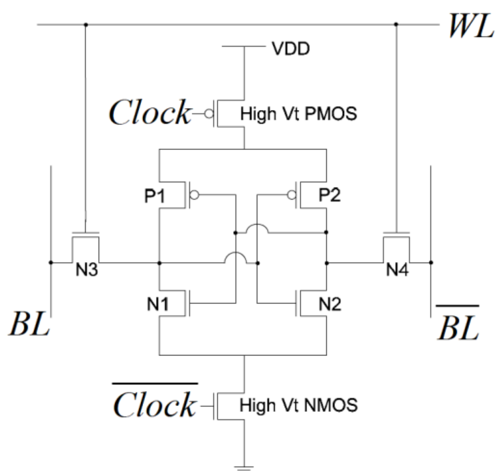

Fig.4: SRAM cell using MTCMOS Method

C. Dual Threshold Technique:

In the Dual threshold approach, few of the transistors in the circuit are of high threshold voltage whereas the remaining transistors are of a low threshold voltage. As given in Fig. 5, transistors N3 , N4 are the driving ones and thus a low threshold could be applicable. These thin channel devices, reduces the switching time that in turn gives fast access to the cell. The remaining N1, N2, P1 and P2 transistors use high threshold voltage, denoted by the thick channel, such that they can prevent the leakage Current of low subthreshold. Therefore reduction of leakage current makes the operation of low power possible in SRAMs.

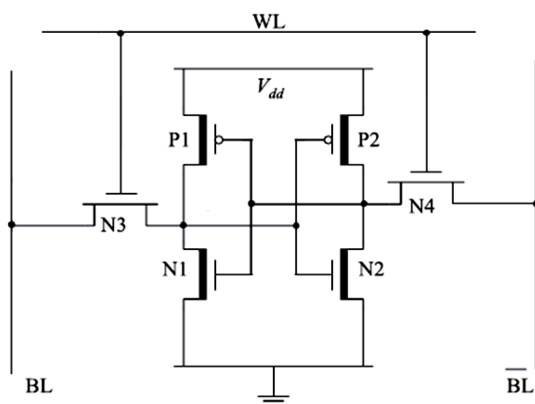

Fig.5: SRAM cell using Dual Threshold Method

D. Transistor stack technique:

This technique resembles the conventional 6T SRAM, except that it has some added stack of transistors introduced down to the nmos transistors as given in Fig.6. The added stacking of nmos transistors increases the threshold voltage (Vt) so as to reduce the subthreshold current such that leakage current can be minimized[7]. The current flowing through more than one OFF transistors reduces the Leaked current than the current which is flowing through the single OFF condition transistor[8].

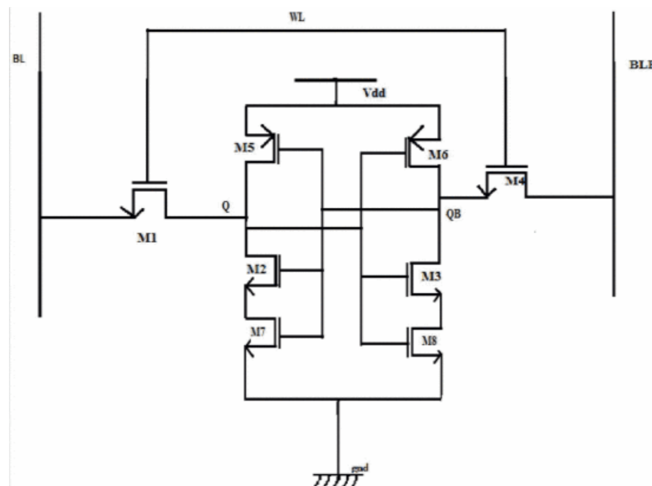

Fig.6: SRAM cell using Transistor stack Method

V. CONCLUSION

Static random access memory's standby leakage current is been a major issue in the modern Low power System on Chip(SoC) devices with the scaling of technology. This paper gives a brief review on various leakage components present along with different leakage current reduction techniques. These techniques achieve the common aim of reducing leakage current in memory. However, these techniques are well preferred in minimizing the leakage currents of the SRAM cells.

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