

Low Cost Automated Washing Machine



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Abstract: Before purchasing any equipment, everybody will ask two things about the products. i. The cost of the equipment's. ii. Efficiency of the products, both never go together. But in our proposed system we present such a system which fulfill both the conditions (low cost and efficient). Presently all hostess (House Wife) is using a smart phone. By making use of these smart phones we are controlling low cost non-automated washing machine and we use it like smart washing machine. The designed circuit used in the washing machine is simple and it consumes less power which in turn dissipate less heat and consumes less space.

Keywords : Smart Phone, Washing Machine.

I. INTRODUCTION

In the existing system washing machine are controlled by the smart mobile phone. But both devices (smart phone and automated washing machine) are smart. They uses separate processors, separate memory and separate display, due to this cost involved is more, they consume more energy and they dissipate more heat. More heat dissipation makes equipment's non-environmentally friendly.

To overcome these problems, we are proposing the system called "Low cost automated washing machine". In proposed system we are making use of the mobile processor to control all the operations which are controlled by the micro-controller. We are bringing all the control system and display of washing machine to existing smart mobile to cut down the cost of washing machine.

Processor and CPU Cores:

The ARM Company produces and licenses design for ARM processors and closely associated components such as caches and memory management units. Companies that procedure embedded systems and other application-specific computer products acquire those designs for incorporation into their products. In most cases, the ARM designs are integrated with application-specific hardware on the same chip. To capture this intended usage, the ARM designs are called cores. Designs are provided by ARM in two different forms: hard

macrocell or synthesizable. The hard macrocell version is a detailed physical layout, targeted to a particular chip fabrication process. The synthesizable form is a high-level language software module that can be synthesized using a suitable cell library in the required target technology. This form allows a number of options on processor functionality to be easily included or omitted. The ARM7TDMI processor is a hard macrocell core, and ARM7TDMI-S is its synthesizable version.

ARM designs are classified as either processor cores or CPU cores. A processor Core contains only a processor and associated address and data bus connections. A processor core contains only a processor and associated address and data bus connections. A CPU core contains cache and memory management components in addition to a processor. The name CPU is somewhat misleading, because traditionally it has meant Central Processing Unit, but we use the name here because it is an identifiable ARM term. We now give brief description of some representative processor and CPU cores.

ARM7TDMI Processor Core:

This core is commonly used for low-cost low-power application. The processor has a simple 3-stage pipeline consisting of fetch, decode, and execute stages. It realizes version v4T of the architecture, supporting both the Thumb and standard instruction sets. Typical operational parameters are 3.3 v power supply and a 66 MHz clock rate. But this core design can be synthesized for 0.9 v operation for low-power battery supply applications or for over 100-MHz clock rates to achieve higher performance.

ARM9TDMI and ARM10TDMI Processor Cores:

These two processor cores are based on 5-stage and 6-stage pipelines, respectively. They have separate instruction and data ports to provide much higher performance levels than the ARM7TDMI can provide. AT clock rates of 200MHz and 300MHz for these processors, Performance levels of the 7,9, and 10 versions of this processor core are in the ratios 1:2:4. The ARM10TDMI has a wider 64-bit path to each memory port, as compared to 32-bit paths for the other two processors. The ARM9TDMI and ARM10TDMI implement versions v4T and v5TE of ISA, respectively. Both of them decode Thumb instruction directly for execution. Cache memories must be used with both of these cores to achieve the higher performance levels.

ARM720T CPU Core:

This core consists of the ARM7TDMI processor core combined with an 8k-byte unified instruction and data cache, and virtual memory management hardware. The cache structure has 16-byte blocks and 4-way set associative. The memory management unit uses a 64-entry associative translation lookaside buffer for holding recent translation. The clock rate for this integrated unit can be up to 60 MHz.

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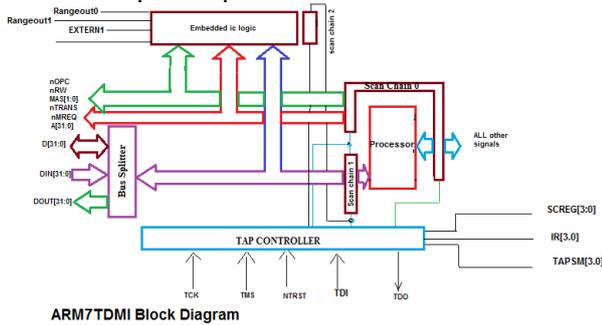
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The added cache and MMU circuitry increases the total silicon area required by a factor of about 5 over that required by the processor the total silicon area required by a factor of about 5 over that required by the processor core alone, and power consumption triples.



ARM920T and ARM1020E CPU Cores:

These CPU cores, based on the ARM9TDMI and ARM10TDMI processor cores, have separate instruction and data caches. Each of the caches in the ARM920T contains 16k bytes and has 32-byte blocks, with 64-way set associativity. There is an MMU for each memory port, and each of them has a 64-entry associative TLB. The ARM1020E has 32K bytes in each cache; otherwise, the caches and the MMUs are similar.

Strong ARM SA-110 CPU Core:

The StrongARM CPU core was developed by ARM in collaboration with Digital Equipment Corporation (now folded into Compaq company), and the SA-110 version is manufactured by Intel. The processor component implements version v4 of the architecture. It does not support the Thumb instruction set. Otherwise, the processor is comparable to ARM9TDMI processor core. The performance of the strongARM SA-110 is comparable to that of the ARM920T, but it is implemented using an earlier technology and has higher power consumption at a 200-MHz clock rate.

The Strong ARM processor has a 5-stage pipeline. There are separate 16K-byte instruction and data caches. Each cache has 32-byte blocks and 32-way set associativity. The translation look aside buffers for each of the caches have 32 entries. The high-speed multiplier circuitry has a latency of three or fewer clock cycles, designed for good performance in digital signal processing application.

1) Present system in washing machine:

Traditional washing machine includes the following parts

i. Water control inlet valve ii. Water pump iii. Tub iv. Agitator v. timer vi. drain pipe and vii. Motor Proper coordination among all these parts is very essential to clean the clothes. This coordination requires a lot of artificial intelligence which comes from various electronic circuit/ components which are control from software's / programs. Many of these AI features can be implemented in the basic washing machine through the smart phones which are available with all hostess. The concept of controlling the motor speed of washing machine which couple to the disc through smart phone is our objective.

The single-phase current source is used for single-phase motor. The motor generates an inter-spares magnetic field. The armband produced is zero at zero speed. To start such a motor, it is necessary, besides a primary winding, to have an auxiliary winding to help to produce the phase-shifted magnet space. The accessory winding is placed in quadrature with the primary winding. The current flowing to the accessory

winding has to be phase shifted from the current flowing through the primary winding. There are numerous ways to do this.

Capacitor is usually connected in series with the auxiliary winding. Thus, we can generate magnetic flux of primary and accessory windings shifted 90° Such a field appears to rotate the same as for a field in three-phase motors. It permits motor to start rotating. When motor attains 70% speed the capacitor and accessory winding are disconnected. The motor continues to run on main winding with the help of centrifugal switch. For the washing machine high torque is required at the beginning, this can achieve with above configuration.

We can skip the centrifugal switch and capacitor when high starting torque is not required. Then circuit need to be designed for suitable capacitor and accessory winding. capacitor and an auxiliary winding have to be designed for continual operation.

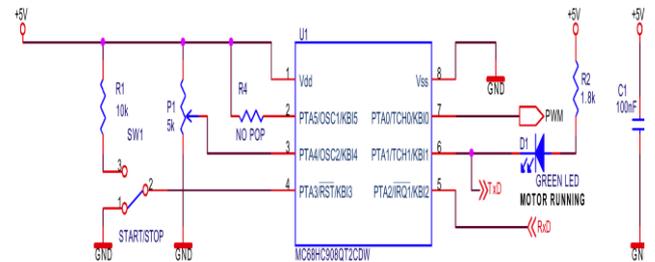
shaded-pole motor is used to start a single-phase motor. Starting winding and capacitor is not required for such configuration. A short copper rings are placed around the stator. In relation to non-shaded part the magnetic field of the shaded part of the pole is delayed. The motor start rotating when magnetic field start rotating. Shaded pole motors are very cheap when they produced in mass. Along with many advantages, they have number of disadvantages: low efficiency (below 20%), starting torque and high slip. They have a limited range of use, i.e. in small home appliances such as fans or blowers.

2) Varying Speed of Single-Phase Split-phase induction Motors:

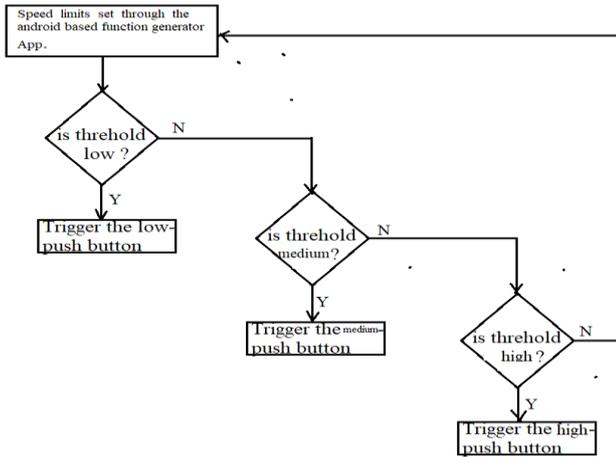
To control the speed of washing machine it is useful to use different technique to control the speed. This can be achieved by changing voltage amplitude and frequency (called volt-per-hertz control) or by the changing of supply voltage magnitude with constant frequency (slip control).

B. Controller Part

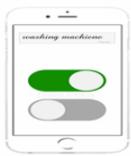
We know that washing machine uses split-phase induction motor. Speed control of these motors is accomplished by changing the magnitude of voltage given to the stator. This circuit is triggered by the push buttons which are activated by smart phones, according to the speed limit set in the program called Android Smartphone-Based Function Generator which is already available. For example, threshold values for speed limits can be defined as low, medium and high which in-turn triggers the corresponding switch button to activate the control circuit. Interfacing of smart phone and push button is done by 3.5 mm audio jack cellphone out pin.



II. RESULTS:



Flow chart for proposed method



III. CONCLUSION

With this idea the common man can use washing machine by paying very less amount. It works on a concept called low cost with high efficiency. It is cost effective and environment friendly. This system consumes very less power.

REFERENCES:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: "Computer Organization", TMH
2. William Stallings: "Computer Organization and Architecture", PHI, Pearson Education, Delhi, 10th Edition, 2016, ISBN: 9780134101613.
3. David. A. Patterson, John L. Hennessy: "Computer Organization and Design – The Hardware / Software Interface", ARM Edition, 5th Edition, Elsevier, 2014, ISBN: 97801240776263.
4. Abdullah Rashid, Zuakafal Nacem, Waqas Malik, ISBN-13: 978-3-8473-7956-0, ISBN-10:3847379569
5. LAP LAMBERT Academic Publishing (2012-11-25), ARM processor - a new era in low power application - ISBN-13: 978-3-659-30751-5
6. LAP LAMBERT Academic Publishing (2012-10-07), BLAKE Algorithm Evaluation on ARM Processor - ISBN-13: 978-3-659-24778-1
7. LAP LAMBERT Academic Publishing (2014-09-22), Computer Organization and Architecture - ISBN-13: 978-3-659-56212-9
8. Muhammad Ali Mazidi, Janice Gillespie Mazidi, Rollin D. McKinley: "The 8051 Microcontroller and Embedded Systems – using assembly and C", Pearson Publication, New Delhi, revised 2nd Edition, 2011, ISBN: 978-81-317-5899-1.
9. John Davies: "MSP430 Microcontroller Basics", Elsevier, 2008, ISBN: 978-0-7506-8276-X.
10. Kenneth J. Ayala: "The 8051 Microcontroller Architecture, Programming & Applications", revised 3rd Edition, Thomson Learning, 2005, ISBN: 81-315-0200-7.
11. V. Udayashankar and Malikarjuna Swamy: "The 8051 Microcontroller", Tata McGraw-Hill Education, 2009, ISBN: 978-0-07-008681-4.

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