Clock Delayed Dual Keeper Domino Logic Design with Reduced Switching

Anju Varghese, Anusha.S.R, A. Anita Angeline, Kanchana Bhaaskaran.V.S

Abstract: ***Clock Delayed Dual Keeper domino logic style with Static Switching mechanism (CDDK_SS) using delayed enabling of the keeper circuit and modified discharge path has been proposed in this paper. In CDDK domino circuit, the principle of delayed enabling of keeper circuit offers reduced contention between keeper circuit and Pull Down Network (PDN). The modified discharge path at the output node eradicates the switching at the output node for identical TRUE inputs during the pre-charge phase. This facilitates in obtaining static like output in contrast with conventional domino logic. The simulation results of Arithmetic and Logic Unit (ALU) subsystems demonstrate 17.7% reduction in dynamic power consumption while compared to conventional domino logic. Furthermore, 62% enhancement in speed performance has been achieved with good robustness. Design and simulation have been executed using Cadence® Virtuoso with UMC 90nm technology node library.***

Keywords: Domino logic, Keeper transistor, Static Switching Mechanism, High speed, Low Power Consumption

I. INTRODUCTION

Dynamic logic circuit occupies prominent position in digital designs due to high-speed performance and lower power consumption. The conventional domino logic circuits comprise the dynamic circuit structure with a static inverter at the output node. This makes the triggering of successive stages to be flawless. The domino logic circuit design with reduced number of transistors and NMOS transistors for evaluation makes the design to be more power efficient and offer comparatively faster performance [1].The keeper transistor M_2 has been incorporated to replenish the dynamic node against leakage-current and charge sharing. Depending on footer transistor inclusion, the domino logic circuit variants are classified as footed domino logic and footer-less domino logic circuits [2,3].

Domino logic circuit operation occurs in two phases as defined by the clock CLK signal. The pre-charge phase occurs when clock signal CLK is LOW and evaluation phase occurs when clock CLK is HIGH. Scaling up of keeper transistor size increases the robustness of the circuit. However, this increases the contention between keeper and PDN. This is due to the keeper circuit, which tries to retain the logic HIGH during HIGH input conditions to the pull-down network (PDN). This leads to decreased speed performance. To alleviate this issue, various domino logic structures are proposed in the literature [4-6].

Although, dynamic logic circuit offers reduction of area and increased speed, significant dynamic power consumption is high due to the output signal transitions at the output node during pre-charge phase even for consecutive HIGH inputs. The necessity to reduce the dynamic power consumption paved to various static switching mechanism design structures of domino logic such as Pseudo dynamic buffer (PDB) [8], Limited Switch Dynamic logic (LSDL) [9]. In PDB mechanism, during the second pre-charge phase, the discharge of the output node is prevented. This facilitates in retaining the previous evaluation output. Thereby, the switching at the output node is reduced.

This paper proposes clock delayed dual keeper with static switching (CDDK-SS), a control mechanism for the keeper to reduce contention current and also provides a static output. It is based on the delayed enabling of the dual keeper transistor arrangement using delayed inverted clock signal. The static inverter configuration at the output node prevents the discharge of the output node during the pre-charge phase. Section 2 details the domino logic operation, Section 3 elaborates the existing switching mechanism and Section 4 elaborates the CDDK domino logic design. Section 5 exhibits the design of CDDK-SS mechanism. Section 6 elaborates the design and simulation of CDDK-SS mechanism and Section 7 concludes.

II. DOMINO LOGIC CIRCUIT DESIGN

Fig.1 depicts the conventional domino logic which includes a PMOS transistor M_1 at the Pull Up Network (PUN) and NMOS transistors PDN connected according to the required logic along with the NMOS footer M_3. Thus, the number of transistors has been reduced from 2N to N+2 which decreases the power consumption and area.

When clock CLK is at LOW, pre-charge of the dynamic node Z to logic HIGH occurs through the PMOS transistor M_1. During this time evaluation network is OFF so that the pull down path is disabled. When clock is HIGH device M_1 turns OFF and M_3 turns ON. The dynamic node Z discharges based on the inputs and the PDN topology. The PMOS keeper transistor M_2 is used to compensate the charge leakage problem at the dynamic node [3].

If the PDN is FALSE, then the dynamic node Z should remain HIGH state due to the preceding pre-charge operation. However, this charge gradually leaks away due to leakage current. This leads to false computation of the output.

The function of the keeper transistor is to compensate for the charge lost due to the pull-down leakage paths. The keeper transistor tries to hold the charge even when the dynamic nodal charge tends to discharge through the PDN. However, this leads to

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increased contention between the PDN and the keeper circuit.

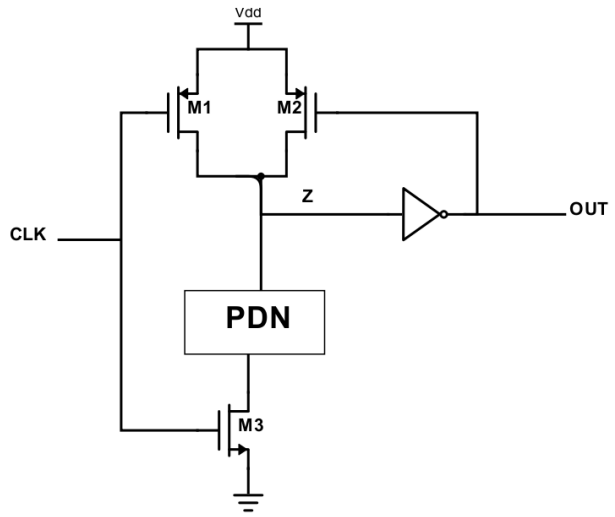

Fig.1 Conventional Domino Logic Structure

III. PSEUDO DYNAMIC BUFFER DOMINO LOGIC

Dynamic power consumption is very high in domino logic due to unwanted switching transients at the output node during pre-charge operation. To alleviate these switching transients and decrease the dynamic power consumption Pseudo Dynamic Buffer (PDB) was designed [8]. Fig.2 shows the PDB based domino logic. In the circuit structure, the source terminal of M_5 transistor is connected to the node A, which is the drain terminal of the footer transistor instead of grounding.

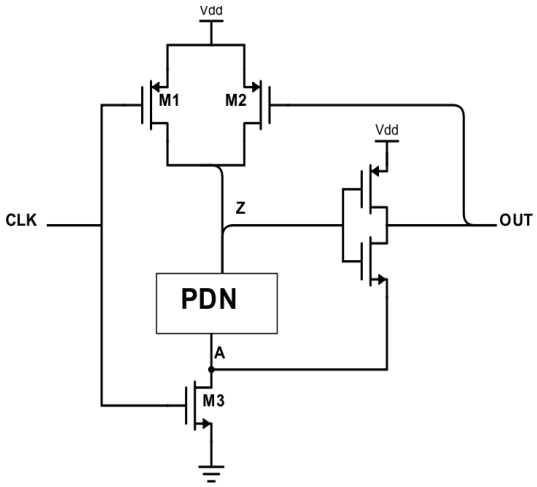

Fig. 2 Pseudo Dynamic Buffer Domino Logic

When the input to the PDN is LOW, the dynamic node Z does not discharge and stays HIGH, and the output is LOW in case of pre-charge and evaluation phases. While considering the inputs being HIGH, there arise two cases with respect to the state of clock. With the clock signal CLK as HIGH i.e. evaluation phase, node Z will discharge to ground and the output is HIGH. While clock is LOW, PMOS device M_1 is turned ON and dynamic node Z is charged to logic HIGH. Unlike domino logic, in PDB, the output remains HIGH since it is not able to discharge as the clock turns OFF the device M_3.

IV. CLOCK DELAYED DUAL KEEPER DOMINO LOGIC

Although, the switching is reduced in PDB, the problem raised due to the contention current is not eliminated. This mechanism explains how an extra keeper reduces the contention current [5]. Fig.3.depicts the Clock Delayed Dual Keeper (CDDK) domino logic where M_4 is the additional keeper with delayed inverted clock as input. The new keeper transistor $M_4$is kept in series with the conventional keeper. Pre-charge transistor M_1 will be in conducting mode when clock signal is LOW and the dynamic node Z will get charged to V_{dd}. During evaluation, i.e. when the clock signal is HIGH, the keeper transistor M_4 will be disabled, since the delayed inverted clock is given to the gate terminal. This facilitates the PDN to discharge with higher speed according to the input combinations. The problem of contention is thus reduced but power consumption is high due to increased switching at the output.

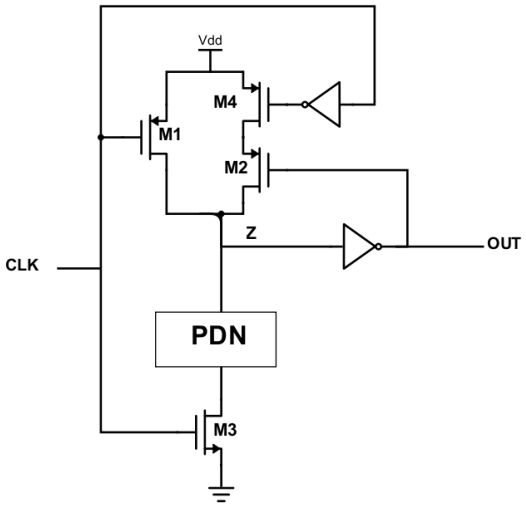

Fig.3 Clock Delayed Dual Keeper Circuit

V. CLOCK DELAYED DUAL KEEPER WITH STATIC SWITCHING MECHANISM

The proposed Clock Delayed Dual Keeper domino with static switching mechanism (CDDK-SS) inherits the advantages of both pseudo dynamic buffer (PDB) and conventional CDDK. As in PDB, the source terminal of M_5 is connected to the drain of footer transistor M_3. Because, of this the unnecessary switching during pre-charge phase is eliminated.

Fig.4 shows the proposed clock delayed dual keeper with static switching mechanism. It should be noted, that the OUT node is completely isolated from the ground during the pre-charge phase. This results in reduction of switching power. In addition, the contention reduction technique as in CDDK is employed by using an extra keeper circuit with delayed enabling of clock.

At ideal conditions, the dynamic node Z should remain HIGH during evaluation phase. However, this charge gradually leaks away due to the OFF state transistors. This results in incorrect operation of the gate. To avoid this, a pull-up device called keeper or bleeder M_2 is used to retain the charge during evaluation phase when the PDN is OFF. However, the keeper transistor

tries to retain the charge at the dynamic node even while the PDN evaluates TRUE condition. Thus, the contention arises between PDN and keeper device.

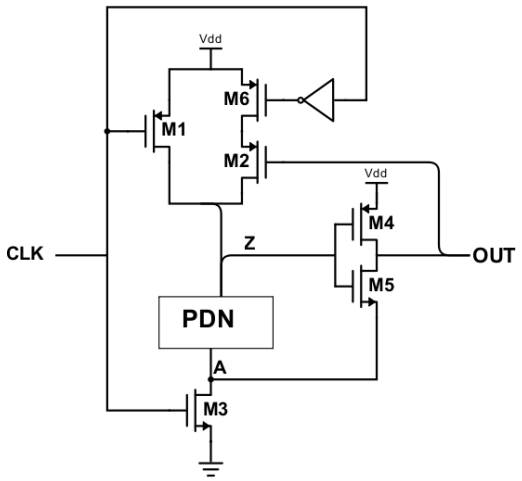

Fig. 4 Clock Delayed Dual Keeper with Static Switching Mechanism (CDDK-SS)

VI. ARITHMETIC LOGIC UNIT (ALU) - SUB SYSTEM DESIGN

For analyzing the CDDK static switching mechanism, designing of the subsystems of Arithmetic and Logic Unit (ALU) is performed. The motive for considering ALU subsystems being that ALU is the primary block of a processor. Thus if the power consumption of ALU is reduced that in turn reduces the power consumption of processor [10, 11]. ALU includes arithmetical and logical blocks. Logical block consists of OR, AND, NAND, NOR, XOR and XNOR operations. Fig.5 depicts the AND gate design using CDDK-SS logic where the PDN topology is the basic AND configuration along with delayed enabling of the keeper transistor and modified discharge at the output node. Similarly, Fig. 6 depicts the OR gate design using CDDK-SS. Consider the clock being low, which turns on M_1 transistor and then the dynamic node Z charges to Vdd. When clock is high the delayed keeper M_6 is disabled in the initial part. This enables faster discharging of node Z when inputs are high. After this short delay M6 will be enabled and then charge retention is determined by M_2. Arithmetic block consists of Adder/ Subtractor and Multiplier [12].Fig.7. depicts the Adder / Subtractor unit, where the same full adder unit is reconfigurable for adder and subtraction operation. Operation to be performed is deciphered using decoder circuit based on the instruction mnemonics. Since there are 8 operations considered, a 3:8 decoder is preferable for the ALU design. The 3-bit input to the decoder is the 3-bit MSB from the OPCODE of an instruction. A 3 x 8 decoder is implemented using all the four logics explained above for the comparison.

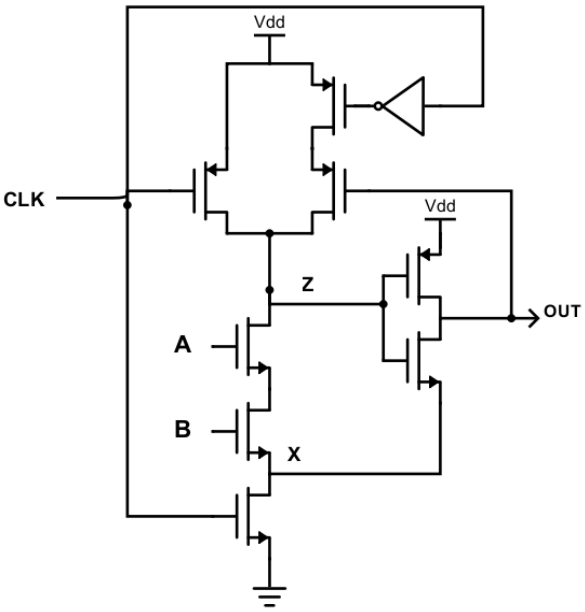

Fig.5 AND Gate Design Using CDDK –SS

The arithmetic block includes add/sub unit and multiplier units. Using add/sub unit it is possible to compute both the sum and difference of 2 inputs. The block diagram for a 4 bit add/sub is given in Fig.7.

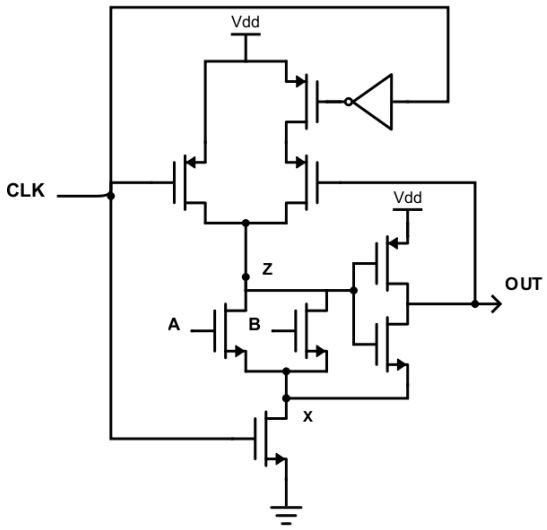

Fig.6 OR Gate Design Using CDDK –SS

Additional XOR gates used to perform both the addition and subtraction operations. Consider the input C_0, if C_0 is given as zero then this block will perform the addition of inputs A and B. If C_0 is one then it computes the compliment hence, if the input B is provided then it performs the subtraction operation.

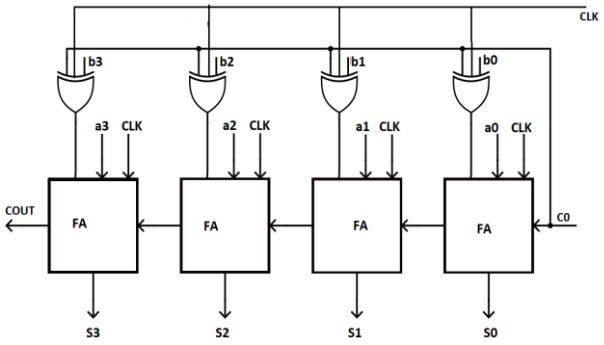

Fig.7 Block Diagram of ADDER /SUBTRACTOR

For multiplication, an array multiplier [6] is designed using half adder and full adder blocks as depicted in Fig.8. An array multiplier is preferred for its regular uniform architecture. The structure of array multiplier shows that the multiplication is done by shifting and adding. Each multiplier bit is multiplied with the multiplicand and the partial products are generated. These partial products are shifted according to the multiplier bit order and are added.

A multiplexer has several inputs and a single output is obtained, which is one among the inputs according to the select lines.Fig.9. depicts the 32:1 multiplexer which is designed using five 8x1 multiplexers. For a multiplexer having N select lines there will be 2^N inputs.S

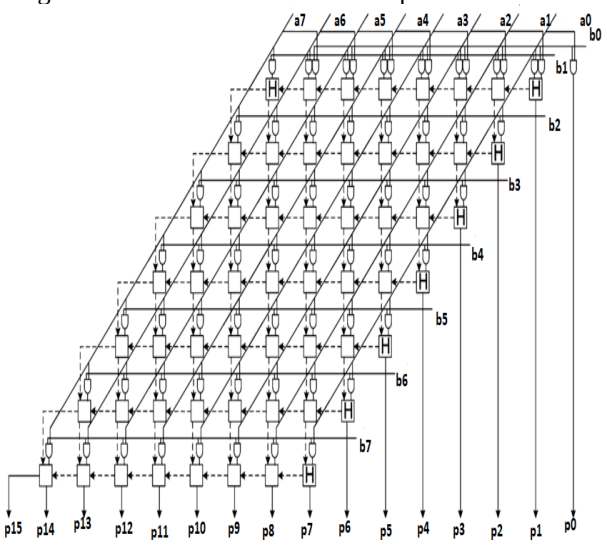

Fig.8 Array Multiplier Design

VII. SIMULATION RESULTS AND ANALYSIS

Design and simulation of ALU sub systems are carried out using Cadence® Virtuoso using UMC 90nm technology library. Table 1 given below shows the power and delay of various wide fan-in circuits. Fig.10. depicts the transients of the OR gate using domino logic where there is increased switching at the output. Fig.11 in contrasts depicts the reduced switching at the output node.

Table 1 details the comparison of power consumption and delay between conventional domino, CDDK logic and proposed CDDK-SS mechanism for various benchmark circuits.

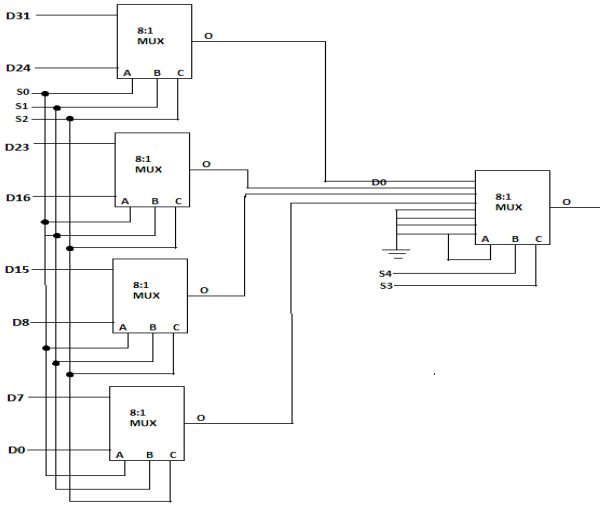

Fig.9 32x1 Multiplexer

It can be inferred, that the CDDK-SS have less power consumption and delay while compared with the dynamic logic. Conventional domino logic has power consumption of 59.65µW for 256 bit OR gate and using CDDK domino logic it is reduced to 57.16µW.Further using CDDK-SS mechanism it is reduced to a value of 49.09µW.

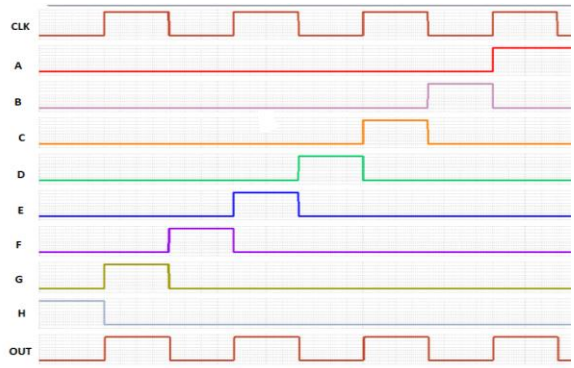

Fig.10 Output Waveform of Domino Logic for OR gate

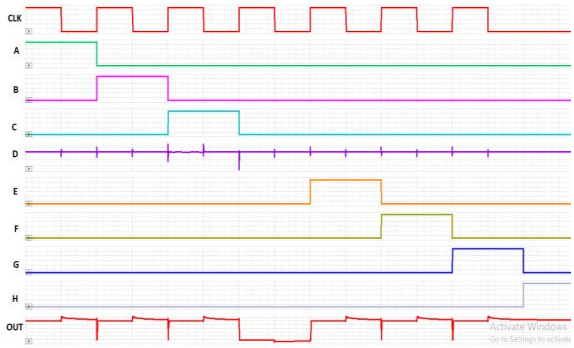

Fig.11 Output waveform of CDDK –SS Mechanism of OR gate

The output waveforms of decoder using domino logic and CDDK_SS are illustrated in Fig. 12 and Fig.13 respectively. A large amount of reduction in the delay can be observed in all of the given circuit irrespective of number of bits.

Table 1: Power and Delay for various Wide Fan-In Circuits

Circuit	Conventional domino		CDDK Logic		CDDK Static switching mechanism	
	Power (µW)	Delay (ps)	Power (µW)	Delay (ps)	Power (µW)	Delay (ps)
16-0R	3.71	76.74	3.45	64.65	2.92	49.74
32-OR	8.07	24.23	7.49	19.49	6.25	15.71
64-OR	3.34	260.5	3.276	250.6	2.8	95.55
128-OR	27.4	307.3	26.32	304.0	22.7	271.9
256-OR	59.65	940.1	57.16	937.1	49.09	357.1

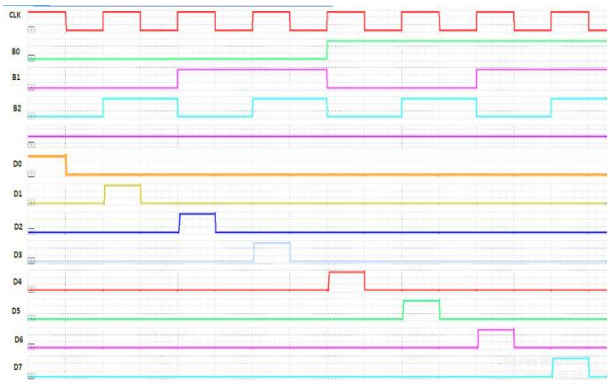

Fig.12 Output Waveform for Decoder using Domino Logic

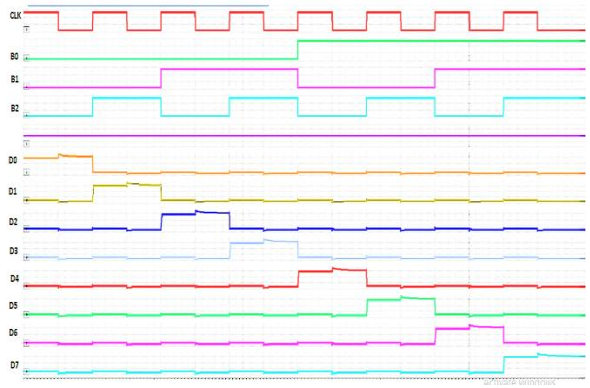

Fig.13 Output Waveform for Decoder using CDDK-SS Mechanism

Examining the case of 256 bit OR gate itself it is visible that the delay of 940.1ps in dynamic logic is reduced to 357.1ps in CDDK_SS mechanism. In the similar way, the power and delay of decoder used for the ALU subsystem design is shown in the Table 2.

This reduction in power consumption is due to the elimination of pre-charge stage and speed increases because the delay caused by the contention in domino logic is avoided. This reduces the contention in spite of the additional keeper device. The addition of a new PMOS transistor will lead to slight increase in the power consumption, but this is negligible in the case of wide fan-in circuits.

Table 2: Comparison of Power Consumption and Delay for Decoders

Logical Styles	Power(µW)	Delay(ps)
Conventional domino	19.04	220.4
Pseudo dynamic buffer	11.93	123.03
CDDK Domino	20.33	107.4
CDDK –SS Domino	18.34	90.13

From Table 2 and Fig.14 it is inferred that the proposed CDDK static switching mechanism has less delay compared to other domino logic styles.

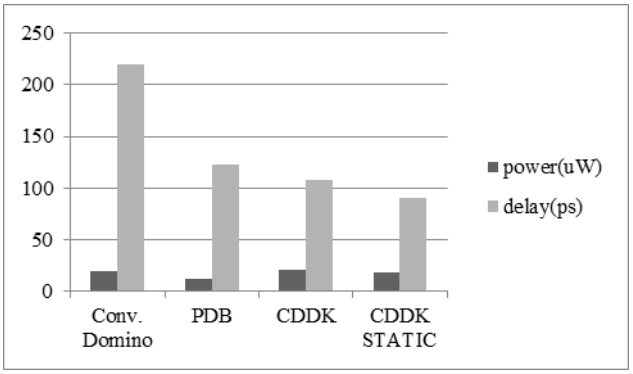

Fig.14 Comparison of Power and Delay of Decoder using various domino logic topologies.

Table 3: Power Consumption and Delay Comparison of 32 x 1 multiplexers

Logic	Power(µW)	Delay(ps)
Conventional domino	*191.1*	574.1
Pseudo dynamic buffer	148.1	363.4
Conventional CDDK	204.7	313.4
CDDK static switching mechanism	198.9	273.8

The proposed CDDK static switching mechanism shows lesser delay proving reduced contention and avoiding switching. The CDDK_SS offers reduced power consumption and less delay as depicted in Table 3.

VIII. CONCLUSION

The unnecessary switching during the pre- charge phase of the domino logic is eliminated by connecting the source terminal of NMOS transistor of the output inverter to the drain terminal of footer transistor in CDDK_SS mechanism. This avoids discharge of the dynamic node during pre-charge operation and thereby reduced switching at the output node is reduced. The delayed enabling of the keeper circuit also reduces the contention current. The incorporation of these principles, offers increased speed performance with reduced power consumption. It is observed that for a 128 bit OR gate the power consumed has decreased from 27.4µW to 22.7µW and

the delay has been reduced from 307.3ps to 271.9ps.These results confirms that proposed clock delayed dual keeper with static switching mechanism offers high speed with low power consumption.

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