Performance Analysis of Modified High Voltage Gain Boost Converter for PV-fed LED Lighting Applications

Pydikalva Padmavathi, Sudhakar Natarajan

Abstract: ***Nowadays, the development of PV (Photo Voltaic)-fed LED (Light Emitting Diode) lighting technology is requires high gain ratios with efficient performance of the converter. The presented converter topology is non-isolated possess high gain voltage with low stress voltage. The design of the modified high voltage gain boost configuration is projected with continuous current at input, which is flexible to control. The conduction, switching loss at the switch, reverse recovery problem and electromagnetic interference are mitigated due to low duty cycle. But to explore the differentiation of their characteristics, advantages and several reasonable evaluations are carried out. The operating principle, theoretical analysis and experimental results of modified high gain step-up converter are provided for PV-fed LED lighting applications to verify the efficient performance in all aspects.***

Keywords: ***Solar PV, Boost Converter, High Gain, PWM Controller, LED Lighting.***

I. INTRODUCTION

In present scenario, high gain boost structures are extensively using in several applications. Due to the un-sufficient generation of the electricity, the proper usage of available energy is necessary at this situation. In this case, PV (Photo voltaic) fed dc-dc boost structures plays a key role in various fields of LED (Light Emitting Diode) lighting applications. Nowadays the literature review is greatly discussing and concentrating on the proposals regarding efficient techniques and methods to enhance the efficient PV fed LED lighting systems [1-2]. LED lighting is promising technology accepted as a new generation of lighting source for different fields of applications with long lifespan and its energy saving [3-4]. Solar PV is primary renewable energy source, which protects from environmental pollution. The photovoltaic panels are available in the market with reasonable cost and reducing day by day continuously. PV fed DC-DC converter for power electronics applications is the most important aspect, and it depends on the efficiency, component reliability, and its maintenance [5]. One of the key factors affecting the PV fed system for LED applications is

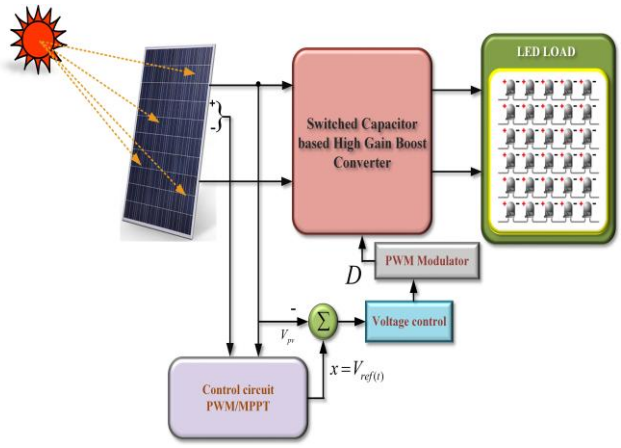

Fig.1 Block diagram of modified high voltage gain boost converter

the proper selection and design of the dc-dc structures utilized. In order to implement PV fed LED lighting system, the conventional design uses several dc-dc converters with different drawbacks such losses in the power semiconductor devices, switch voltage stress, very less voltage gain and so on. The different considerations are there in order to propose high gain boost converter is low cost, high efficiency of power conversion, size and complexity. There are some approaches are to produce high gain voltage in dc-dc converters. Switched capacitor, switched inductor, Voltage-lift cell, coupled inductor, voltage multiplier cell is integrated with traditional dc-dc topologies to rise the gain. Dickson and Cockcroft multiplier cells are utilized to improve the voltage of the converters. To analyze the performance of the converters, Dickson and Cockcroft multiplier cells are incorporated in the step up converters [6,7]. The voltage conversion ratio of the configuration is raised by accumulating coupled inductor to the structure of converter and is presented in [8]. This causes to improve the components count. In the literature step up converter with integration of coupled inductors are analyzed [9,10]. Still, the usage of multiple coupled inductors gives complications in the analysis of dynamic configurations. F.L.Luo et.al introduced ultra-gain structures by voltage-lift cells [11, 12]. However, high voltage conversion ratio is attained with re-lift and self-techniques but with high number of components [13,14]. To attain high voltage gain more than two methods are incorporated and combines it advantages for effective performance.

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In order to reduce switching losses quasi resonant operation is employed and switched capacitor cell is combined with coupled inductor to derive high gain converter. Hybrid switched inductor is employed in symmetrical and asymmetrical converters for PV fed applications [15]. However, various topologies are investigated above by adding extra elements to the traditional configurations. This paper introduced a high gain structure with simple modification in the existing topology. The foremost aim of the proposed effort is to model high voltage gain boost converter with mitigated losses comparing to the traditional converter and can be suitable for PV-fed LED lighting applications. The design of the existing configuration presented here i.e., high gain boost converter with voltage lift technique [16]. The proposed converter is modified with addition of one capacitor and shifting place of one diode. The clear analysis of the modified converter proves that the extreme stress voltage across all the passive elements and power semiconductor devices are lower related to the quadratic high gain step up converter. Mostly, the comparative analysis can be done based on stress voltage, reliability and volume. Usually input current of all conventional quadratic dc-dc configurations are naturally discontinuous, which causes to inject ripples in to the converter and complicates the structure for the requirement of filters. But the novel design of the proposed topology's input current is continuous in nature. The presented converter has wider voltage gain than that of existing converter and converter is using only one power switch. The operation of the structure with continuous input current, which can simplify the structure of the topology without filters.

The paper systematized as monitors: Section II presents the PV panel process and its specification requires for the LED load requirement. Section III provides the working principle of the projected converter topology with continuous inductor current and explains the steady state presentation of the model is analyzed with efficient MPPT controller. Section IV, which is followed by the comparison between the conventional and modified converter. Section VII. Theoretical waveforms and investigational results from a prototype made in the laboratory are explained. Section VIII concludes the paper.

II. MODELLING OF SOLAR PANEL

The basic corresponding structure of the photovoltaic cell is described in Fig.2. This structure is also named as four parameters model, which the current source of the PV cell represents the generated light current, shunt resistance signifies the leakage current to the ground, series resistance corresponds to the internal electrical losses and the diode is signifies the nonlinear impedance. Theoretical model of the PV cell structure is having diode connected in anti-parallel with the source current. When the radiation of sun falls on the PV cell, the direct current develops that can varies with solar radiation [17].

Applying Kirchhoff current law, PV cell's current at output side.

$$I_{pv} = I_{ph} - I_d - I_{sh} \quad (1)$$

The diode current I_d is given by

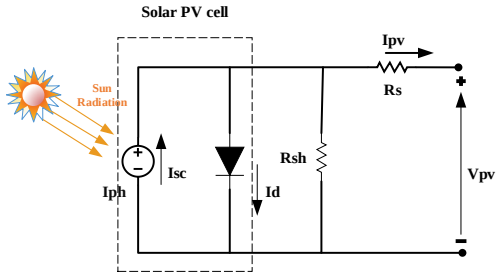

Fig.2. Equivalent circuit of Solar PV cell

$$I_d = I_s\left(e^{\frac{q(V_{pv}+R_sI_{pv})}{mkT}} - 1\right) \quad (2)$$

The current flowing through the resistance at shunt is I_{sh} is

$$I_{sh} = \frac{V_{pv} + R_sI_{pv}}{R_{sh}} \quad (3)$$

The generated light current varies with solar radiation and temperature is given by the expression [18]-[19].

$$I_{pv} = I_{ph} - I_s\left(e^{\frac{q(V_{pv}+R_sI_{pv})}{mkT}} - 1\right) - \frac{V_{pv} + R_sI_{pv}}{R_{sh}} \quad (4)$$

Where
T Temperature coefficient of Kelvin
K Constant of Boltzmann 1.3865×10^{-23} J/k
I_{ph} Generated light current (Amps)
I_s Diode's reverse saturation current (Amps)
R_{sh} R_s Resistances connected in shunt and series respectively (Ω)

PV cell's current at output side is

$$I = I_O \times N_p \times I_{ph} - N_p \times \left[e^{\left(\frac{V/N_S + I\times R_S/N_P}{m\times V_t}\right)} - 1\right] - I_{sh} \quad (5)$$

$$I_{sh} = \frac{V \times N_p/N_S + I \times R_S}{R_{sh}} \quad (6)$$

Where N_p &N_S are the number of cells connected in parallel and series correspondingly.

III. ARRANGEMENT OF THE CONFIGURATION

Figure 3(a) & 3(b) presents the existing quadratic boost structure and modified quadratic boost configurations correspondingly. The adjustment prepared in the existing quadratic boost configuration by adding one capacitor and shifting the place of one diode. The number of passive components in quadratic boost converter is five, and it is six in the proposed topology. The diode count in the existing and proposed converter is same.

The structure generally comprises of four capacitors, three diodes, two inductors, load, and a switch. The several advantages of the adjustment made in the topology are conferred in section IV. Figure 4 delivers the different operating modes of the presented configuration.

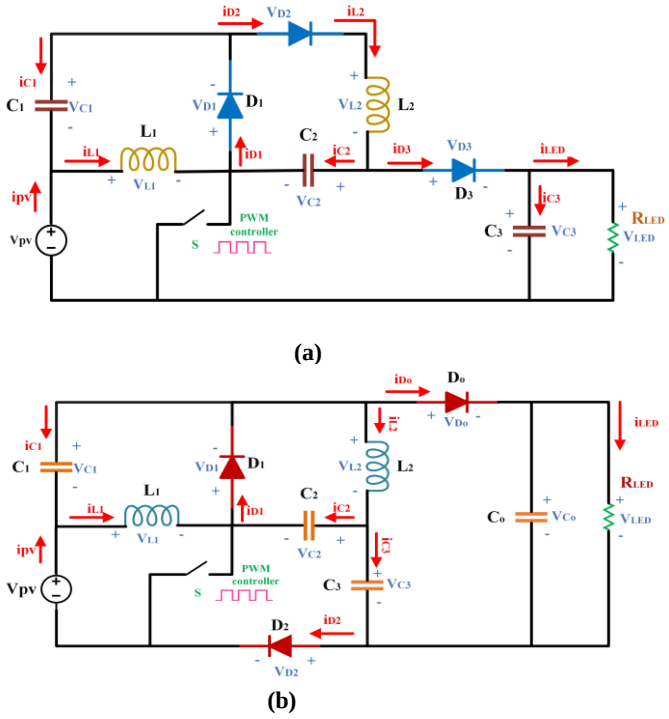

Fig. 3(a). Quadratic boost converter 3(b). Proposed converters

Mode 1: at this interval of time ($0 \le t \le t_o$) the device is in conduction state and the path for current flowing for the switch 'S' as presented in the figure 4(a). When the switch S is ON the diodes D_1 & D_2 are reversely conducted by the negative polarity of the source voltage over the switch. Diode D_o is conducted in forward direction. Inductor L_1 is directly connected to solar PV voltage V_{pv}. The current i_{L1} is increases linearly from lowest value to extreme value. Due to its energy storage is increased, as a outcome inductor L_2, capacitors C_1 and C_2 are in series and are connected to V_i. The inductor L_2 also starts rises from least value to supreme value. Also the capacitor voltage C_1 is reduced from its extreme value to least value, capacitor voltage C_2 is improved from its minutest value to extreme value and capacitor voltage C_3 is reduced from its supreme value to tiniest value.

Mode 2: Figure 4(b) the current path is still in conducting state at the interval ($t_o \le t \le t_1$), the switch S is ON position, the diodes D_1, D_2, & D_o are reverse biased due to polarity reversal of the input voltage over the power switch. The current over inductors L_1 and L_2 are in increased level reaching to its maximum value. Also, the voltage and energy stored in the capacitors C_1, C_2 and C_3 remains constant.

Mode 3: At this time interval of time ($t_1 \le t \le t_2$) Figure 4(c) gives the path of the current passing when the switch S is non-conducting state. Diode D_1 & D_o are reversely conducts and D_2 is forward conducted, the inductor L_1 is connected C_2, C_3. The inductor L_2 is associated in series with C_1, C_2 and L_1. Then, the current flowing over the inductor L_1, L_2 are starts to reach their minimum values. The capacitor voltage C_1 continuous it's discharging state. Where, the capacitor Voltages C_2 and C_o are starts to rise in negative direction and the capacitor C_3 gets charged linearly.

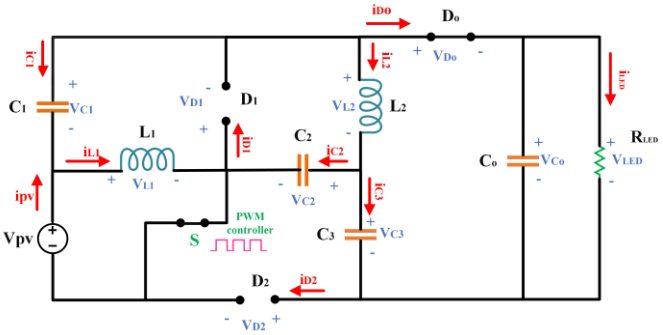

Fig 4(a). Mode 1 ($0 \le t \le t_o$)

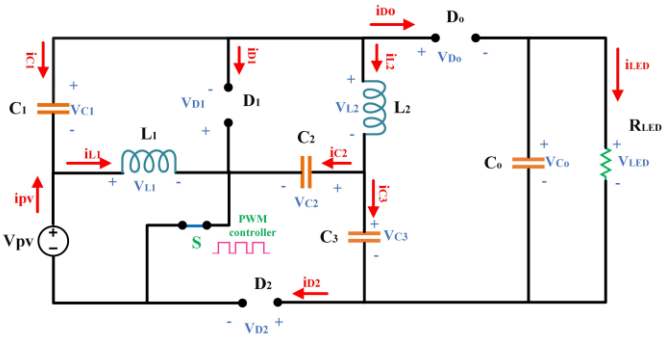

Fig 4(b). Mode 2 ($t_o \le t \le t_1$)

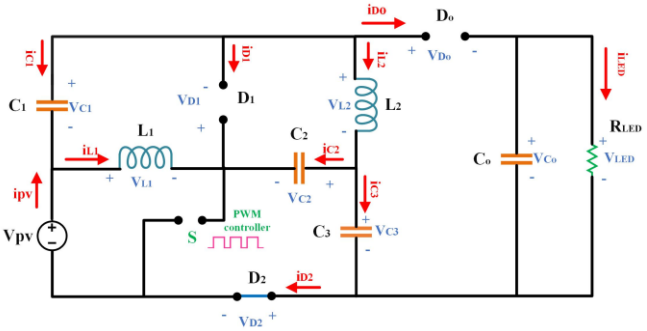

Fig 4(c). Mode 3 ($t_1 \le t \le t_2$)

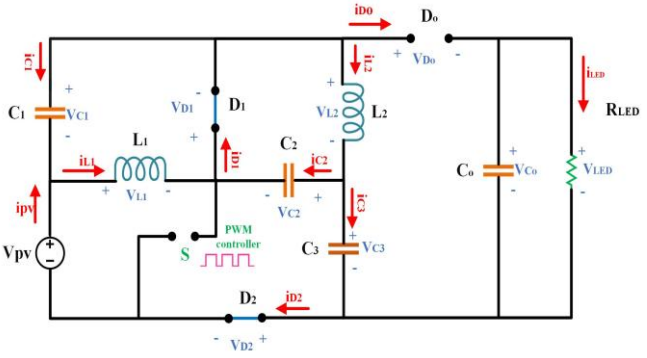

Fig 4(d). Mode 4 ($t_2 \le t \le t_3$)

Mode 4: During this interval of time ($t_2 \le t \le t_3$) figure 4(d) gives the path of current flowing when the switch S in OFF position. The diodes D_1, D_2 are conducted in forward direction and D_o is goes to reverse biased condition.

The currents flowing thorough the inductors L_1, L_2 are almost reaches to the minimum value. The solar PV current flows through the series combination of C_2, C_3 over the diode D_2 to the input source. The capacitor C_1 voltage is equal to voltage across capacitor C_2 and inductor L_1 is also equal to the voltage across inductor L_2. As a outcome, the capacitor voltage

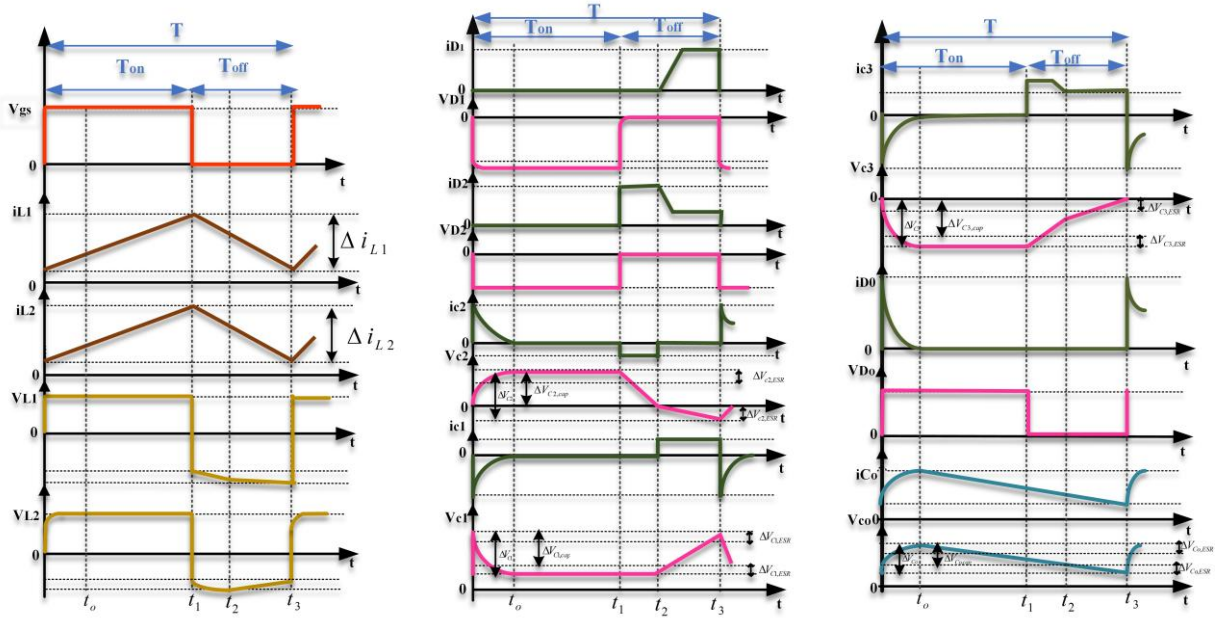

Fig. 5. Theoretical Waveforms of Proposed Converter

C_2, C_o are reduced to their minimum value. Meanwhile, the energy stored of the capacitor C_3 is increased to its peak value. Throughout this period, the capacitor C_1 is parallel to the inductor L_1, thus the voltage is increased to its high value. In this situation, the inductor current L_1 and energy stored in that is goes minimum value. Since the load energy provides the parallel path L_1, L_2, C_1, C_2. The theoretical waveforms of respective modes of operations are represents as exposed in figure 5.

A. Design calculations of the configuration

By applying KVL for the circuit as shown in figure 4(a) & 4(b) is given by eq (7)&(8)

$$V_{L1} = V_{pv} = L_1 \frac{di_{L1}}{dt} = L_1 \frac{\Delta i_{L1}}{T_{on}} \tag{7}$$

$$V_{L2} = V_{pv} + V_{C1} - V_{C2} = V_o - V_{C3} = L_2 \frac{di_{L2}}{dt} = L_2 \frac{\Delta i_{L2}}{T_{on}} \tag{8}$$

where V_g, V_{L1}, V_{L2}, V_{C1}, V_{C2} V_{C3}, V_o are the voltages of the source, L_1, L_2, C_1,C_2, C_3, and C_o respectively. i_{L1}, i_{L2} are the currents through the inductor L_1, L_2 respectively during switch S is ON position.

By applying KVL for the circuit as shown in figure 4(c) & 4(d) is given by eq (9)&(10)

$$V_{L1} = V_{pv} + V_{C2} - V_{C3} = -V_{C1} = L_1 \frac{di_{L1}}{dt} = L_1 \frac{\Delta i_{L1}}{T_{off}} \tag{9}$$

$$V_{L2} = -V_{C2} = L_2 \frac{di_{L2}}{dt} = L_2 \frac{\Delta i_{L2}}{T_{off}} \tag{10}$$

Where V_g, V_{L1},V_{L2},V_{C1},V_{C2}.V_{C3}, are the voltage across input source voltage, the inductor L_1, L_2, capacitors C_2, C_3. i_{L1}, i_{L2} are the currents through the inductor L_1, L_2 during switch S is OFF position.

By relating volt-sec balance principle for inductor L_1, L_2 using eq.(7)-(10), is given by eq.(11)&(12)

$$\frac{1}{T_S}\left(\int_0^{DT_S} V_{pv} + \int_{DT_S}^{T_S} (-V_{C1}) dt \right) = 0 \tag{11}$$

$$\frac{1}{T_S}\left(\int_0^{DT_S} (V_{pv} + V_{C1} - V_{C2}) + \int_{DT_S}^{T_S} (-V_{C2}) \right) = 0 \tag{12}$$

By solving equation eq.(11) and (12), the capacitor voltage C_1, C_2 we get V_{C1} and V_{C2} values as follows. Voltage gain

$$= \frac{V_O}{V_{pv}} = \frac{V_{pv} + V_{C1} - V_{C2} + V_{C3}}{V_{pv}} = \frac{2}{1-D} \tag{13}$$

Where $V_{C3} = V_{pv} + V_{C1} + V_{C2}$ (14)

Current gain $\frac{I_o}{I_{pv}} = \frac{1-D}{2}$ (15)

B. Efficient algorithm for control circuit

Incremental conductance (INC) method is introduced to overcome the weakness of perturb & observe technique such as at fast varying atmospheric conditions it's difficult to measure the peak power. INC can stop the perturbation of the operating point and able to define the value of MPP. If the situation is not satisfied, the operating points perturbation can be calculated by using relation dI/dV and I/V. This relation is determined from the details that when the MPPT is right to the position of MPP then dP/dV is negative and if it is left side to the position of MPP then dP/dV is positive. The incremental conductance method can able to track fast varying irradiation conditions accurately than P and O method [20].

We have

$$P = VI \tag{16}$$

By applying the chain rule, we get $\frac{\partial P}{\partial V} = \frac{[\partial[VI]]}{\partial V}$ [17]

At MPP, $\frac{\partial P}{\partial V} = 0$ (18)

The eq.18 can be stated in expressions of array current and voltage i.e.,

$$\frac{\partial I}{\partial V} = \frac{-I}{V} \quad (19)$$

From the PV characteristics the power curve is zero at MPP, right to the MPP is decreasing and left to the MPP is increasing. The equations can be represented as follows.

At MPP, $\frac{\partial I}{\partial V} = \frac{-I}{V}$ (20)

Left to the MPP, $\frac{\partial I}{\partial V} > \frac{-I}{V}$ (21)

Right to the MPP, $\frac{\partial I}{\partial V} < \frac{-I}{V}$ (22)

The PWM modulation signal of the high gain boost structure can be regulates the MPPT tracking till the situation $(\partial I/\partial V)+(I/V)=0$ is fulfilled.

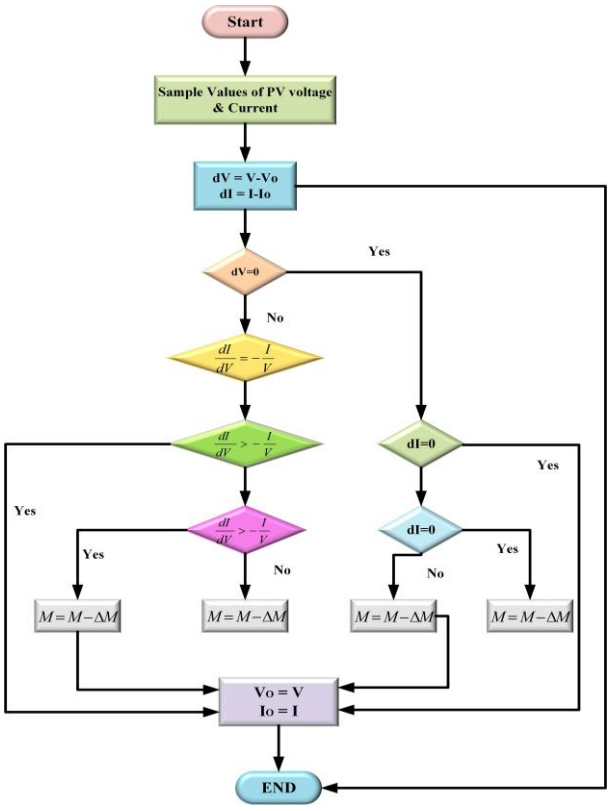

Fig.6. Flowchart of Control Algorithm

The comparison between traditional and presented converter comprising the voltage gain, number of elements, stress and ripple voltage of the both configurations are obtainable. Conferring to the figure 7(a), figure 7(b) it can be state that the introduced converter have the high voltage conversion ratio at less duty cycle with condensed ripples. The duty cycle of converter is less in two modes of operation. The efficiency of the converter around 98%., the ripple current and voltage are also reduced.

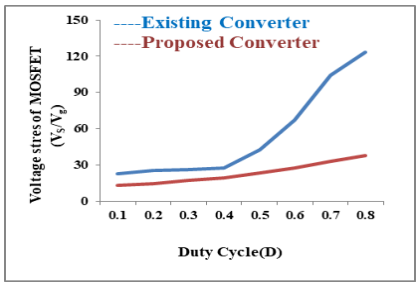

Fig. 7(a). Stress voltage versus duty cycle

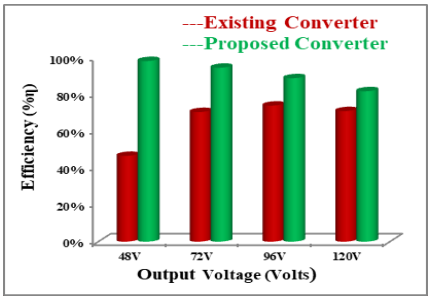

Fig. 7(b). Output voltage versus efficiency

Figure 7(a) clearly enlightens the stress voltage and ripple amount of the introduced structure is less than that of the traditional converter. The relation displayed in Figure 7(b) observed that the efficiency of the presented configuration with output voltage is high associated to the existing boost converter. The supreme efficiency of modified high voltage gain boost converter is approximately 97%.

IV. EXPERIMENTAL RESULTS

In accordance with design equations and circuit analysis, a prototype configuration has been modelled and verified. The outline of design considerations are mentioned as follows: 120Watts, 48V, 2.5A LED array is considered for street lighting applications as a design example. The specifications of the converter for the following input and output V_{pv}=12V, V_o= 48V, P_o = 120W and f_s=20 kHz. The main advantage for the circuit is due to the switched capacitance the circuit works always in continuous conduction mode operation. The two inductor values L_1 & L_2 are chosen as 5mH & 2mH with ESR of 20mΩ & 15mΩ respectively. Whereas the capacitors values C_1, C_2, C_3 are set to 110µF with ESR of 15mΩ and output capacitance C_o value is 63µF with ESR of 10mΩ. MOSFET IRFP460PBF is used as a switch S and diode MUR1560 are utilised for the diodes D_1, D_2 & D_o. The power switch S is operated by the TLP250. A Aplab regulated dual power supply LD3210 is used as the source to the input in the hardware implementation.

The differential probes of kind PINTEK DP-25 is used to measure the voltage and probes of type CHAUVIN ARNOUX E3N are used to measure current. All the result waveforms from hardware experiment are recorded by the digital storage oscilloscope of type DSO-X 3014A as shown in fig.8(a), 8(b).

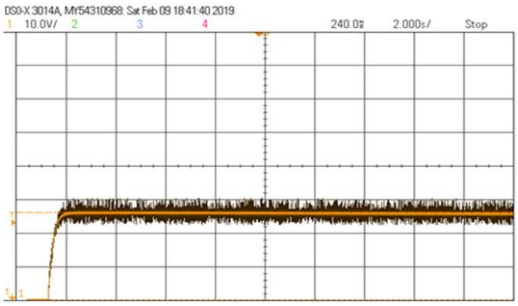

Fig. 8(a). Output Voltage of introduced converter to the LED load
V_{LED} =47.65V

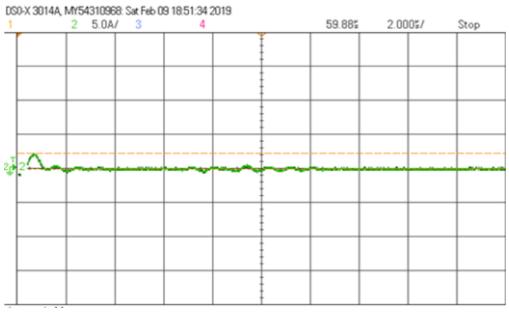

Fig. 8(b). Output Voltage of introduced converter to the LED load
I_{LED} =2.482A

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