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Time Amplifier Based Bang-Bang Phase Frequency Detector in 0.18µm CMOS Technology

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Abstract*: *A CMOS Implementation of Time amplifier (TA) based Bang-Bang Phase Frequency Detector (BBPFD) using Sense amplifier based flip flop (SAFF) is presented in this paper using 0.18µm CMOS technology. A time amplifier based on feedback output generator concept is utilized in minimizing the metastability and increasing the gain of TA which in turn boosts the gain of Phase Frequency Detector (PFD). Also, a modified SAFF was built in CMOS 0.18µm technology at 1.8V which further reduces the hysteresis and metastability aspect related to PFD. The proposed PFD works at a maximum frequency of 4GHz consuming 0.46mW of power with no dead zone.

Keywords*: *Time amplifier, BBPFD, SAFF.

I. INTRODUCTION

In today's communication world, the permissible bit error rate of a system defines the transmission and reception of data. In recent times all digital phase-locked loops (ADPLL) have been in the forefront in communication system for the reason of being scalable, immune to noise, offering lesser design complexity and avoiding many passive components thus reducing the overall chip area. Analysis of ADPLLs, either in locked state or in transient state will reveal two most important parameters that will define the performance of ADPLL; they are lock time and timing jitter. ADPLLs being a closed loop system, the efficacy of such system strongly relies on the proper functionality of its individual components. Detectors play a vital role in many applications such as delay alias-locked loops, digital-microwave radio, clock and data recovery circuits and phase-locked loops (PLLs). Phase detectors are sensitive to the phase difference between two signals on input and frequency detectors are sensitive to the frequency difference on its input. If incoming signals are with the same phases then phase detectors are not sensitive to frequency and vice versa. Basically the PDs can work as FD but with limited range. A phase-frequency detector (PFD) being one of such mature detector circuits that is used to detect both phase and frequency differences of reference and feedback signals and plays a vital part in defining lock-in time. PFDs have two modes of operation viz. *linear and nonlinear modes*. Several literatures have revealed DFF and 2XOR based PFDs, which are linear PFDs but have low timing jitter during locked state and they suffer from prolonged locking method [1]. They are also sensitive to process variations. On the other hand Non linear PFDs [2-3] being one of the alternatives to linear PFD offer high gain but high reset delay and non zero dead zone are major concern. From the literature it can be found that Phase detectors either fall in any one of the category viz, analog PD, digital PD, Dynamic PDs and Binary PD. The most common digital PD being XOR based PD (double balanced mixer) [4], has (i) limited pull in range which demands an additional frequency acquisition circuit, which otherwise makes the locking very difficult, (ii) the dependence of linearity on the duty cycle error. Dynamic PDs are having good jitter performance but they are not sensitive to duty cycles, where as binary PDs have better locking process but they suffer from large timing jitter under locked condition. Bang-bang phase detectors being binary phase detectors, a 2-level bang-bang phase detector with a phase quantization error of $\pi/2$ and phase detection range of $-\pi/2 < \Delta\Phi < +\pi/2$ samples the data using three samplers [5]. The lock state occurs at $\Delta\Phi=0$. On the other hand the 4-level bang-bang phase detectors proposed in [6] lowers the phase quantization error to $\pi/4$ at the cost of five samplers. Thus it can be clearly seen that the performance of bang-bang phase detectors depends upon the speed of the DFF-samplers that are being used. Ideally the output of Phase detector alternates between +1 and -1, i.e. the oscillations are under driven and over driven in every alternate cycle by same amount, thus the average of output frequency will be constant while the phase will be periodically toggling resulting in phase error that in turn generates a limit cycle which has a period two fold that of the reference clock [7]. The performance of loop with respect to jitter and spur is dictated by the presence of limit cycles. We can describe the limit cycles by their radius expressed in number of clock cycles. The loop jitter performance is degraded, every time the radius increases. Several investigations performed [8], [9] have focused towards finding the source of limit cycle and to minimize them.

II. MOTIVATION

The mixed mode design of Phase locked loops (PLLs) typically uses time-to-digital converter (TDC) as one of the solution to overthrow PFD, instead of a linear phase detector, and a digital loop filter.

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Typically a high resolution TDC consumes more power and creates complications in the design. Several TDC-based structures like Pseudo-differential TDC**,** time amplifier TDC have been reported to minimize the real estate of chip and improvising the time resolution. However, ADPLL with TDC is quite complicated and consumes more power. The following observations have motivated to come out with novel architecture of PFD.

a) The property that the output of PD is active in full reference
period makes the entire PLL noise performance dependent on PD noise performance.

b) In applications where only high-frequency phase noise is of interest, a wide loop bandwidth can be accommodated in an ADPLL with a simple bang-bang phase detector (no TDC). However, more generally in ADPLLs with wide loop bandwidth, it is desirable to have very fine TDC resolution. [10].

c) But, the TDC design being complicated with limited resolution has a chance of entering into non linear region very soon. Thus it loses its advantage over BBPFD. Moreover it is a power hungry device.

d) The BBPFD also has the issues of metastabilty with reference to the kind of flip flops being used [11].

e) A simple bang–bang phase-frequency detector (BBPFD) alleviates the issues created by TDC. However, the strong dependency on jitter along with addition of quantization noise and random noise creates difficulties for BBPFDs.

f) An alternative to BBPFD was proposed in [12] using multi-phase bang-bang detector (MPBBD) which quantified its analysis w.r.t cycle slipping behavior.

g) In [13] automatic loop gain control mechanism was adopted to enhance the lock time using 1-bit TDC. However, the control circuitry used was very complex, resulting in large real estate and more power consumption.

h) Further to our survey it was found that on top of quantization noise, BBPFD itself introduces some sort of random noise into the system. Hence it is advisable to go with a time-amplifier (TA) based PFD [14].

The above observations motivated us to come up with a novel PFD architecture that not only has high gain but the impact of non-linearity caused by metastability is reduced. Hence the advantages of TA and BBPFD are combined to obtain this novel PFD.

III. TIME DIFFERENCE AMPLIFIER

The proper description of Time difference amplifier (TDA or TA) was reported earlier in [15], which consisted of two mutual exclusive circuit i.e. MUTEXs. These MUTEX comprises of a SR latch along with XOR gate as shown in figure 1. The traditional time amplification process relies majorly on the metastabilty aspect of SR latch along with positive feedback. Whenever the time gap between two rising edges becomes very narrow in terms of pico seconds. The problem of non linearity arises very quickly.

Many TDAs have been presented in the literature over past few decades that try to mitigate this issue of non linearity, but the problems still remains as a hot cake for research. One such solution was proposed in [16] by assigning time delay to either of inputs to SR latch, but the time delay will always limit the linearity of the input range.

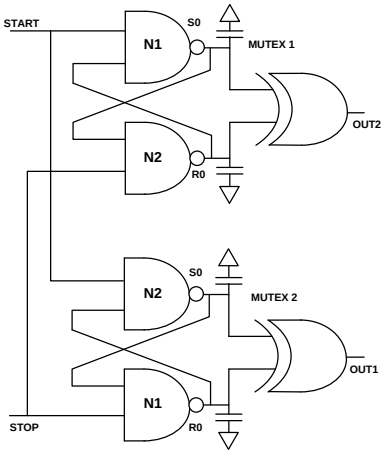

Fig. 1 Traditional TDA [15]

SR latch forces the values R_0 and S_0 to either one or zero. Generally the output regeneration time and inputs have a relationship [16] expressed as

$$\Delta T_{OUT} = \tau * (\log (V_{TH}) - \log \left| \alpha * \Delta T_{SR} \right|) \quad (1)$$

Where α is a proportional factor, τ = C/gm is time constant where C gives the value of node capacitance consisting of both capacitances of NAND gate and XOR gate, gm being transconductance and V_{TH} is the threshold voltage of MOSFETs. ΔT_{OUT} is log function of ΔT_{SR}. The final TA gain is given by $G = \frac{2C}{T_{td}}$ where T_{td} is input range.

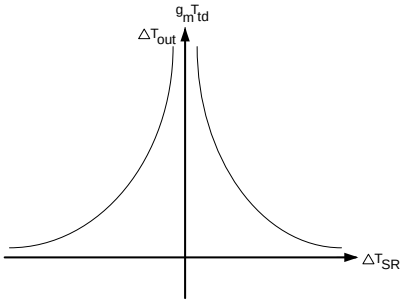

Fig 2. Output time of MUTEX versus input time differences of S-R latch

Here in this brief, a TA with the concept of feedback is proposed which can achieve high gain using the concept of feedback output generator whose functionality resembles that in [15]. We realize the increase in output regeneration time by the addition of a buffer and two feedback keeper circuits between EXOR gate and SR latch. Later this time amplified signal is used as input to BBPFD which is built using modified SAFF based Flip flop.

The time gap between the rising edge of IN1 and IN2 is considered as TA's input. If IN1 rises to VDD before IN2, then Tin is regarded as positive else negative.

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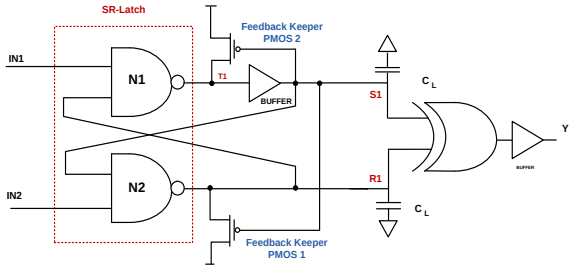

Fig. 3 Feedback output generator that is employed in TA

At the beginning of operation both IN1 as well as IN2 are at lower potential thereby holding the voltages at node S1, T1 and R1 equal to VDD hence feedback keepers are switched off.

Case 1: IN1 rises to VDD at t0 and Tin is positive

Under this condition T1 is pulled to ground faster when IN1 goes to VDD. VS1 (VS1= voltage at node S1) also goes to zero after some delay and VR1 remains at VDD.

Case 2: IN2 rises before t1

At time t1 PMOS-1 and PMOS-2 turns on. Before the rise of IN2 to V_{DD}, VS1 slowly decreases until it is equal to $V_{DD} - |V_{THP}|$, which turns ON the two feedback keepers. In the mean time, VT1 is pulled to V_{DD} due to turning on of PMOS-1. Here, VR1 is dependent on IN2. Therefore there is a possibility of VR1 getting reduced to ΔV if IN2 rises before t1 i.e. even before PMOS-2 is on. But VR1 will remain at V_{DD} if IN2 rises after t1.

From the timing diagrams in Fig. 4(a) and 4(b), it can be seen that the discharge action of VR1 is dependent on rising edge of IN2. Hence, smaller the Tin larger will be ΔV and large ΔV means discharging of capacitor is quick. The entire process of feedback will be happen during the time when the current through the PMOS-2 is constant (diode connected). At this point of time both, IN1and IN2 will be held at V_{DD}.

IV. BBPFD USING TIME AMPLIFIER AND MODIFIED SAFF

The literature has clearly suggested that good metastability in DFF is very essential in the design of BBPFD. Hence sense-amplifier-flip-flop (SAFF) is selected to realize the DFF in BBPFD. Because of the memory effect during sampling process, the conventionally used SAFF has a hysteresis effect, affecting the jitter performance. The kickback effect resulting in slave stage to master stage can be eliminated by isolating the two stages as shown in Fig. 6(b). Event the clock is delayed for slave stage. The hysteresis of the modified SAFF is evaluated to 11fs as shown in Fig. 7, which is way less than conventional SAFF. Fig. 8 indicates the correctness in the output of modified SAFF which takes care of metastability.

PFD used in ADPLL does the phase comparison between reference clock and feedback clock. Fig. 9 depicts TA+BBPFD architecture. Fig. 10 shows the TA+SAFF based BBPFD architecture. According to the requirements of BBPFDs metastability and gain of BBPFD, slight changes have been incorporated that helps us to measure the phase error. The start and stop signal marks the beginning and end of phase error. Signal Dir, indicates the sign of phase error. When the phase of TA_{OP} leads that of TA_{ON}, Dir signal outputs 1, conversely Dir outputs 0 when TA_{OP} lags that of TA_{ON}.

The equation (2) and (3) depict the relationship between various signals of SAFF based PFD

Start = ~Dir * DN + Dir * UP (2)

Stop = ~Dir * UP + Dir * DN (3)

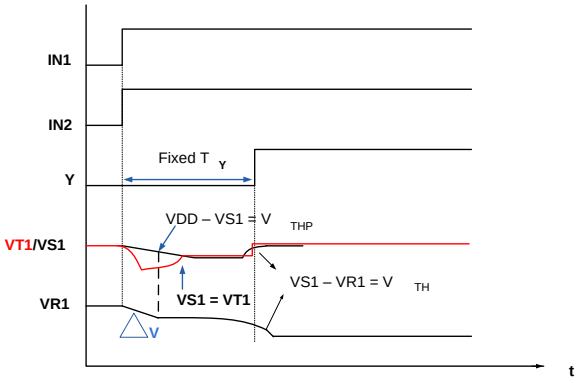

Fig. 4(a) Timing diagram of IN1 and IN2 with respect to ΔT (ΔT=0)

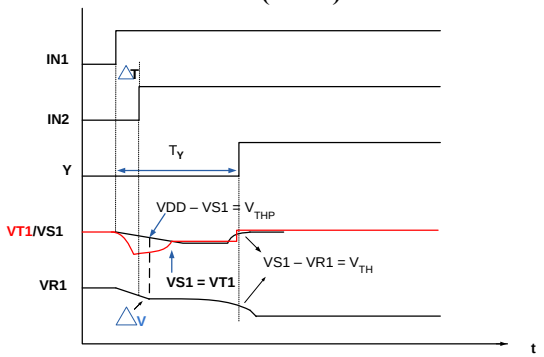

Fig. 4(b) Timing diagram of IN1 IN2 with respect to ΔT (ΔT>0)

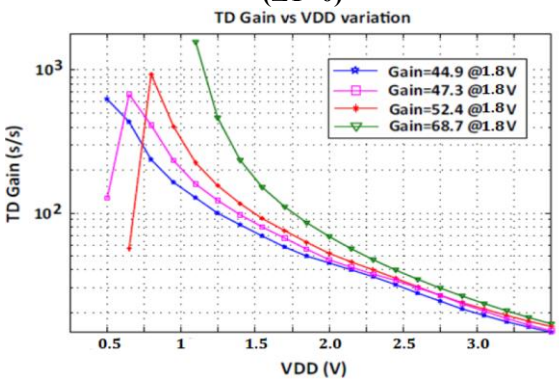

Fig. 4(c) Effects of V_{DD} on Time Difference (TD) amplifier gain.

Fig. 5 shows the designed time amplifier using the concept of feedback output generator.

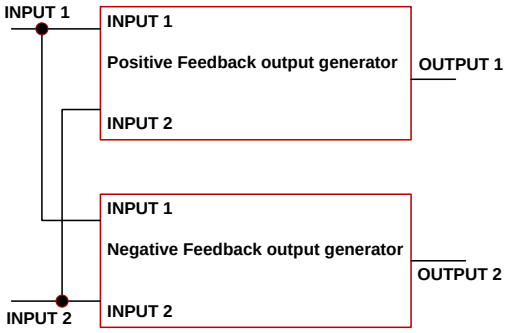

Fig. 5 Time amplifier with feedback output generator

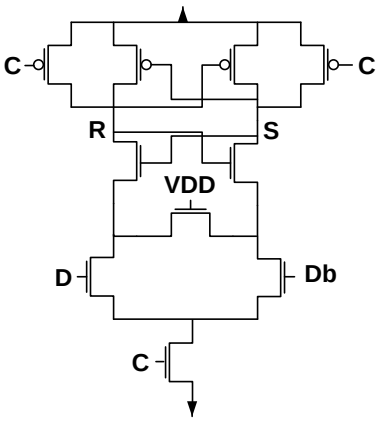

Fig. 6 (a) Schematic of Conventional SAFF

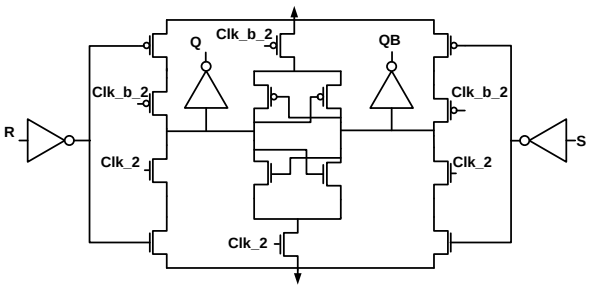

Fig. 6(b) Schematic of modified SAFF in slave stage.

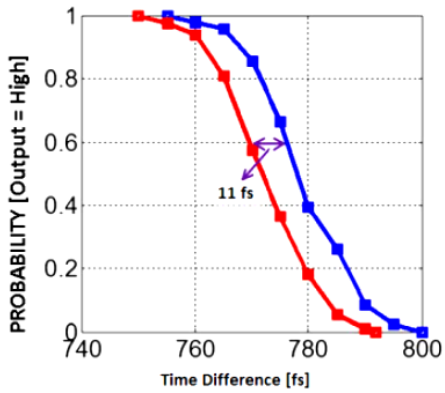

Fig. 7 Result of Transient noise simulation depicting hysteresis of modified SAFF.

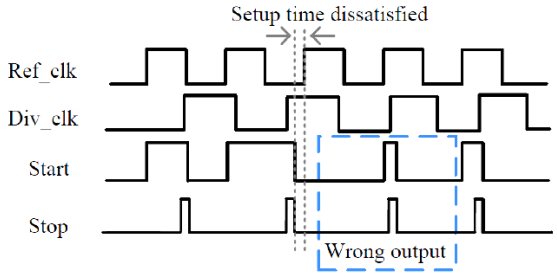

Fig. 8(a) Waveform of Typical DFF based PFD

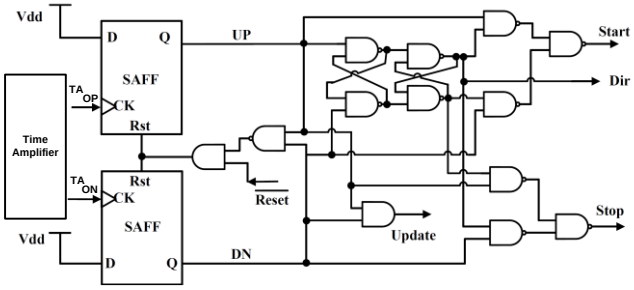

Fig. 10 TA+SAFF based BBPFD architecture

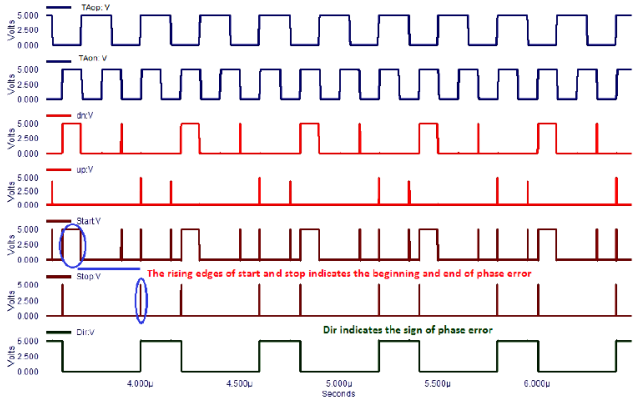

Fig. 11. Final waveforms of TA+SAFF+BBPFD

V. CONCLUSION

A Time amplifier based bang-bang phase frequency detector (BBPFD) is implemented using Sense amplifier flip flop. Due to the non linearity of BBPFD and the metastabilty of flip flops, it becomes very necessary to choose the right flip flop in the design of PFD which over comes the issues of metastabiity. Hence modified sense amplifier based DFF was built in this paper.

BBPFDs are most common alternative to the power hungry TDC. But the non linearity of BBPFD makes the gain of PFD to fall down. Hence in this paper it was very clear to build a PFD with high gain. The summary of results depicted in Table.1 justifies the work. Many Time Amplifiers have been presented in the literature over past few decades try to mitigate this issue of non linearity, but the problems still remains as a hot cake for research.

Further, the mismatch effects related to of MOSFETs parasitic capacitance results in variation of gain and many time offset issues are also generated. These areas also can be explored as a further research.

Table I. Pfd performance chart

Performance Parameter	Results
CMOS tech (µm)	0.18µm
Power consumption (mW)	0.46 mW
Power supply	1.8V
Gain	34 - 256
Max freq. (GHz)	~4 GHz

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