Design of Beyond Millimeter Wave Oscillator in 22nm Bulk CMOS technology

Nithin M, Harish M. Kittur

Abstract: ***This paper presents the design of an LC oscillator using inductive feedback technique in bulk CMOS 22 nm technology using predictive technology models. The core oscillator is based on the popular Cherry Hooper amplifier topology. The development of the oscillator circuit from the standard Cherry Hooper topology is discussed in this paper with detailed analysis. The inductors are modelled by considering the various effects in this frequency range. The broadband technique used in the CH topology enables the circuit to oscillate at frequencies more than millimeter wave regime. By employing MOS varactors the designed oscillator was converted into a voltage-controlled oscillator also. The fundamental mode of the oscillator is around 372 GHz with a phase noise measured around -70 dBc/ Hz at 10 MHz offset. The VCO has a tuning range of about 490 MHz when the voltage is varied from 0.3 to 0.8 V. The oscillator circuit consumes power of 3.75 mW from a power supply of 0.8 V.***

Keywords: Cherry Hooper, Millimeter Wave Regime, Phase Noise.

I. INTRODUCTION

The 19th century marked the foundation of millimeter wave (MMW) technology. The Scottish mathematician James Clark Maxwell predicted the possibility of radio waves. Later Heinrich Hertz confirmed the existence of radio waves. Measurements at MMW were done first by Jagadish Chandra Bose in 1890s. After the birth of transistor, especially CMOS technology and its possibilities at higher frequency led to tremendous growth in wireless communication especially in the areas of remote sensing, radar, missile guidance. With the invention of integrated circuit technology and its developments on CMOS transceiver chipsets, MMW circuits gained much attention.

Today by the evolution of mobile communication and its deep impact in the life of millions of people the possibility of MMW and the range beyond MMW are generating a lot of research interest. The phenomena of people to thing communication by the developments of cellular communication from analog cellular 1G to present generation mobile networks influenced the human generation in a deeper way than any other developments. The current IoT boom, which aims at connecting people and objects anywhere at any time will be enabled mainly by 5G. 5G will further improve our quality of life.

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The key benefits of moving to MMW frequency range and beyond are more bandwidth and smaller chip size. For any communication device, transceiver is an integral part which helps in transmission and reception of signals and the processing of it. Fig 1 shows the general block diagram of a receiver. The design challenges at MMW are more compared to the design at lower GHz range, especially in the key blocks like Low Noise Amplifier, Voltage Controlled Oscillator, Phase Locked Loop and Power Amplifier.

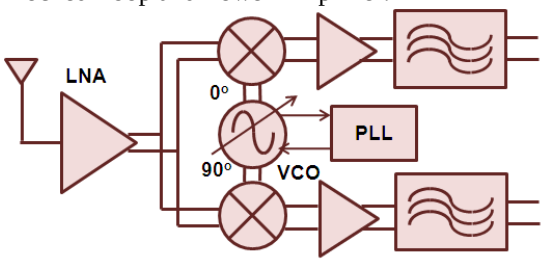

Fig. 1. General block diagram of a Receiver

The crucial block, PLL in the transceiver and the phase noise measured at the output of the PLL limits the maximum spectral efficiency of the entire transceiver system. The phase noise of the PLL depends mainly on its circuit blocks. VCO is one of the main constituents for the phase noise. Therefore, designing a low phase noise VCO is a challenging task at MMW regime. Many attempts are made in the past to achieve a low phase noise VCO from an LC based oscillator in MMW regime.

This paper proposes a Beyond MMW LC based oscillator (BMMWO) designed in 22 nm CMOS technology. The oscillator core uses the famous Cherry Hooper broadband amplifier technique to oscillate at extremely high frequency. The work also introduces tuning methods to make use of the designed oscillator as a VCO. The rest of the paper is organized as follows. Section II presents the circuit description of the BMMWO, section III brings the analysis of the topology and inductor modelling used in the simulation, section IV discusses the simulations and section V concludes the paper with future scope.

II. FUNDAMENTAL CIRCUIT DESCRIPTION

The basic Cherry Hooper amplifier circuit uses a drain to gate feedback as a broadband technique. To arrive at the basic CH topology, consider the CS amplifier stage with inductive load as shown in the Figure 2.

The use of inductive loaded CS stage ensures the operation with low supply voltages.

The inductor resonates with the total capacitance at the output and thereby operates at a much higher frequency compared to the resistive load counterpart.

The gain of the circuit in Figure 2 is

$$\frac{V_{out}}{V_{in}} = -g_m Ls$$

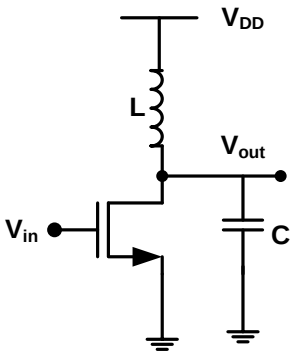

Fig. 2. Inductive loaded CS amplifier

Generally, to avoid tradeoff between the gain and bandwidth in a CS amplifier with resistive loaded circuit, a simple CD stage is inserted, to reduce the effect of the miller cap of the successive stage not to affect the bandwidth. A similar approach is done and drain to gate feedback is given to the basic CS amplifier using an inductor to arrive at the topology in Figure 3.

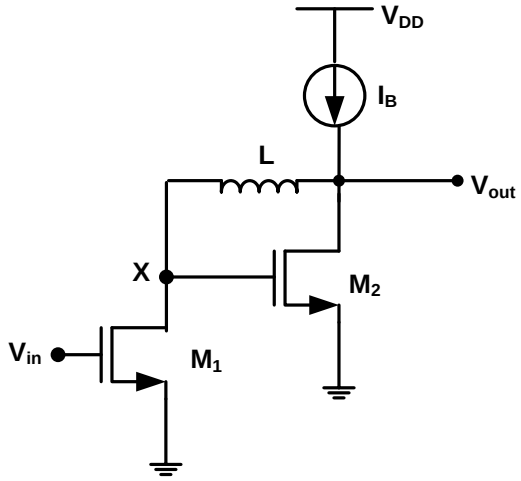

Fig. 3. Amplifier topology with inductive feedback

The inductor L establishes feedback by sensing the output voltage and returns a proportional current to node X. The voltage gain of the circuit can be obtained as

$$V_{out} - g_{m1} V_{in} sL_1 = V_x$$

It follows that

$$g_{m2} V_x = -g_{m1} V_{in}$$

$$\frac{V_{out}}{V_{in}} = -g_m Ls - \frac{g_{m1}}{g_{m2}}$$

The key advantage of the circuit lies in the small signal resistance at the output node and node X. This pushes the poles of the circuit to a much higher frequency enabling the circuit to operate at MMW range and beyond. Figure 4 shows the equivalent circuit of a inductive loaded voltage amplifier using Cherry Hooper topology with parasitic capacitances at both nodes.

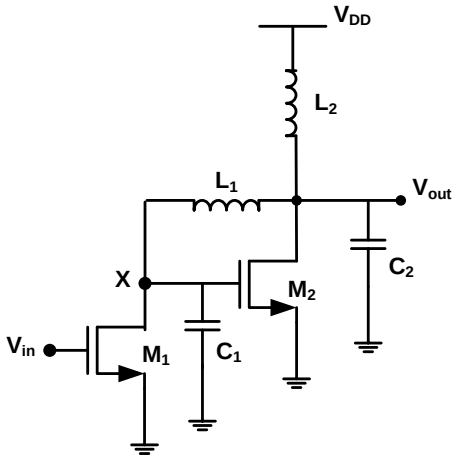

Fig. 4a. Voltage amplifier based on Cherry Hooper topology

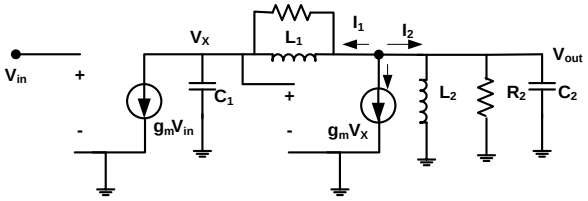

Fig. 4b. Equivalent circuit of the amplifier

Applying KCL at the output node of Figure 4b by assuming $C_1 = C_2 = C$, $L_1 = L_2 = L$ and $R_1 = R_2 = R$ gives

$$I_1 + I_2 + g_m V_x = 0$$

$$\frac{Cs(R + Ls)}{RL^2C^2s^2 + R} V_{out} + \frac{(RLC\,s^2 + Ls + R)}{(RLs)} V_{out} + \frac{g_m(R + Ls)}{RL^2C^2s^2 + R} V_{out} \approx 0$$

This gives the condition of transconductance as

$$g_m \cong \frac{3\sqrt{5} + 5}{2} \cdot \frac{1}{R}$$

$$g_m \cong \frac{5.85}{R}$$

This value of gm places the circuit at the edge of oscillation when configured connected as an oscillator with suitable feedback. Figure 5 shows the single ended oscillator topology which can oscillate beyond MMW range and hence called as Beyond Millimeter Wave (BMMW) Oscillator.

The equivalent circuit aids to obtain the transfer function, to achieve a loop gain of unity for sufficient oscillations under equal transconductance for both MOSFETs as

$$H(s) = \frac{g_m Ls\left(g_m Ls - \frac{Ls}{R} - 1\right)}{L^2C^2s^4 + 3\frac{L^2C}{R}s^3 + \left(3LC + \frac{L^2}{R^2} + g_m\frac{L^2}{R}\right)s^2 + \left(2\frac{L}{R} + g_m L\right)s + 1}$$

From the transfer function, we obtain the oscillation frequency as

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{2 + 2\,g_m R}{3LC}}$$

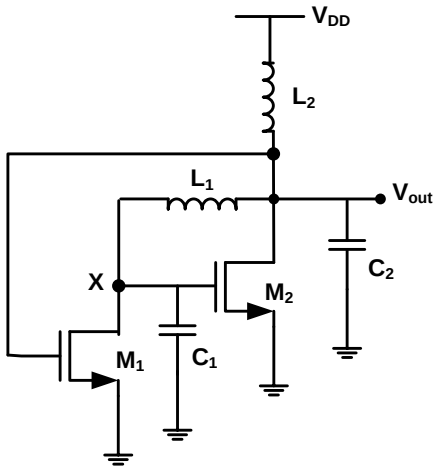

Fig 5 Single ended BMMW Oscillator topology

The differential topology of BMMW oscillator can be obtained by extending the circuit in Figure 5. The feedback polarity offers oscillation at a particular frequency.

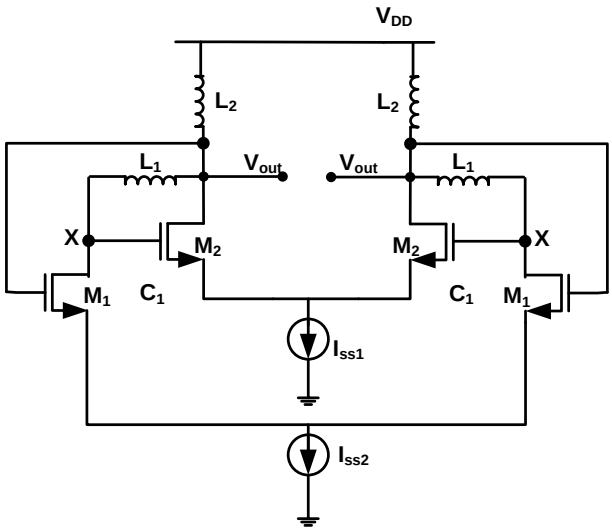

Fig 6 Differential BMWWO

III. CIRCUIT ANALYSIS

This section presents the analysis of the circuit described in the previous section in terms of the reactive elements. All the parasitic elements are accounted for the analysis. To arrive at the pole frequencies of the passive network, transistor is omitted and a current source is used to drive the network. The equivalent circuit by including the parasitic capacitance of the transistors at input and output node is as shown in Figure 7. The capacitance C is the sum of Cgs, Cds and Cdb.

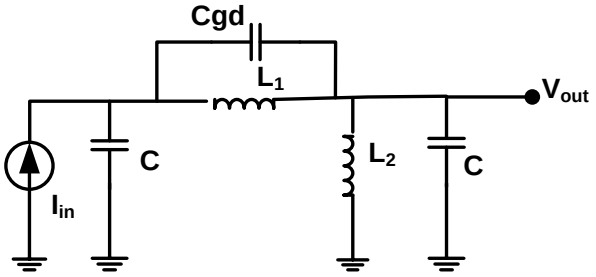

Fig 7. Equivalent circuit of the oscillator topology expressed in terms of passive elements

The circuit may contain four poles. It will be complex conjugate in nature.

$$\omega_{p1-4} = \sqrt{-\frac{1}{2(L_1||L_2)C} - \frac{1}{2L_1C} \pm \sqrt{\frac{1}{4((L_1||L_2)^2C^2)} + \frac{L_2 - L_1}{2L_1^2L_2C^2} + \frac{1}{4L_1^2C^2}}}$$

A. Inductor Modelling

This section presents the inductor model used for the design. To develop a model of inductor for simulations various effects need to be considered. The metal losses can be represented by a series resistance Rs, but this is valid for only a limited range of frequencies. The losses can also be modelled using a parallel resistance Rp. To enhance the available bandwidth, a combination of these two resistances is used and the model is shown in Figure 8.

$$R_s = \frac{L_1\omega}{2Q}$$

$$R_p = 2QL_1\omega$$

$$Q = \frac{L_1\omega R_p}{L_1^2\omega^2 + R_s(R_s + R_p)}$$

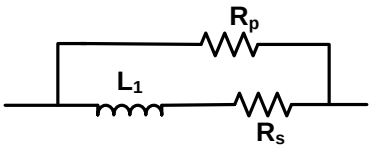

Fig 8 Inductor model representing losses

IV. SIMULATION RESULTS

The working of the oscillator in beyond MMW range is confirmed through various simulations in Cadence Virtuoso using Spectre simulator. This section presents the results of all the circuits pertaining to the development of differential BMMW Oscillator.

A. DC Analysis of Single ended BMMWO

The dc operating points of the transistors in the oscillator circuit is tabulated in Table1. The relevant parasitic capacitance of the transistors is also evaluated by the dc analysis. All the capacitance is in femto or atto farad range. The simulated power consumption of the circuit is 3.9 mW

TABLE 1. DC Operating point of transistors

Transistor	g_m (mA/V)	I_D (mA)	(W/L)
M1, M2	4.954	2.438m	1.76 µ / 22n

TABLE 2. Structure capacitance of transistors

Transistor	C_{gs}, C_{gb}, C_{gd}	C_{ds}, C_{db}
M1, M2	1.4 fF 20 aF 544 aF	212 aF 29 aF

B. Periodic Steady State Analysis of SE BMMWO

The fundamental frequency and the harmonics of an autonomous circuit is obtained using PSS analysis using harmonic balance method. The spectrum obtained after PSS is tabulated in Table 3. The fundamental frequency, f_o of the circuit is obtained as 371 GHz with a few harmonics.

TABLE 3. Periodic Steady State Analysis Spectrum

Frequency	Amplitude in dB
f_o	-2.4
2 f_o	-21
3 f_o	-34
4 f_o	-41

C. Periodic Noise Analysis of SE BMMWO

Periodic noise analysis computes the noise of the circuit including the effects of thermal noise, flicker noise and shot noise. The phase noise of the oscillator which is an important parameter is obtained by pnoise analysis and is tabulated in Table 4. Table 5 shows the noise contribution summary of active devices in the circuit.

TABLE 4. Periodic Noise Analysis

Offset Frequency (M Hz)	Phase Noise (dBc/Hz)
1 MHz	-40.9
10 MHz	-71

TABLE 5. Noise Summary

Device	Parameter	Noise contribution	% of Total
M1	fn	10.2 M	82.04
M2	fn	2.23 M	17.96

TABLE 6. Single ended BMMWO design summary

Performance parameters	Values
Oscillation frequency	371.9 GHz
Output Swing	1.5 V pp
Phase noise	-71 dBc / Hz at 10 MHz offset

D. DC Analysis of Differential BMMWO

The dc operating points of the transistors in the oscillator circuit is tabulated in Table 7. The simulated power consumption of the circuit is 3.72 mW

TABLE 7. DC Operating point of transistors

Transistor	g_m (mA/V)	I_D (mA)	(W/L)
M1,M2	4.951	1.165m	1.76 µ / 22n

TABLE 8. Structure capacitance of transistors

Transistor	C_{gs}, C_{gb}, C_{gd}	C_{ds}, C_{db}
M1, M2	1.35 fF, 23 aF, 550 aF	195 a,F 24 aF

E. Periodic Steady State Analysis of Differential BMMWO

The spectrum obtained after PSS is tabulated in Table 9. The fundamental frequency, f_o of the circuit is obtained as 372.9 GHz with a few harmonics.

TABLE 9. Periodic Steady State Analysis Spectrum

Frequency	Amplitude in dB
f_o	-2.96
2 f_o	-21.21
3 f_o	-35.65
4 f_o	-42.07

F. Periodic Noise Analysis of Differential BMMWO

The phase noise of the oscillator obtained by pnoise analysis and is tabulated in Table 10 and noise summary in table 11.

TABLE 10. Periodic Noise Analysis

Offset Frequency (M Hz)	Phase Noise (dBc/Hz)
1 MHz	-38.48
10 MHz	-70

TABLE 11. Noise Summary

Device	Paremeter	Noise contribution	% of Total
M1	fn	768.5	65.76
M2	fn	319.14	27.31

M3	fn	60.66	5.19

G. Figure of Merit Calculation of BMMWO

To compare the performance of VCOs, with different center frequencies, power consumption and offset phase noise, a figure of merit widely accepted is

$$FOM = L(f_o, \Delta f) + 10 \log\left(\left(\frac{f_o}{\Delta f}\right)^2 \frac{P_{dc}}{[mW]}\right)$$

The performance of an Oscillator is considered better with a more negative value of FOM.

TABLE 12. Differential BMMWO design summary

Performance parameters	Values
Oscillation frequency	372.9 GHz
Output Swing	1.46 V pp @single ended
Phase noise	-70 dBc / Hz at 10 MHz offset
FOM	167

H. Performance Comparison

The designed BMMWO is compared with state-of-the-art oscillator architectures across various performance parameters.

TABLE 13. Performance comparison with state-of-the-art architectures

Ref No	Center frequency GHz	Phase noise dBc / Hz @ 10 MHz @ 10 MHz offset	FOM	Technology
4	70	-107	159	350 nm SiGe
5	90	-110	173	65 nm CMOS
6	90	-114	176	28 nm CMOS
6	128	-105	-	90 nm CMOS
This work	372	-70	167	22 nm Bulk CMOS

I. Tuning extension methods for BMMWO

The designed BMMWO is converted to a voltage-controlled oscillator by incorporating tuning methods. MOS varactors are realized to employ frequency tuning. MOS varactors designed in 22 nm technology with a control voltage varying from 0.3 to 0.8 V gives around 490 MHz /V as shown in Figure 9.

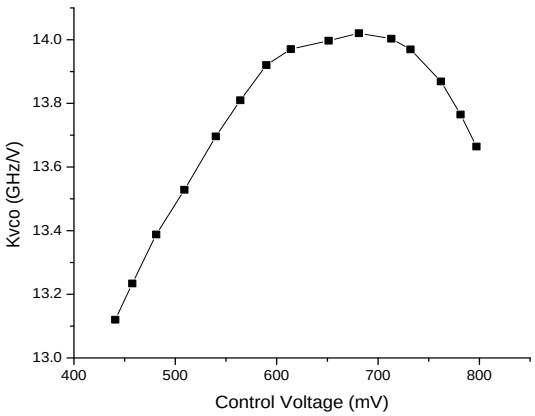

Fig 9 Kvco plot of BMMVCO

V. CONCLUSION AND FUTURE WORK

The proposed BMMW oscillator and VCO designed in 22 nm bulk CMOS technology promises that it can be used at MMW applications and beyond. The achieved phase noise at the center frequency is quite good when compared to state-of-the-art oscillators designed for lower frequency. The entire circuit is designed using the predictive technology models of a 22 nm bulk CMOS. The total power consumed by the circuit is 3.72 mW. The simulation results can be further verified by performing layout and post layout simulations to use the circuit at frequencies beyond MMW.

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