

Efficient VLSI Architecture for Odor Recognition with a Spiking Neural Network

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Abstract: In this paper spiking neural network (SNN) is presented which can discriminate odor data. Spike timing dependent synaptic plasticity (STDP) means a plasticity which is controlled by the presynaptic and postsynaptic spikes time difference. Using this STDP rule the synaptic weights are modified after the mitral and before the cortical cells. In order to determine whether the circuit has correctly identified the odor the SNN has either a high or a low response at the output for any odor given as the input.

Keywords: Olfactory system, Spike timing, Spiking neural network, STDP

I. INTRODUCTION

The foremost function of the nervous system, in any biological organisms is communication and processing of information through neurons and synapses by means of electrical and chemical signals. In order to design more intelligently engineered systems the artificial neurons and synapses need to be designed such that they closely emulate the biological counterparts. The olfactory system is the sensory system used for odor detection. Fig. 1 shows a part of the mammalian olfactory system [1]. The Olfactory receptors respond to the odorants and transmit a signal to the glomerulus in order to pre-process and encode. The signal is then sent to the mitral cells and then to the cortical cell [2].

The spiking neural network presented here uses spike timing dependent learning circuit with dynamic adaptive weights for detection and classification of odor. The exact time at which spikes are generated by the neurons is considered for synaptic weight changes. STDP is controlled by the time difference between the presynaptic spikes and postsynaptic spikes [3]. The previous systems used chemical detection for the olfactory systems which addressed separately sensing, signal processing and neuromorphic simulation models [4] [5]. Also, the STDP has a stable learning process as it uses an adjustable weight dependent mechanism. The correlations detected here are much fine than using a weight-independent method.

Where most SNN circuits are based on the learning through firing rate, it doesn't stand accurate in case of olfactory system as the distinction of odor in a mammalian olfactory system occurs within one sniff, Schaefer and Margrie proposed that the onset of latency can be a better alternative to the firing rate mechanism. In biological neurons the soma voltage is continuously oscillating even in the absence of the input stimuli, so the addition of a subthreshold oscillation in

the network will help in mimicking the biological system better with improved classification performance [6].

For identifying the odor, in the proposed work we are using Cadence Virtuoso software with circuits designed and simulated in 180nm technology node.

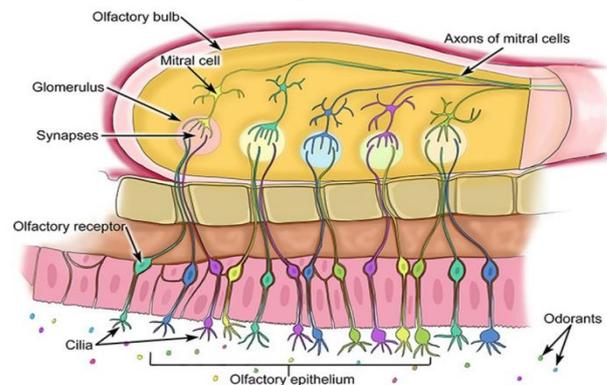


Fig. 1. Mammalian Olfactory System [1]

II. OLFACTORY SYSTEM: CIRCUIT IMPLEMENTATION

The Olfactory receptor cells in a response to the odorant molecules sends an indication to the glomerulus. Multiple glomeruli pre-process, in addition encode the signal to be transferred to the mitral cell and further to cortical cells via synapse. The flow of signal from the Receptor cells to the cortical cell where the identification of odor will happen as shown in the Fig. 2. Each glomerulus sends signal to 4 mitral cells. Each mitral cell is further linked to 1 cortical cell. To each cortical cell eight mitral cells are connected. Two cortical cells form a cortical cell group and they inhibit each other acting as a one vs one classifier [2]. In order to identify three different odors, each cortical cell group is designed to produce different output signal for each odor. Three cortical cell groups will be designed to identify the 3 odors. Every cortical cell in the cortical cell group will have different output pattern for each odor. When 2 of the 3 cell groups have similar output the categorization is done.

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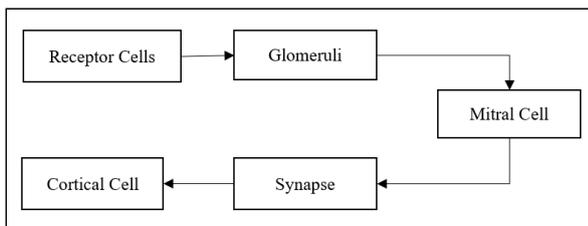


Fig. 2. Block diagram of the Signal Travelling in the Olfactory System

A. Mitral Cell

In the neural organization, the neurons does the integration of the excitatory post-synaptic current (EPSC) produced from the pre synaptic stimulus, for changing its soma voltage. When the voltage of soma is greater than a set threshold value, a spike is produced. A sub-threshold oscillation is added to the chip in order to define the latency for the spike. In the circuit the oscillation is given by a saw tooth waveform voltage given externally. In case if the voltage of the oscillation is low and the current to reset the soma is large the probability of spike production is reduced, else if the voltage of oscillation is high the probability of spike to occur is also high. Therefore, the spike occurs only near the peak of the oscillation. The latency will be defined here as the time difference between the start of the subthreshold oscillation and the output spike.

The threshold voltage of the mitral cell circuit is varied in order to represent varied responses of the sensors. Stronger input stimulus indicates a low threshold voltage. When the transistor supplying the EPSC is not in saturation and the source of EPSC is not on, there is no firing activity.

In this paper the mitral cell only resets the soma voltage at the end of the period of subthreshold oscillation and not every time when the neural depolarization comes to an end. The mitral cell produces an infinite numbers of spikes after initial depolarization which can explain the wide pulse output produced.

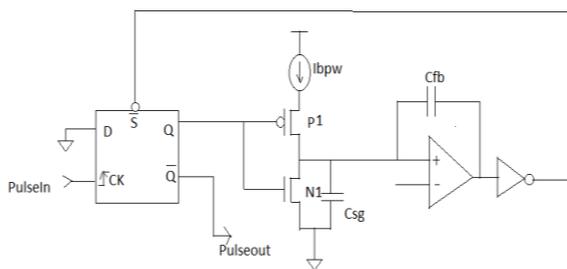


Fig. 3. Mitral cell

B. Synapse circuit

Information exchange happens between the neuron cells with the help of synapse. Several sites called synapses transfer the pre synaptic neural signal to the post synaptic neuron. It acts as an area of contact between the presynaptic neurons and postsynaptic neuron. A link is formed in between presynaptic neuron and postsynaptic neuron by synapse and it sends the signals through electrical and chemical interactions. The basic unit for computation and information exchange in both biological and neuromorphic system is the synapse, so the synapse circuit has to be modelled with at most care. There are two types of synapse - excitatory and inhibitory. If probability of occurrence of

action potential in a post synaptic neuron is increased by the action potential in the presynaptic neuron then it is called as excitatory synapse. Whereas inhibitory synapse is just the opposite of this [7].

The circuit shown in Fig. 4 is a pulse shaping circuit, it takes input from presynaptic neuron and produces two voltages Vpot (potentiation voltage) and Vdep (depression voltage). When a pre synaptic spike occurs both Vdep and Vpot increases sharply and then there is a logarithmic decay [8]. This will increase the weight of the synapse, representing potentiation. The reverse will decrease the weight of the synapse as it will represent depression. In the Fig. 5 there are six MOSFETS, in which M1 and M6 operate in subthreshold region. The current flowing through M1 is Ipot which is proportional to Vpot and similarly the current flowing through M6 (Idep) is proportional to Vdep. The transistors M2 and M5 are in linear region acting as switches, switching ON for the duration in which the post and pre synaptic neurons spike. The transistors M3 and M4 restrict the current through the capacitor Cw. The voltage across the capacitor gives the synaptic weight.

The synapse circuit shown in Fig. 6 has four transistors M1, M2, M3 and M4. M2 takes presynaptic spike input, M1 acts as a weight transistor, M3 and M4 are current mirrors. The output of the circuit is the mean current which increases with the increase in the synaptic weight and pre synaptic spike.

Whenever there is a presynaptic spike the transistor M2 switches ON and it acts as a switch. In the mean time between the spikes the transistor M2 is in OFF state. M2 transistor will be operating in subthreshold regime. When a spike occurs the capacitor will discharge through the M1 and M2 transistor. In the intermediate time between spikes the capacitor will be charged through transistor M3 which is in diode connected configuration (always in saturation region). When the capacitor discharges the current through the transistor M4 it will increase as the gate of M4 transistor is connected to the capacitor. Thus the voltage across the capacitor controls the current value. This circuit implements the function of the synapse, conversion of the incoming voltage spike to a current spike with current strength proportional to the synaptic weight.

C. Cortical Cell Group

There are two cortical cells in every cortical group and an inhibitor in it. Each cortical cell consists of a Timer, comparator, Vrate, Adaptive bias, Leakage current generator and input from synaptic cell. The period of each spike in high state and refractory duration of the capacitor which integrates current is determined by the timer. The voltage integrated from output spike is Vrate.

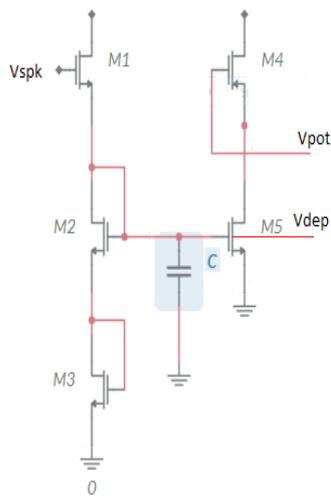


Fig. 4. Pulse changing circuit

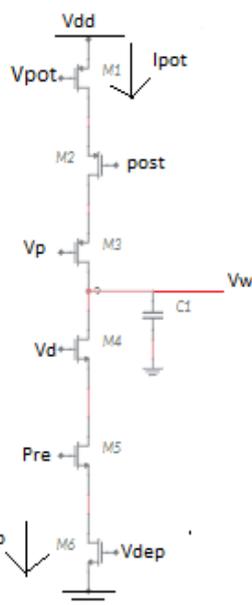


Fig. 5. Weight changing circuit

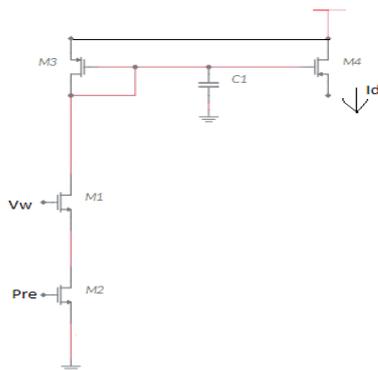


Fig. 6. Synapse Circuit

The timing of each spike is crucial. In an oscillation period the number of spikes formed by each cell is counted. Even though the spiking frequency is different two cells of a cell

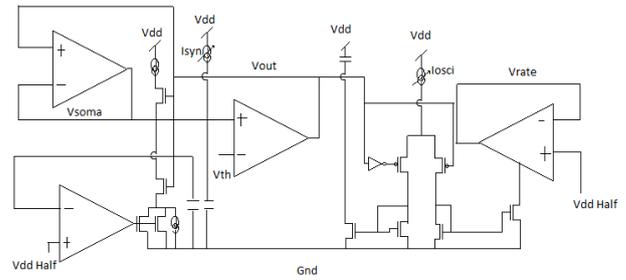


Fig. 7. Cortical Cell

group finding the same number of spiking in the two cells in a group is easy because it is counting the number of spikes formed in an oscillation period. The Vrate is an integer, to provide more accuracy Vrate can be taken as floating point number. The Inhibition block present in between the two cortical cell in the cortical group is crucial because Vrate value from two cortical cell is compared. The one with higher Vrate compared to other cortical cell is inhibited by inhibition block by transmitting the negative current to it to lower the voltage. To get a distinct output each cortical cell try to prevent other. Due to this the output appears fast and distinct. As we mentioned before the cortical cell with higher Vrate is inhibited by passing the negative current, due to which the firing rate is smaller. Inhibition block is a positive feedback. The weak inhibition fails in creating the distinct output but stop the circuit from being inaccessible. In subthreshold oscillations the peaks are clustered around the peak, so as to get a clear difference between the frequencies of spiking of cortical cells strong inhibition is used [3]

Inputs for a comparator in a cortical cell is threshold voltage and Vsoma. As the difference between these two voltages are large the comparator provides output quickly.

The slew rate is enhanced using two methods one is by EC generator, the other is by using adaptive current bias techniques used for comparator. EC generator acts like a leakage current generator when the soma voltage is lower than the threshold voltage. When the Vsoma is higher than the threshold voltage then the neurons depolarizes and the steep increase of output voltage is observed as the current generator is excitatory leading to a positive feedback. In adaptive bias when the comparator is depolarizing the bias current is enlarged due to which output voltage becomes steep These two methods help in achieving the fixed spike width along with reduced power consumption [3].

The large capacitor in the soma is an issue. Before the next operation the capacitor value should be zero that is complete discharge has to be taken place, as the size is huge the time taken to discharge the capacitor is not sufficient so there is a presence of some charge left before the next operation which affects the next operation. There is a solution by discharging the charge using large switch so the voltage of the soma can be reset quickly but this increases the switching power and also increases the leakage power so keeping the efficient power in mind this method cannot be used.

Another method is after the action potential is produced the EPSC integration is prevented for a short period of time. So the discharge of same happens and made sure the capacitance is zero before the next cycle [3].

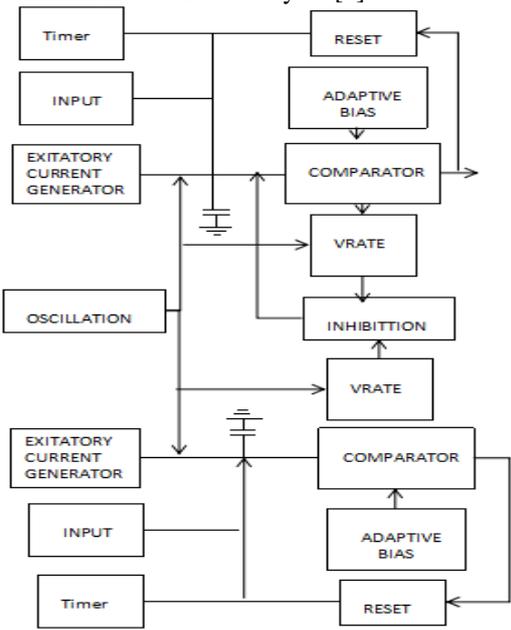


Fig. 8. Block Diagram for Cortical Cell Group

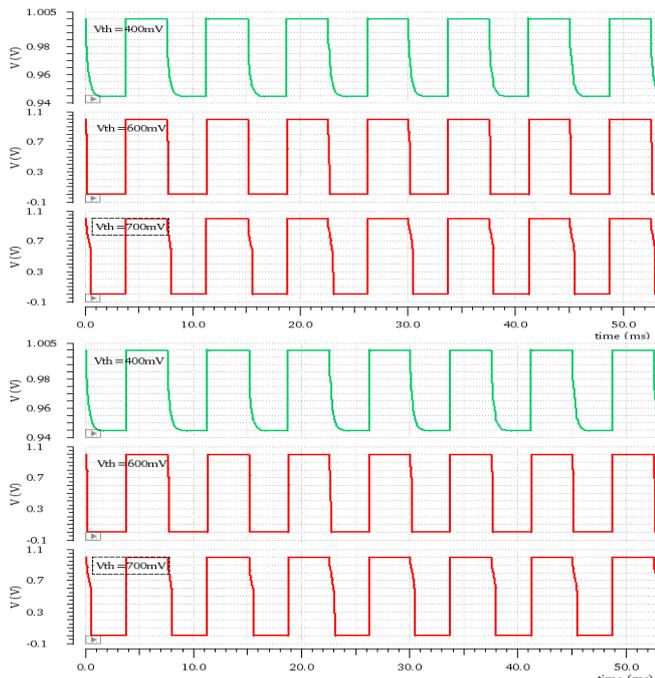


Fig. 9. Simulation waveform of Cortical cells for different threshold values

III. SIMULATION AND RESULTS

The mitral cell, synapse circuit and cortical cell were individually designed and simulated in using 180nm technology node in Cadence Virtuoso software.

For the mitral cell circuit, the sensory input in terms of voltage (Vpulse) is given and it gives an output voltage pulse. The output voltage from mitral cell is given as input to the synapse circuit which acts as a communication link between the mitral and cortical cell, the synapse circuit produces a

output current according to the synaptic weight as shown in Fig. 9.

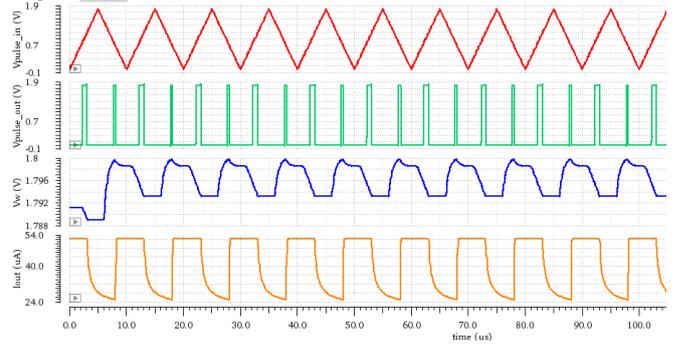


Fig. 10. Simulation waveform of Mitral cell, weight change circuit and Synapse circuit

The cortical cell takes the input current from synapse circuit and it gives a spiking output voltage as shown in Fig. 10 according to the threshold voltage given (which represents the odor data threshold).

FUTURE SCOPE

In future this work can be extended by connecting 48 mitral cells with 48 synapse circuit and each mitral cell can be connected to one cortical cell, 8 mitral cells are connected to one cortical. Each cortical cell output can be compared with the others to distinguish the odors data. In the proposed work, the synapse circuit is designed for symmetric STDP, in future it can be done for asymmetric STDP.

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