Design of LowPower Hybrid Gaincell-eDRAM for Embedded Processors

G VamsiKrishna Reddy, Sri. G. Ramesh

Abstract*: This brief mainly focuses on increasing the data retaining capability at the Storage Node (SN) and reducing the power consumed by the Hybrid Gaincell eDRAM/SRAM (HGC-eDRAM/SRAM). A Hybrid Gaincell eDRAM/SRAM cell contain SRAM cell and DRAM cell. Both the SRAM and DRAM cell share the SN. The DRAM cell here is implemented as 3T Gaincell. The data retaining capability is improved by isolating the shared SN of the SRAM cell and adding a capacitance at the SN if the 3TGaincell. The above-mentioned modifications are implemented in Cadence Virtuoso 6.1.6 using 90nm technology.

***Keywords*: Gaincell, SRAM, embedded DRAM (eDRAM), hybrid gaincell.**

I. INTRODUCTION

High performance Embedded Processors require adequate amount of on-chip memory. The type of on-chip memory decides the performance of the processor. In most of the cases the on-chip memory is SRAM. Because SRAM cells are very fast when compared to other types of memories.

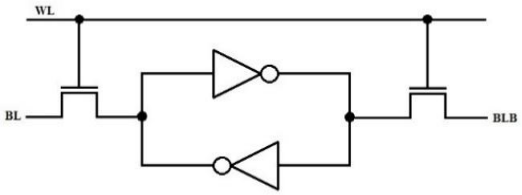

Fig (1): Conventional 6T SRAM cell.

The 6T SRAM cell, as in fig (1), is ideal when the processor is active or operational. The SRAM cells do not require any refresh cycles, because the data is retained till the SRAM is powered. But these SRAM cells consume dominant power, when the processor is idle. When the device is operational, the power consumed by the SRAM cell accounts to 50 percent of the total power consumed. But, when the device is idle, or in standby mode these memories consume dominant portion of the SOC power.

To overcome this disadvantage of increased standby power, Hybrid Gaincell-eDRAM was proposed as an alternative to the SRAM cell. A Hybrid Gaincell-eDRAM is designed by combining the Storage Node (SN) of SRAM keeper with the SN of DRAM. The DRAM is implemented using 3T gaincell, as shown in fig (2). Gaincell usage is more advantageous over conventional 1T DRAM, because the Gaincell provides 2-port operation.

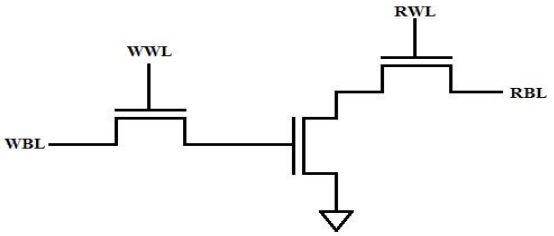

Fig (2): 3T-Gaincell.

Gaincell usage is advantageous over conventional 1T DRAM, because the Gaincell provides 2-port operation. These Hybrid Gaincell-eDRAM cells consume less power compared to the SRAM cells when device is idle. So, this provides an advantage over conventional SRAM cells. The retention time of these bitcells is limited. So, we need frequent refresh cycles to retain the data. This has direct impact on the power consumption due to requirement of frequent refresh cycles. To overcome this limitation, an improved Hybrid Gaincell-eDRAM is proposed. The power consumption of the Hybrid Gaincell-eDRAM can be reduced by isolating the Storage Nodes (SN) of the SRAM cell and Gaincell. This also prevents the data degradation at SN. So that we can achieve a higher retention time. This reduces the requirement of frequent refresh cycles.

II. EXISTING DESIGN

The HGC-eDRAM is implemented using PINV1, NINV1, PINV2, NINV2 and PIOSL, as SRAM keeper latch. MW, MR1, and MR2 together form a 3T gain cell. The PINV1 and NINV1 in SRAM, of bit-cell are isolated using PISOL. The whole SRAM cell and PIOSL are power gated using Power Gating block. All the bit-cells in a row share the same Power Gating block.

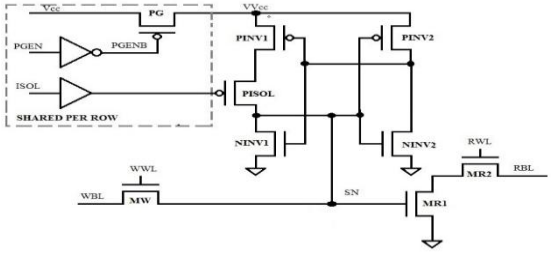

Fig (3): Hybrid Gaincell-eDRAM bitcell.

Fig (3) shows Hybrid Gaincell-eDRAM. The Power Gating block is enabled when the processor is active, and it is switched off in the standby mode. During the refresh operation, the power gating block is enabled and PIOSL is switched on by making ISOL=0.

Revised Manuscript Received on October 05, 2019

G VamsiKrishna Reddy, Pursuing M. Tech in VLSI and ES at G. Pulla Reddy College of Engineering, Kurnool, Andhra Pradesh, India – 518007.

G. Ramesh, Assistant Professor, Department of Electronics and Communication Engineering, G. Pulla Reddy College of Engineering, Kurnool, Andhra Pradesh, India – 518007.

III. PROPOSED DESIGN

From the existing design, the PISOL which isolates PINV1 and NINV1 is removed. PISOL is now used to isolate the SNs of the SRAM and Gaincell. The same can be observed in Fig (4). This will help in isolating the SRAM cell and gaincell. This will help in reducing the dynamic power of the bit-cell. In addition to this, MC is added at the SN of the Gaincell to enhance the data retaining capability of the Gaincell, when the Power Gating block is switched off.

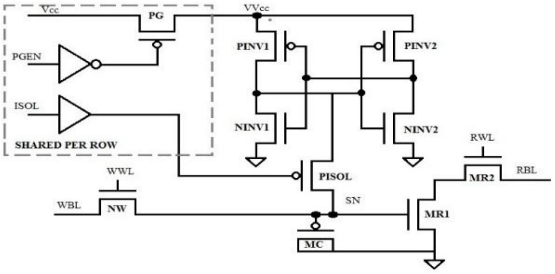

Fig (4): Schematic of Improved HC-eDRAM.

A. *9T Hybrid Gaincell eDRAM*

The SRAM keeper of the bit-cell implemented using INV1 and INV2. 3T Gaincell is implemented using MW, MR1 and MR2. The PIOSL will isolate the SNs of the Gaincell and the SRAM keeper. To retain data at the SN, a MC is connected at the SN of the Gaincell. As PMOS can pass high voltages., PISOL used here is a PMOS.

B. *Operation*

The operation modes can be categorized as Active mode, Standby mode (Power saving mode). Active mode refers to mode operation when processor actively running. Power saving mode refers to mode of operation when the processor is idle.

In active mode the above designed bitcell can be operated as normal SRAM cell. For write operation, initially the Power Gating block is enabled and IOSL is made 0. This will power on the SRAM keeper (PINV1, NINV1, PINV2 and NINV2) in the bitcell. The data to the SN is written through write word line (WWL) by enabling the write bit line (WBL). The data once written at the SN is retained till it is rewritten by another level.

In power saving mode or standby mode, the SRAM keeper is powered down by disabling the Power Gating block and the storage nodes are isolated. As soon as the SRAM keeper is powered down, the data at the SN tend to degrade due to leakages. To retain the data at the storage node, refresh cycles are implemented.

C. *Refresh cycle*

The refresh cycle will regenerate the degrading data at the SN. The refresh operation is performed by switching on the SRAM keeper latch. This is done by making PGEN=1 and IOSL= 0. The SRAM should be powered on prior to connecting the storage nodes to avoid data degradation at SN because of SRAM keeper cell.

IV. SIMULATION AND RESULTS

The schematic is designed using 90nm Process Design Kit (PDK) and simulations for the two modes of operation namely Active and Power saving are done.

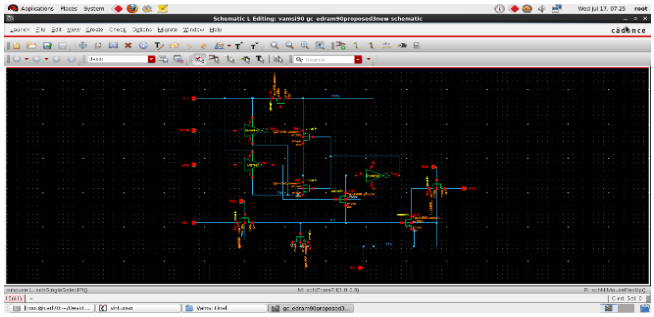

Fig (5): Implementation of proposed design.

A. *Active Mode Simulation*

Schematic designed as in fig (5), is simulated in the active mode of operation, VVcc is supplied to the SRAM keeper by enabling the power gating block, and the PIOSL is switched on. The data '1' is written to SN through WBL by switching the MW to 'ON' state by making WWL=1. In this mode as the power gating block powers the SRAM keeper cell, the data in the bitcell is retained. The same can be observed in the Fig (6).

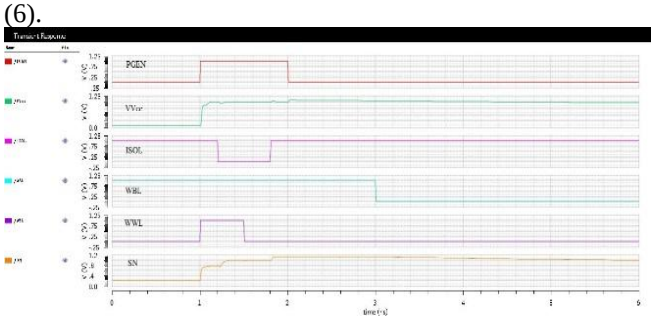

Fig (6): Simulation of write operation in active mode.

B. *Standby Mode Simulation*

In standby mode the VVcc that is supplied prior to writing the data at the SN is removed by Power gating. And the storage nodes of SRAM keeper and Gaincell are isolated by making PGEN=0 and ISOL=1. Now the data at the SN starts to degrade. The same can be observed from fig (7). After an interval of 100ns the voltage retained at the SN was 171.982 mV. This is much higher than the existing design.

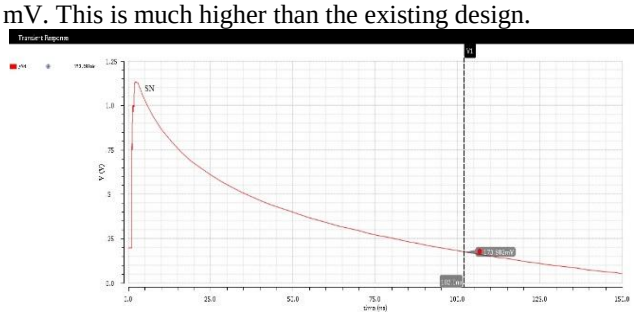

Fig (7): Data degradation at SN in standby mode.

C. *Refresh cycle Simulation*

To refresh the data at the SN, refresh cycles are necessary during standby mode of operation.Before the data at the SN is completely degraded, refresh cycles are generated by making PGEN=1 and ISOL=0. This will power the SRAM keeper and connect the storage nodes of SRAM keeper and gaincell. This is done by making PGEN=1 and ISOL=0. But, PGEN is first

turned on prior to PISOL to avoid degradation of data.

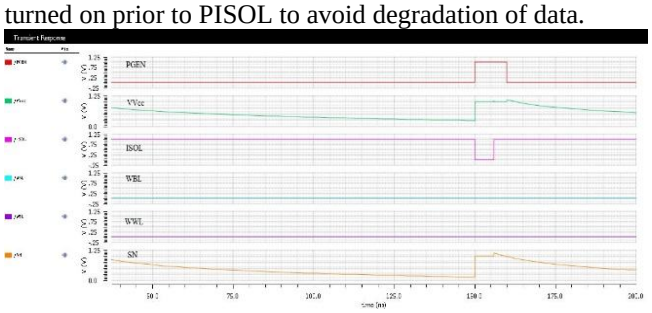

Fig (8): Refresh operation simulation.

Power consumption

The improved design consumes 47.80uW of power on average. This is less when compared to the existing design. Fig (9) shows power consumption plot of proposed design.

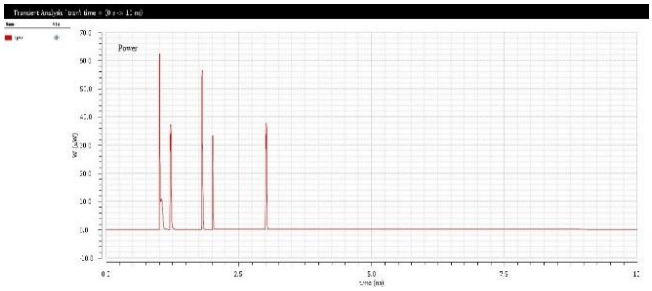

Fig (9): Power consumption plot of improved HGC-eDRAM.

Comparison of Existing and Proposed Designs

Parameter	Existing Design	Proposed Design
Supply Voltage	1V	1V
Voltage retained after 100 ns	65.012mV	171.982mV
Delay	806ps	790ps
Power	51.78uW	47.80uW

V. CONCLUSION

A 9T Hybrid Gain-cell e-DRAM was proposed to combine the advantages of both the SRAM and 3T Gaincell. The same is implemented in Cadence Virtuoso 6.16 tool using 90nm technology. Compared to existing Hybrid Gaincell-eDRAM, reduction the dynamic power consumption and improvement in the data retaining capability of the bit-cell was observed. So, the improved design will also require less frequent refresh cycles, which in turn reduces the standby power consumption of the GC-eDRAM.

REFERENCES

1. R. Giterman *et al.*, "Hybrid GC-eDRAM/SRAM Bitcell for Robust Low-Power Operation" IEEE Trans. Circuits Syst. I, vol. 64, no. 2, pp 1362-1365, 2017.
2. P. Meinerzhagen et al., Gain-Cell Embedded DRAMs for Low-Power VLSI Systems-On-Chip. Cham, Switzerland: Springer, 2017.
3. R. Giterman et al., "An 800Mhz mixed-VT 4T gain-cell embedded DRAM in 28nm CMOS bulk process for approximate computing applications," in Proc. Eur. Solid State Circuits Conf. (ESSCIRC), 2017, pp. 308–311.
4. P. Meinerzhagen, A. Teman, R. Giterman, A. Burg, and A. Fish, "Exploration of sub-VT and near-VT 2T gain-cell memories for ultralow power applications under technology scaling," J. Low Power Electron. Appl., vol. 3, no. 2, pp. 54–72, 2013.
5. P. Meinerzhagen, A. Teman, R. Giterman, A. Burg, and A. Fish, "Impact of body biasing on the retention time of gain-cell memories," IET J. Eng., vol. 1, no. 1, pp. 1–3, 2013.
6. A. Teman, P. Meinerzhagen, R. Giterman, A. Fish, and A. Burg, "Replica technique for adaptive refresh timing of gain-cell-embedded DRAM," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 4, pp. 259–263, Apr. 2014.
7. R. Giterman, A. Fish, A. Burg, and A. Teman, "A 4-transistor nMOSonly logic-compatible gain-cell embedded DRAM with over 1.6-ms retention time at 700 mV in 28-nm FD-SOI," IEEE Trans. Circuits Syst. I, Reg. Papers, to be published.
8. R. Giterman et al., "Single-supply 3T gain-cell for low-voltage lowpower applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 1, pp. 358–362, Jan. 2016.
9. N. Verma and A. P. Chandrakasan, "A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy," IEEE J. Solid-State Circuits, vol. 43, no. 1, pp. 141–149, Jan. 2008.
10. A. Teman, L. Pergament, O. Cohen, and A. Fish, "A 250 mv 8 kb 40 nm ultra-low power 9T supply feedback SRAM (SF-SRAM)," IEEE J. Solid-State Circuits, vol. 46, no. 11, pp. 2713–2726, Nov. 2011.
11. A. T. Do et al., "0.2 v 8t SRAM with PVT-aware bitline sensing and column-based data randomization," IEEE J. Solid-State Circuits, vol. 51, no. 6, pp. 1487–1498, Jun. 2016.
12. S. Ahmad, M. K. Gupta, N. Alam, and M. Hasan, "Single-ended Schmitt-trigger-based robust low-power SRAM cell," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 8, pp. 2634–2642, Aug. 2016.
13. K. C. Chun, P. Jain, J. H. Lee, and C. H. Kim, "A sub-0.9V logiccompatible embedded dram with boosted 3T gain cell, regulated bit-line write scheme and PVT-tracking read reference bias," in Proc. Symp. VLSI Circuits, Kyoto, Japan, 2009, pp. 134–135.

AUTHORS PROFILE

G VamsiKrishna Reddy, pursuing M. Tech in VLSI and Embedded Systems at G. Pulla Reddy College of Engineering, Kurnool. He has obtained B. Tech in Electronics and Communication Engineering from KSRM College of Engineering, Kadapa in the year 2016.

G. Ramesh, currently working as Assistant Professor with Department of Electronics and Communication Engineering, with 10 years of experience in teaching at G. Pulla Reddy College of Engineering, Kurnool, India. He has obtained M. Tech in Embedded Systems from JNTUH, Hyderabad. Currently pursuing Ph. D from SKU.