Design and Performance Improvement of CNTFET Based Content Addressable Memory (CAM) Cells

Raju Hajare, Mallikarjunagowda C. P, Deekshitha, Madhuri. J, Ananya

Abstract: The scaling down of transistors is of paramount importance to make ICs and devices more portable and efficient. As it is the most basic component of every electronic device, there is need of finding better and innovative methods of transistor characterization. CNTFET has shown the promise and is best suited for today's faster digital processing units and Memory devices. Here Carbon Nano Tube (CNT) is characterized for its electrical property and then designed a XOR based CAM cell using CNTFET. Both delay and power analysis for the designed CAM is done.

Keywords: Carbon Nano Tube FET (CNTFET), Content Addressable Memory (CAM) Cell, SRAM, MOSFET.

I. INTRODUCTION

The electronic devices and systems with their compactness in size, light weight, low power consumption, high performance and rich in functionalities are in great demand. For the last 4 decades, both academia and industries have pushed the downscaling of Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) to achieve these demands. But the downscaling of MOSFET can be achieved only up 45nm node size as it faces severe Short Channel Effects (SCEs) below the 45nm size. So it is very important to look for an alternative device structures for replacing the present MOSFETs [1]. The newer silicon device structures such as multiple gate MOSFETs and FinFETs and others solve the SCEs to some extent. There is one more novel device made of Carbon Nano Tube called CNTFET meets most of the today's IC industries. Among all, top gated CNTFETs have attracted more attention of device scientists as it is giving better performance with respect to switching element in ICs. The improvement in performance is due its scalable dimensions and adoption of suitable geometry [8]. The ballistic carrier transport nature of CNTs with high carrier mobility achievement in semiconductor devices makes CNTFET a promising candidate for the future fast processing digital systems and faster memory chips. At the same time this device has advantages of compatibility with existing CMOS fabrication process [12]. But CNTFET is still in research phase due to its reliability issues.

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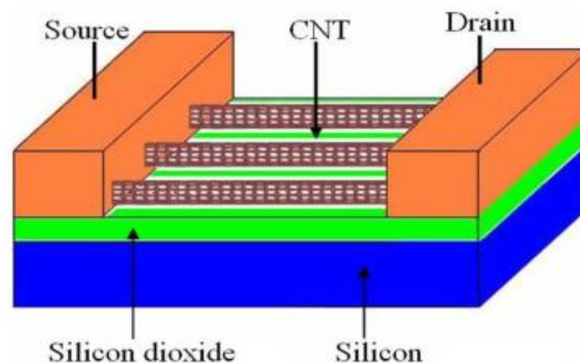

Figure 1: Structure of CNTFET [2].

II. PROPOSED CNTFET-BASED SRAM DESIGN:

Figure 2 shows a CNTFET-based 6T SRAM cell. Here the Static Random Access Memory (SRAM) cell comprising of simple CNTFET latch is shown. It has two cross coupled inverters along with two access transistors. Once Word Line(WL) is asserted the data write operation can be achieved by applying the proper values to bit lines called BL and BL'. After memory write operation, SRAM cell comes to standby mode while the WL is set to 0, and the memory cell stores the data until next working period. The simulation time taken is short for CNTFET based SRAM, with an average CPU time of circa 1 second. The power consumption of the device is obtained by calculating the output current of the SRAM cell. With small supply voltages at terminals of the transistors, the SRAM can be estimated to be power efficient.

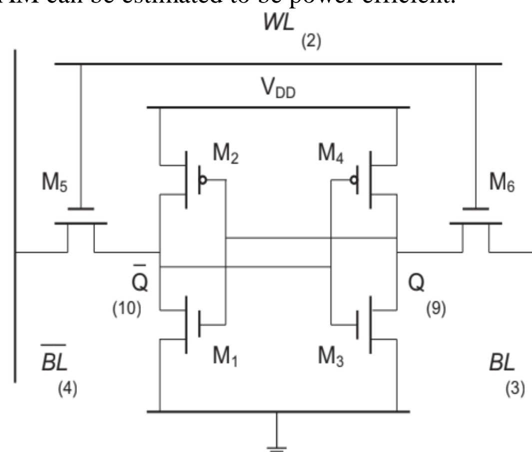

Figure 2: SRAM cell [2].

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Write operation:The write cycle begins by applying the value to be written to the bit lines. If '0' is to be written, then we would apply '0' to the bit lines, i.e. setting BL to 1 and BL' to 0

A. Write Operation

The write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1and BL' to 0. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A '1' is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. This works because the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself so they can easily override the previous state of the cross-coupled inverters. In practice, access NMOS transistors M 5 and M 6 have to be stronger than either bottom NMOS (M 1 , M 3) or top PMOS (M 2 , M 4) transistors. This is easily obtained as PMOS transistors are much weaker than NMOS when same sized. Consequently, when one transistor pair (e.g. M 5 and M 6) is only slightly overridden by the write process, the opposite transistors pair (M 7 and M 8) gate voltage is also changed. This means that the transistors can be easier overridden, and so on.

B. Read Operation:

Reading only requires asserting the word line WL and reading the cell state by a single access transistor and bit line. However, bit lines are relatively long and have large parasitic capacitance. To speed up reading, a more complex process is used in practice. The read cycle is started by pre-charging both bit lines BL and BL', to high (logic 1) voltage. Then asserting the word line WL enables both the access transistors M 3 and M 4, which causes one bit line (BL) voltage to slightly drop. Then the BL and BL' lines will have a small voltage difference between them. A sense amplifier will sense which line has the higher voltage and thus determine whether there was 1 or 0 stored.The higher the sensitivity of the sense amplifier, the faster the read operation. As the NMOS is more powerful, the pull-down is easier. Therefore, bit lines are traditionally pre-charged to high voltage.

III. RESULTS AND DISCUSSIONS

When SRAM cell is evaluated for current characteristics, the following simulated waveforms are obtained.

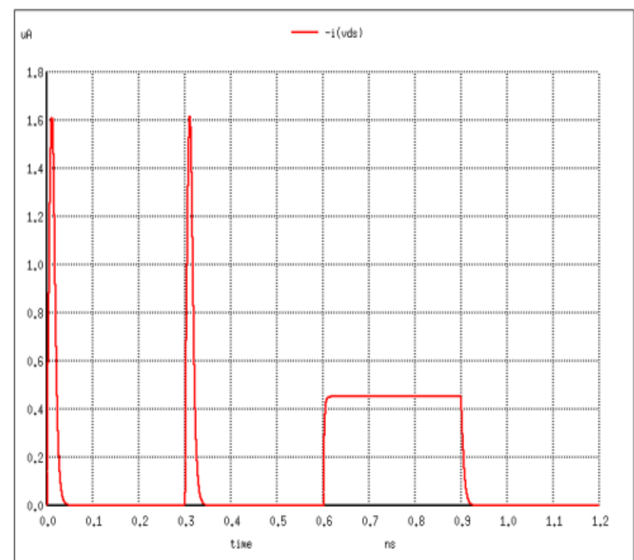


Figure 3: The operation current characteristics of the SRAM cell.

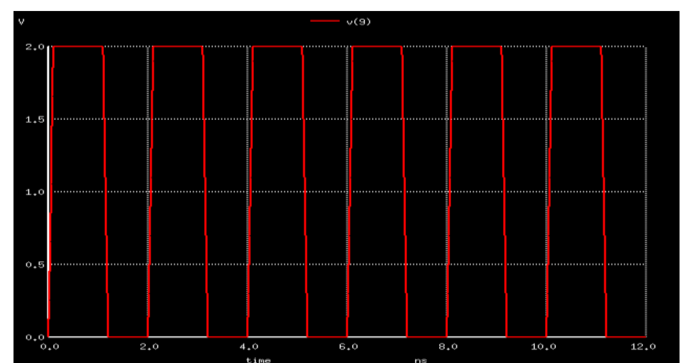
Figure 3 illustrates that the drain current of the transistors within the memory cell is less than 1.6µA. Power consumption of the SRAM cell can be estimated using Eq. 1

Psc = ½ Vdd Ipeak Tt fn – 1

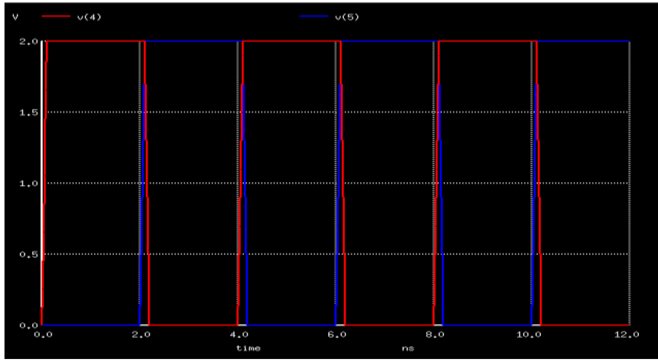
Where 'Vdd' is the drain voltage taken as 0.5V for the SRAM simulation 'f' is the frequency of operation (3.33GHz), 'Tt' represents the transition time of the input(0.1ns), 'Ipeak' is the maximum saturation current of the CNT transistor in SRAM cell(1.6µA), and 'n' is the number of transistors(6 transistors) used in the SRAM Cell.

With parameters that are derived from the simulation, the power consumption Psc can be estimated to be circa 0.8µW for the SRAM cell as per equation-1, which dissipates small energy around 2.4x10-16J per switch for the CNT based SRAM cell.

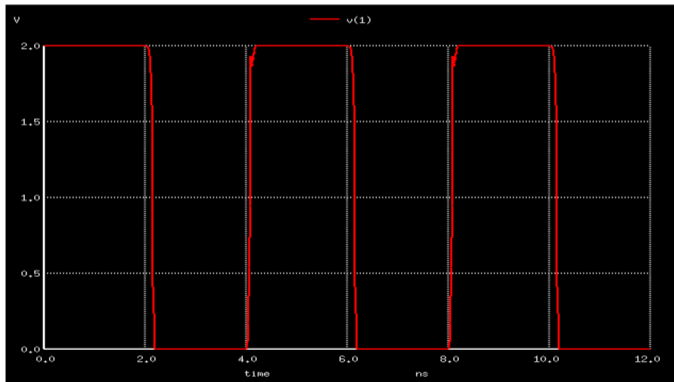
3.1 Sram Waveforms



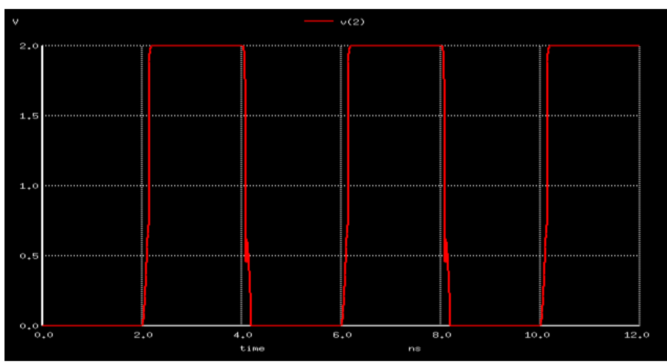
[a]



[b]



[c]



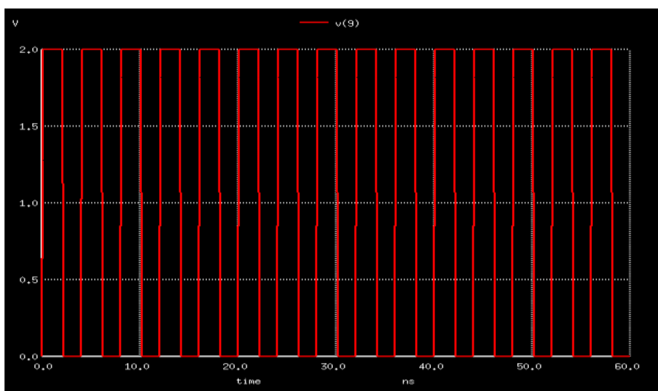
[d]

Figure 3.1: Read and write operations in SRAM.

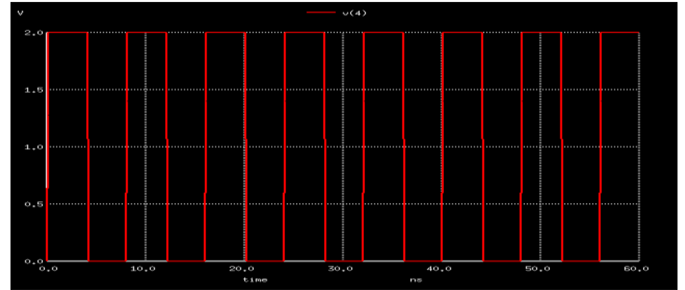
[a] Word Length (WL) [b] BL and BL' [c] Output at point Q

[d] Output at point Q'.

3.2. Cam Waveforms :



[a]



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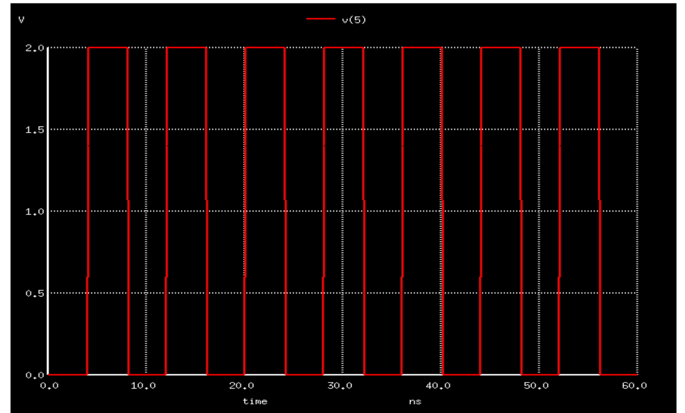
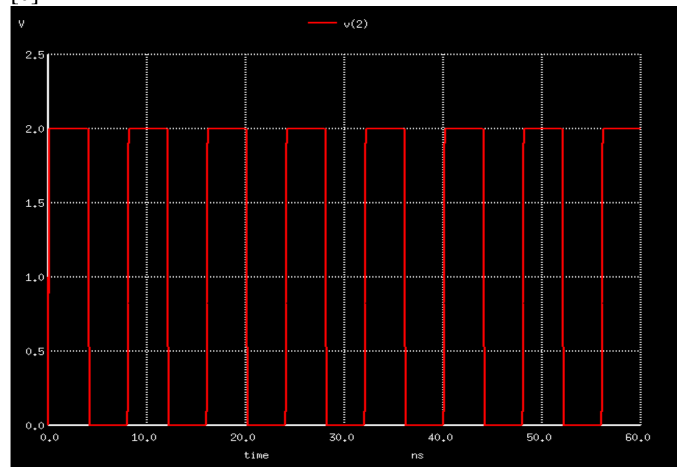


[c]



[d]

Figure 3.2: Read and write operations in CAM.

[a] Word Length (WL) [b] BL and BL' [c] Output at point Q
[d] Output at point Q'.

3.3. Cascaded Inverter Based Cam Waveforms:

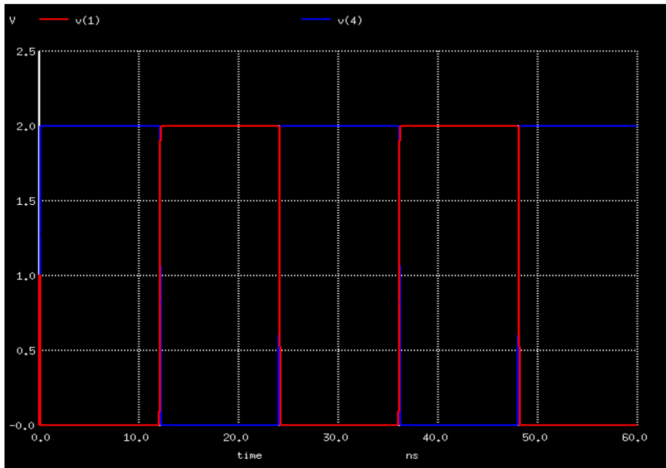


Figure 3.3: [a] Delay in 2 inverter based CAM cell

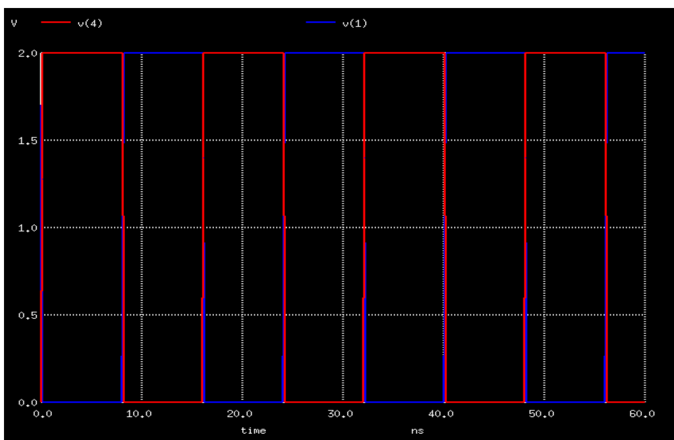


Figure 3.3: [b] Delay in 6 inverter based CAM cell.

Table 1: Delay in 2 inverter and 6 inverter based CAM cell

Operation	2 Inverter based CAM	6 Inverter based CAM
Read	321ps	62.5ps
Write	156ps	78ps

From Figure 3.3 and Table 1, it is observed that the delay is reduced by a significant amount when 6 inverters are used to latch the data instead of 2 inverters. The delay during the read operation for 2 inverter and 6 inverter based CAM cell is 312 picoseconds and 62.5 picoseconds respectively. During the write operation the delay is 156 picoseconds for 2 inverter based CAM and 78 picoseconds for 6 inverter based CAM. The pictorial graph giving comparison for inverter 2 and 6 inverter based CAM Cell is as shown in fig-8.

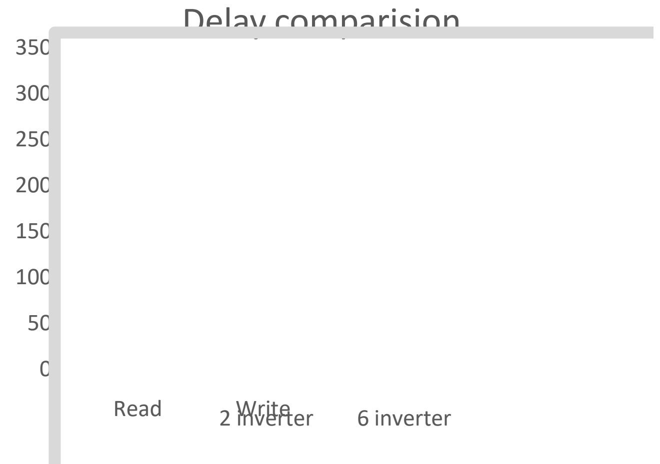


Figure 3.4: Pictorial comparison of Delay in 2 inverter and 6 inverter based CAM cell

Due to the inverse relation between current and time, the delay time can be reduced by increasing the current flowing through the circuit. 6 inverters drive more current than 2 inverters and thus its delay time is lesser.

IV. APPLICATIONS

CAM cells are used in Computer network devices. The MAC address table is implemented with a binary CAM, so as to find destination port very quickly when MAC table is looked into in network switching when it receives a data frame from one of its ports. It reduces the switch latency.

There are CAMs also known as ternary CAM used in network routers, which make the look up process very efficient.

The other applications of CAM also include

Artificial Neural Networks

Database engines

Data compression hardware

Intrusion prevention system

IVa . Advantages

The advantages of CAM system are:

Data storage and retrieval capabilities which simplify common data manipulations like searching, matching, sorting, cross referencing and updating.

Programming simplifications based on the placement of data in a memory.

Interconnections between components are simplified, reducing propagation delays.

Loss of any cell or malfunction doesn't affect the program, since it has periodic structure.

IVb . Disadvantages

Floating point arithmetic operations are not efficient, since it is necessary to sequentially normalize cell contents.

Cost of refrigeration for crytron devices may be considered as a disadvantage.

New software developments are required for use of CAM cell.

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V. CONCLUSION

Here Content Addressable Memory designs using CNTFET is carried out to improve upon the performance in terms of read and write operation. Circuit Simulation results confirm that the CAM cells perform function accurately during read, write and search operations. It is also observed that the proposed CAM cells achieve significant improvement in terms of search speed due to reduced match line capacitance and number of transistors with respect to the CNTFET based conventional cells. Hence, the observed results reveal that the proposed CAM cells are capable of enhancing the performance of memory systems

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