Performance Analysis Of Double-Gate Carbon-Nanotube FET And MOSFET For High Speed Integrated Circuits Design

Aakanksha Lakhanpal, Karmjit Singh Sandha

Abstract: This paper explains the detailed structure as well as performance of DG-CNTFET (Double Gate Carbon Nanotube Field Effect Transistor) and its performance is compared with the DG-MOSFET (Double Gate Metal Oxide Semiconductor Field Effect Transistor). Various parameters like I-V characteristics, ON current, OFF current and ON to OFF current ratio have been evaluated using nano-TCAD ViDES. Also, the transport description of DG-MOSFET and DG-CNTFET has been described in detail. It has been observed that DG-CNTFET has lower OFF current and higher ON current in comparison to the DG-MOSFET. The higher ON current of DG-CNTFET depicts that it requires less time to turn on the device in comparison with DG-MOSFET. Also, OFF current of the DG-CNTFET is lesser as compared to MOSFET. The DG-CNTFET's higher ON to OFF current ratio outperforms the DG-MOSFET in term of switching speed of the device. It is proposed that CNTFET can be used as an alternative of MOSFETs for high speed Integrated Circuit (IC) design.

Keywords-DG-MOSFET, MWCNT, SWCNT, DG-CNTFET (Double Gate Carbon Nanotube Field Effect Transistor).

I. INTRODUCTION

One of the main purposes of the semiconductor technology is that it scales down the transistor size as well as the transistor integration on an individual chip is increased. According to the Moore's law prediction, with the advancement of semiconductor technologies are leveling down to the nanometer the size of the devices is also been shrinking. The semiconductor device technology is significantly improving due to the result of the persistent success in scaling these devices. In the past two decades, the MOS based transistor size is reduced in a characteristic size that varies from various microns to the less than 45 nm. When the semiconductor device's channel length is reduced than the drain induced barrier lowering, threshold voltage roll-off and short channel effects increased significantly. The MOSFET's scaling capability is limited by the short channel effect. With the advancement in technology, carbon nanotube (CNTs) are discovered as a structure which plays an important part in the future electronic systems. Carbon nanotubes have been evolved as one of the outstanding material in eradicating the limitations of various parameters like increased leakage current by modifying the channel material by carbon nanotube in MOSFET devices at nanoscale. CNTs are described as the planar graphene sheets which are wrapped in the tube like structures. The CNT's electrical characteristics changes with the graphene's wrapping angle and CNT's diameter [1]. The wrapping angle as well as the diameter can be explained by the fundamental indices of tube (n, m). Depending upon the chirality, the CNT is classified as semiconductor or metallic. Chirality is the property of CNT which decides how tube-like structures are formed by rolling up the graphene sheets. There are two categories of the carbon nanotube such as Multiwall Carbon Nanotubes (MWCNT) and Single Walled Carbon Nanotubes (SWCNT) [2].The SWCNT involves wrapping of graphene sheet's one-layer into cylinder and can be used as transistors. Every SWCNT bundle has number of SWCNT having same diameter and same number of conducting channels. The diameter is 0.33 to 5.0 nm and lengths are 2 to 10nm [3].

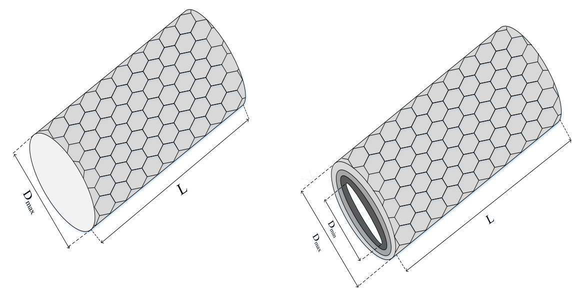

Fig.1. Structure Of SWCNT And MWCNT Where *L*= Length Of Nanotube, D_{max} = Outer Diameter And D_{min} = Inner Diameter Of Nanotube.

Multiwall carbon nanotube consists of multiple layers of graphene to form concentric cylinders. The MWCNT bundle can be depicted as number of concentric shells with different diameter and therefore different number of conducting channels [4]. Where as in case of SWCNT bundle, every nanotube has same diameter as well as similar conducting channels numbers. The diameter of MWCNT varies from 3 to 50nm and length varies up to several microns.

II. DEVICE DESIGN AND SIMULATION SETUP

Two gates are used by the DG MOSFET that is located in symmetry covering the channels that are situated in opposition to one another as shown in Fig. 2(a). Furthermore, along the gate, the channel is formed. In such devices, similar dimensions as well as similar potential is used to connect both the gates, therefore, it is called as the symmetric DG-MOSFET. The drain field line impact over the distribution of channel potential is reduced because of the presence of double gate due to which SCE is reduced. Also, when the second gate replaces the substrate it results in the reduction in the leakage current

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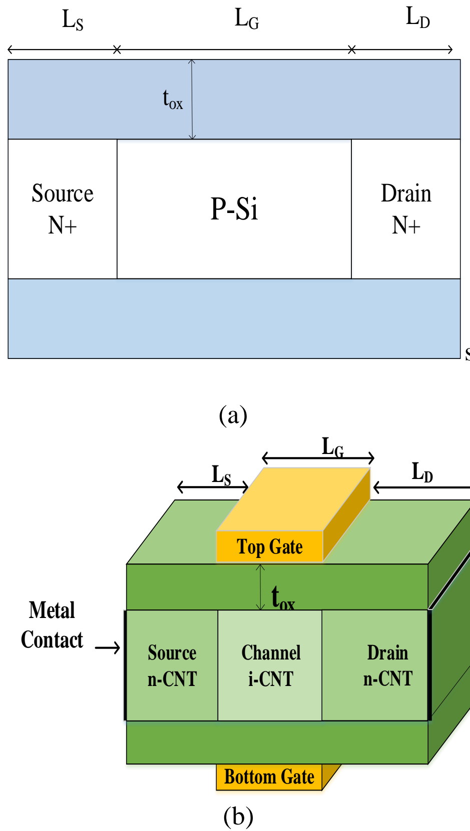
[5]. When similar work function is performed by the gates and a single input voltage is given to them, the double-gate is said to be symmetric. Conventional CNTFET is similar to the construction of conventional MOSFET. Fig. 2.(b) represents the structure of DG-CNTFET. This device uses highly doped drain and source region with n-type or p-type material. On the application of positive voltage i.e. $V_{DS} > 0$, there is a ballistic transport that allows the current to flow at the time when channel formation begins [6]. It also shows best performance in terms of I_{ON}/I_{OFF}.



(b)

Fig.2. Structure of (a) DG-MOSFET (b) DG- CNTFET where L_S = source length, L_G = gate length, L_D = drain length, t_{ox} = oxide thickness.

A. Transport Description of DG-MOSFET

1) *Drift -diffusion model*

This is the isothermal simulation based model. The devices with long active areas and low power density can use this model significantly [7]. In the semiconductors, it has been utilized as the carrier transport simulation [8].

Thus, for an electron the current density is represented as:

$$J_n = q\mu_n E + qD_n \frac{dn}{dx} \tag{1}$$

Current density for holes is represented as:

$$J_p = q\mu_p E - qD_p \frac{dp}{dx} \tag{2}$$

where, q represents the electron charge, E represents the electric field, μ_p is the mobility of holes, μ_n is the mobility of electrons, D_p represents the coefficient of hole diffusion, D_n represents the electron diffusion coefficient, *dp/dx* and *dn/dx* are the concentration gradient.

An n-channel metal gate symmetric DG-MOSFET has been designed and performance of the structure is carried out using TCAD (Technology Computer- Aided Design) simulator.

B. Transport Description of DG-CNTFET

The chiral number *(n, m)* decides the properties of the carbon nanotube which include diameter (D_{cnt}) and bandgap (E_{Gap}). The diameter can be calculated as:

$$D_{cnt} = a\frac{\sqrt{n^2 + m^2 + nm}}{\pi} \tag{3}$$

where a is the lattice constant which is given as 2.49 Angstrom. n and m are the chiral indices.

Next step is to calculate conduction minima which can be carried out using bandgap. Bandgap can be calculated using equation:

$$E_{Gap} = \frac{2aV_{pp\pi}}{d\sqrt{3}} \tag{4}$$

where $V_{pp\pi}$ is 3.033 eV which denotes the carbon π-π bond energy.

The concentration of intrinsic charge carriers η_{cnt} of nanotube is written as:

$$n_{cnt} = \int_{E_C}^{\infty} D(E) f(E) dE \tag{5}$$

where density of states is represented by *D(E)* and *f(E)*represents Fermi- Dirac distribution. Also, the *D(E)* and *f(E)* are computed by equations (6) and (7)

$$f(E) = \frac{1}{1 + e^{\frac{E - E_F}{kT}}} \tag{6}$$

where E_F describes the Fermi level of CNT, T gives operating temperature and k is represented by Boltzmann constant,. Density of states *D(E)* is represented as:

$$D(E)dE = 2\sum_i^{Allbands} \frac{4}{\pi V_{pp\pi} a\sqrt{3}} \frac{E}{\sqrt{E^2 - E_{c\min_i}^2}} dE \tag{7}$$

The concentration of intrinsic charge carriers of nanotube is rewritten as:

$$n_{cnt} = N_c I \exp\left(\frac{-E_c}{kT}\right) \tag{8}$$

where E_c is represented as conduction band energy, E_{cmin} represents the minimum conduction band energy and N_c represents the effective density of states at conduction band edge.

$$N_C = \frac{8kT}{\pi V_{pp\pi} a\sqrt{3}} \tag{9}$$

The CNTFET drain current (I_{DS}) is calculated as [9]:

$$I_{DS} = \frac{1}{\sqrt{kT}} \int_0^{6\frac{E_C}{kT}} \frac{(kTx + E_C)}{x^{1/2}\sqrt{(kTx + 2E_c)}} \exp(-x) dx \tag{10}$$

where k represents Boltzmann constant, E_C represents the conduction band energy and T is operating temperature. The above equation is solved in reference

[10]. The structure of DG-CNTFET is simulated using nanoTCAD ViDES for the following parameters.

Table 1 DG-MOSFET and DG-CNTFET device Parameters [10]

S. No.	Parameter	DG-MOSFET	DG-CNTFET
1.	Gate Length	10nm	10nm
2.	Gate Oxide Thickness	0.8nm	1 nm
3.	Silicon Film Thickness	5nm	5nm
4.	Source/ Drain Doping	4 x10^{19} cm^{-3}	5 x$10^{-3}$$cm^{-3}$
5.	Source/ Drain Length	10nm	10nm

III. RESULTS AND DISCUSSION

This section shows the evaluated results of DG-CNTFET and DG-MOSFET in term of I-V characteristics, ON current, OFF current and ON/OFF current ratio.

A. *I-V Characteristics*

The relationship among current in electronic device and voltage applied across terminals is showed by the I-V characteristics curve. Thus, the component's basic parameters are understood by using these characteristics as a tool.

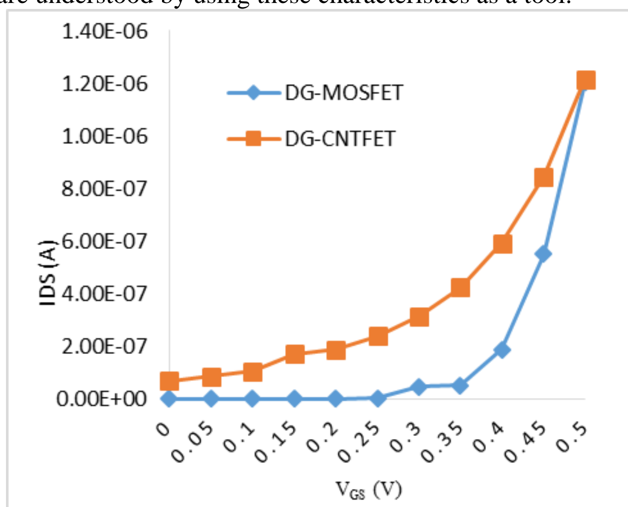


Fig. 3. I-V Characteristics of both structures.

The drain current as a function of gate voltage for DG-MOSFET and DG-CNTFET is shown in the figure 3. This curve indicates the transconductance for both the structures. As we decrease the gate voltage, transconductance of DG-CNTFET increases. As the voltage is reduced in CNTFET the channel is formed at lower gate voltage as CNT has higher dielectric values so drain current increases further transconductance. In case of DG-MOSFET as we increase the gate to source voltage, drain current rises which increases the transconductance. When we compare both these curves, DG-CNTFET shows rise in drain current and increase in transconductance at lower values of gate to source voltage. Thus, DG-CNTFET shows better current to voltage characteristics than DG-MOSFET.

B. *ON Current (I_{ON})*

When the applied voltage is more as compared to the threshold voltage, then device is ON, at this condition current is called ON current.

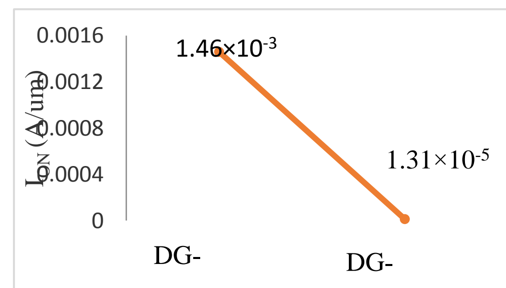


Fig. 4. I_{ON} variation for DG-MOSFET and DG-CNTFET.

Fig.4 describes the variation of ON current for DG-MOSFET and DG-CNTFET. It is depicted from the graph that ON current for DG-CNTFET is more as compared to the DG-MOSFET which clearly means that DG-CNTFET requires less time to turn ON the device.

C. *OFF Current (I_{OFF})*

An N-channel MOSFET is presented in the off-state at $V_{GS} < V_{TH.}$ Although, the source and the drain experiences an undesired leakage current. The MOSFET current is in the off-state when calculated at an N-channel MOSFET. Although, the source and the drain experiences an undesired leakage current. Furthermore, at $V_{GS}<V_{TH}$, MOSFET current is calculated that is known as sub-threshold current.

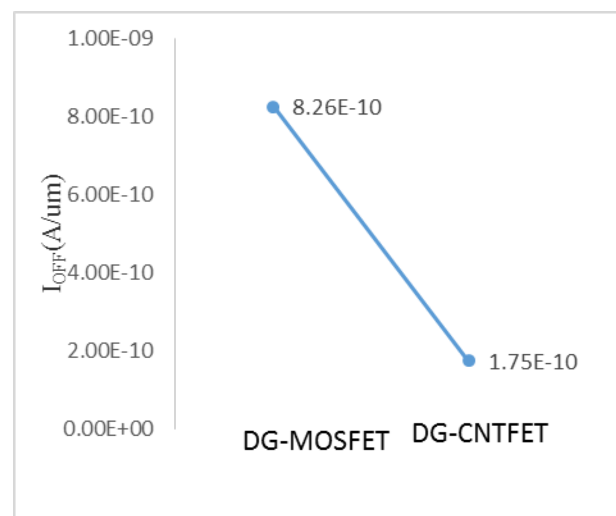


Fig. 5. Leakage current for DG-MOSFET and DG-CNTFET.

Fig.5 shows the variation of OFF current for DG-MOSFET and DG-CNTFET. In comparison with the DG-MOSFET, the DG-CNTFET shows less leakage current.

D. *ON Current to OFF Current ratio (I_{ON}/I_{OFF})*

I_{OFF} is the current at the gate voltage at V_{DS}=0V and I_{ON} is the maximum current at the gate voltage $V_{DS} = V_{DD.}$

$$I_{ON}/I_{OFF} = \log_{10} \frac{I_{ON}}{I_{OFF}} \quad (11)$$

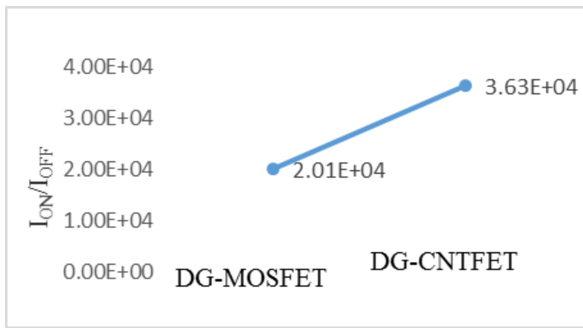


Fig. 6. I_{ON}/I_{OFF} variation for DG-MOSFET and DG-CNTFET

Device has higher value of ON current to OFF current which provide high switching speed. Fig.6 shows the variation in I_{ON}/I_{OFF}. The curve shows that the ON current to OFF current ratio is higher in case of DG-CNTFET.

CONCLUSION

This paper presented the structure of double gate carbon nanotube field effect transistor and MOSFET. The device dimensions for the structures include gate, source and drain lengths of 10nm each. Various parameters like ON current, OFF current and ON current to OFF current ratio have been evaluated for DG-CNTFET and DG-MOSFET. The OFF current of the DG-CNTFET is lesser as compared to MOSFET. It is concluded that the double gate CNTFET shows better performance in terms of ON current to OFF current ratio and ON current which further proves that CNTFET can be used as replacement for MOSFET.

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