Symmetrical Multilevel Inverter based TDVR for Voltage Quality Enhancement

Mohanasundaram Ravi, Chendur Kumaran.R

Abstract*: This Article Presents Symmetrical Multilevel Inverter With Reduced Number Of Switches Based Transformer Less Dynamic Voltage Restorer (SMLI-TDVR) For Voltage Quality (VQ) Enhancement. Reduction Of Transformer From Conventional Voltage Restorer Leads To Increase In Size Of Passive Filters, Which Can Even Reduce By Using Presented SMLI-TDVR. Reduced Filter Size And Less Load Voltage Total Harmonic Distortion Are The Added Advantage Of SMLI-TDVR. The Control Scheme Provides Switching Pulses For Closed Loop Operation Of SMLI-TDVR To Maintain Load Voltage Constant. Real Time Implementation Of Controller Is Done By Utilizing FPGA Based Real-Time Simulator Called OP4500, A Product Of OPAL-RT. Real Time Testing Of SMLI-TDVR Is Carried Out By Power Hardware In Loop Testing Method (P-HIL). Results Of P-HIL Testing Prove That SMLI-TDVR Can Able To Compensate VQ Problems To Make Load Voltage Constant With Smooth Sinusoidal Waveform.

***Keywords* : Power Quality (PQ), Voltage compensation, Dynamic Voltage Restorer (DVR), Multilevel Inverter (MLI) , Power Hardware in Loop (P-HIL), OPAL-RT**

I. INTRODUCTION

Power distribution system should maintain Power Quality (PQ) to avoid financial losses for both customers and suppliers. Voltage Quality problems like sag, swell and unbalance are common problems that are faced by customers [1]. These problems are threat for a sensitive device which causes damage or even shutdown. Standards given by IEEE standard 1159:2009 and 519:2014 are to be followed to maintain better PQ [2], [3]. Dynamic Voltage Restorer (DVR) is an effective solution for voltage restoration. A conventional DVR is connected with the line through a series transformer which makes system cumbersome, require more space and expensive [4], [5]. Recent years Transformer less DVR (TDVR) is introduced to overcome these issues [6]. However required filter size, Total Harmonic Distortion (THD) and complexity in closed loop control operation can be even reduced by using MLI instead of two level VSI used. Recent years many topologies are emerged with reduced component count in MLI with same output level and reduced THD as conventional [7]. Symmetrical Multi Level Inverter (SMLI) are easy to control, hence SMLI is choose for this presented SMLI-TDVR.

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Thus this advantageous SMLI is used in TDVR called SMLI based TDVR for even better output than existing. Power Hardware In Loop (P-HIL) testing method carried out for testing of SMLI-TDVR utilizing a real-time simulator OP4500 [8]. Real world communication of OP4500 with power device under test (MLI with filter circuit) is achieved through Analog I/O and Digital I/O channels of OP4500. Configuration of SMLI-TDVR is presented in section II. Followed by Configuration of SMLI is presented in section II A. control strategy for generate error signal in section II B and pulse generation method in II C. Simulation results of SMLI-TDVR are present in section III. Hardware prototype testing of MLI-TDVR is presented in section IV. Conclusion of this work given in section V.

II. MULTILEVEL INVERTER BASED TRANSFORMERLESS DYNAMIC VOLTAGE RESTORER (MLI-TDVR)

Configuration of SMLI-TDVR for Voltage compensation is shown in the Fig. 1. Source voltage from the grid power supply V_s is supplied to a Point of Common Coupling (PCC) with line resistance R_s and line reactance L_s. Sensitive load and other loads are connected to this PCC. SMLI-TDVR is connected in series with the line in between PCC and sensitive load to be protected from voltage quality problems occurring at PCC. SMLI-TDVR consists of SMLI, DC energy source, filter circuit and a controller. SMLI consist of a Symmetrical Multi-Level DC (SMLDC) circuit connected as input of H-Bridge Voltage Source Inverter (VSI). SMLDC consist of four DC source V_{dcs} , V_{dc1} , V_{dc2} and V_{dc3} . Three IGBT switches S_1, S_2 and S_3 in SMLDC are connected in series with three DC voltage sources V_{dc1} , V_{dc2} and V_{dc3} respectively. These IGBT switches in SMLDC are controlled by switching pulses, generated from SMLDC pulse generation unit. Four reverse bias diodes D_1 , D_2 , D_3 and D_4 are connected parallel to each DC source which act as a bypass diode when any DC voltage source disconnect from the circuit. Output voltage of SMLDC (V_{mldc}) is fed as an input supply for VSI.

VSI consist of four IGBT switches S_4 , S_5 , S_6 and S_7 which are controlled by VSI pulse generation unit. VSI voltage is filtered by filter inductor L_f and filter capacitor C_f to make SMLI-TDVR output voltage V_{inj} as sinusoidal. SMLI-TDVR should inject voltage V_{inj} such that load voltage V_{load} should maintain constant magnitude as 1p.u with smooth sinusoidal waveform. Load voltage V_{load} is equal to PCC voltage V_{pcc} and V_{inj} as given in (1) [9], [10].

$$V_{load}=V_{pcc}+V_{inj} \quad (1)$$

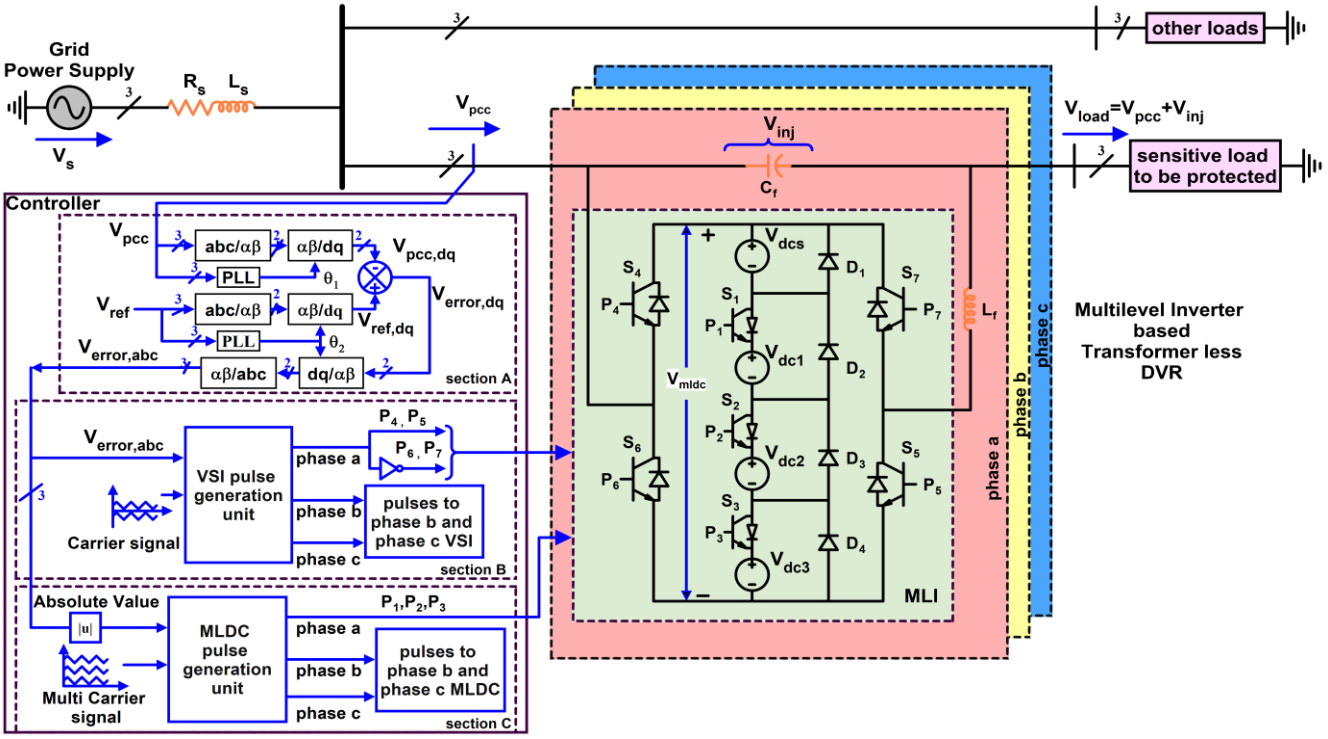


Fig. 1. Configuration of MLI-TDVR in distribution system

A. Symmetrical Multilevel inverter (SMLI) based TDVR.

SMLI input DC voltages sources from V_{dcs} to V_{dc3} are equal potential in the ratio of 1:1:1:1. The k[th] DC voltage value of source is given by following (2).

$$V_{dck} = V_{dc} \quad (2)$$

Where V_{dc} is the base voltage of input DC source and V_{dck} is the k[th] DC voltage ranges from 1,2,…n. Maximum level of Symmetrical MLDC (SMLDC) N_{dcm} is given in (3).

$$N_{dcm} = \left(\sum_{k=1}^{n} (V_{dck}) \right) \quad (3)$$

Maximum level of SMLI output waveform is given by following (4).

$$N_{acm} = 2(N_{dcm}) + 1 \quad (4)$$

Number of IGBT switches present in SMLDC S_{dcm} is given by following (5).

$$S_{dcm} = (N_{dcm}) - 1 \quad (5)$$

Total number of switches present in SMLI S_{acm} is equal to number of switches present in MLDC and number of switches present in VSI as given by (6).

$$S_{acm} = (S_{dcm}) + 4 \quad (6)$$

B. Controller

Control strategy of SMLI-TDVR consists of three sections as shown in Fig. 1. Section A consists of error signal generation for SMLI-TDVR for compensation during voltage disturbance. Section B and section C consists of generation of pulses for the switches present in VSI and SMLDC respectively.

1. Generation of error signal

In this paper Clark and park transformations are utilized for generation of error signal. Section A in Fig. 1 shows generation of error signal for SMLI-TDVR. The SMLI-TDVR should inject voltage such that load voltage magnitude is maintained as 1 per unit (pu) constant with smooth sinusoidal waveform. Let the three-phase PCC voltage V_{pcc} as given in (7-9) is sensed and converted into alpha v_α and beta v_β quantities, as given in (10a-10b). This v_α and v_β are calculated from the matrix equation given in (10). This two phase stationary frame quantities is converted into two phase reference frame quantities v_d and v_q as per given in (11a-11b) and calculated from the matrix equation (11). Phase Lock Loop (PLL) connected to PCC generates θ_1, which is used in park transformation for

generation of synchronization reference frame . Similarly by applying same clark and park transformation, the reference three phase sinusoidal voltage v_{ref} is converted into D and Q axis. These reference axis $v_{(ref,dq)}$ is compared with v_{dq} to get the error signal as $v_{(error,dq)}$ as given in (12). PLL connected to v_{ref} generates θ_2 which is used for synchronization of V_{inj} with V_{pcc}. This error $v_{(error,dq)}$ is again converted in to three phase voltage signal as represented as $v_{(error,abc)}$ by means of inverse park transformation as per (13-13b) and inverse clark transformation given in (14–14c) respectively.

$$v_a = v_m \sin(2\pi f_f t - \delta) \tag{7}$$

$$v_b = v_m \sin(2\pi f_f t - \frac{2\pi}{3} - \delta) \tag{8}$$

$$v_c = v_m \sin(2\pi f_f t + \frac{2\pi}{3} - \delta) \tag{9}$$

Where, v_a, v_b, v_c are the three phase voltages, v_m is the magnitude of PCC voltage, f_f is the fundamental frequency and δ is the changing load angle. Clark transformation matrix is given as below.

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \tag{10}$$

hence,

$$v_\alpha = \sqrt{\frac{2}{3}} v_a - \frac{v_b}{\sqrt{6}} + \frac{v_c}{\sqrt{6}} \tag{10a}$$

$$v_\beta = \frac{\sqrt{3}}{2} v_b - \frac{\sqrt{3}}{2} v_c$$

(10b)

Conversion of direct and quadrature axis from alpha and beta quantity done by using the following matrix

$$\begin{pmatrix} v_d \\ v_q \end{pmatrix} = \begin{pmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{pmatrix} \begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} \tag{11}$$

hence

$$v_d = (v_\alpha \cos\omega t + v_\beta \sin\omega t) \tag{11a}$$

$$v_q = (-v_\alpha \sin\omega t + v_\beta \cos\omega t)$$

(11b)

Compensation voltage to maintain load voltage constant is calculated by comparing reference dq axis $v_{(ref,dq)}$ with sensed PCC voltage dq axis v_{dq}.

$$v_{(error,dq)} = v_{(ref,dq)} - v_{dq} \tag{12}$$

Inverse Conversion of direct and quadrature axis to alpha and beta quantity done by using inverse park's transformation by using following matrix.

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \begin{pmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{pmatrix} \begin{pmatrix} v_d \\ v_q \end{pmatrix} \tag{13}$$

hence,

$$v_\alpha = (v_d \cos\omega t - v_q \sin\omega t) \tag{13a}$$

$$v_\beta = (v_d \sin\omega t + v_q \cos\omega t)$$

(13b)

Matrix conversion of alpha and beta quantities to three phase voltages which is to be injected by TDVR as given below

$$\begin{pmatrix} v_{error,a} \\ v_{error,b} \\ v_{error,c} \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} \tag{14}$$

hence,

$$v_{error,a} = \sqrt{\frac{2}{3}} v_\alpha \tag{14a}$$

$$v_{error,b} = \frac{-v_\alpha + \sqrt{3} v_\beta}{\sqrt{6}} \tag{14b}$$

$$v_{error,c} = \frac{-v_\alpha - \sqrt{3} v_\beta}{\sqrt{6}} \tag{14c}$$

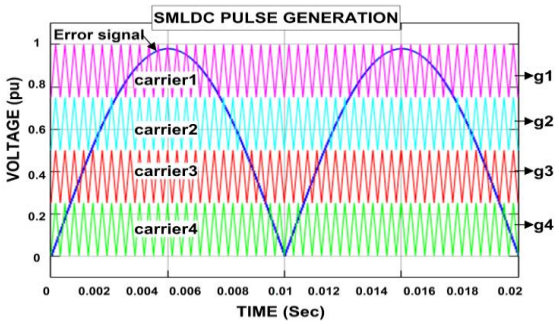
This three-phase voltage error signal is used to generate pulses for the switches present in the SMLDC and VSI by using Multicarrier Phase Disposition Pulse Width Modulation (MCPDPWM) and Sinusoidal Pulse Width Modulation (SPWM) techniques respectively.

C. Pulse Generation

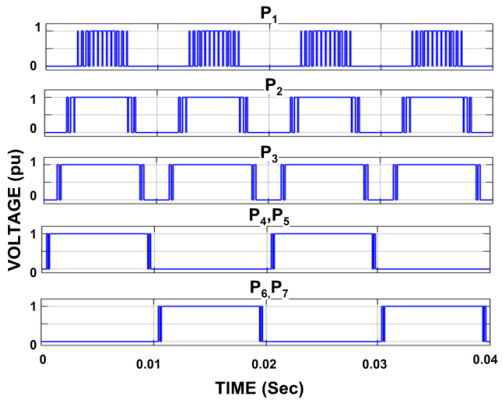
Section C in Fig. 1 shows SMLDC control block diagram. P_1, P_2 and P_3 are the switching pulses generated from SMLDC pulse generation unit.

1. Pulse Generation for SMLDC

Gate pulses for SMLDC switches are generated by using MCPDPWM. For closed loop operation of SMLI-TDVR, the error signal generated in (14a) is compared with four different DC offsets of carrier wave with 5 Khz switching frequency f_{sw} for generating g_1, g_2, g_3 pulses, as shown in Fig 2a. Following (15-17) are the switching pulses given to SMLDC circuit for phase a. Fig 2b shows P_1, P_2 and P_3 switching pulses supplied to phase a SMLDC for switches S_1, S_2, and S_3 respectively.



(a)



(b)

Fig. 2. (a) MLDC pulse generation, (b) switching pulses of MLDC switches.

$$P_1 = g_1 \quad (15)$$

$$P_2 = g_2 \quad (16)$$

$$P_3 = g_3 \quad (17)$$

Table I gives switching states of SMLDC switches with respect to number of SMLDC output voltage levels and output voltage magnitude.

Table- I: SMLDC switching states.

Output levels	SMLDC Switching states			Output Voltage Magnitude
	S_1	S_2	S_3	
1	Off	Off	Off	V_{dcs}
2	On	Off	Off	$V_{dc1}+V_{dcs}$
3	On	On	Off	$V_{dc1}+V_{dc2}+V_{dcs}$
4	On	On	On	$V_{dc3}+V_{dc2}+V_{dc1}+V_{dcs}$

2. Pulse Generation for VSI

SPWM technique is used for generation of switching pulses for VSI switches. P_4, P_5, P_6 and P_7 are the switching pulses for the VSI switches S_4, S_5, S_6 and S_7 respectively. VSI switches operate at fundamental frequency of 50Hz. During Voltage sag VSI operates in phase with V_{pcc} and during swell VSI operates 180 degree phase shift with V_{pcc} for voltage compensation.

Table II shows switching states of VSI switches during voltage sag, swell and normal conditions when there is no disturbance.

Table- II: VSI switching states

Conditions	Switching states			
	S_4	S_5	S_6	S_7
Voltage sag	On	On	Off	Off
Voltage swell	Off	Off	On	On
No disturbances	Off	Off	Off	Off

III. SIMULATION RESULTS AND DISCUSSION

Fig 3 shows single phase simulated symmetrical multilevel DC output voltage waveform and nine level SMLI inverter output voltage waveform. SMLI output voltage levels are calculated by (4).

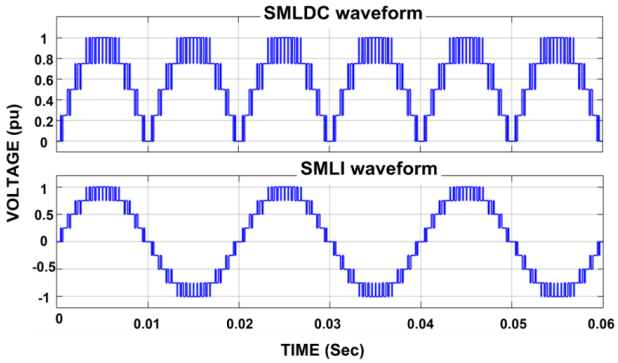


Fig. 3. SMLDC and SMLI output voltage waveforms

It is observed that magnitude of output voltage is constant 1 Per Unit (pu) with three cycles. V_{dc} for each DC input voltage is supplied as 35V and hence maximum of 140V. Simulated System parameters for SMLI-TDVR are given in Table V. SMLI-TDVR starts operate when error signal is calculated by sensing voltage quality problems present at V_{pcc} .. SMLI-TDVR injects voltage such that it should compensate V_{pcc} to maintain load voltage magnitude constant. Fig 4 shows voltage sag, swell, and unbalance compensation done by SMLI-TDVR. Voltage sag occurring from time 0.05secs to 0.01secs with change in magnitude from nominal 1 pu to 0.4 pu. During sag V_{inj} injects 0.6 pu of voltage to make load voltage V_{load} magnitude constant 1 pu. Voltage swell occurring from time 0.15secs to 0.2 secs with change in magnitude from nominal 1pu to 1.3 pu. During swell 180 degree phase shift of 0.3 pu voltage injected by V_{inj} . Voltage magnitude unbalance occurring from time 0.25secs to 0.3 secs in phase b and phase c. Voltage magnitude of these phases changes from 1 pu to

0.8 pu. During unbalance V_{inj} injects 0.2 pu of voltage on phase b and phase c. N_{acm} varies from maximum nine level to depend on the amplitude of error signal.

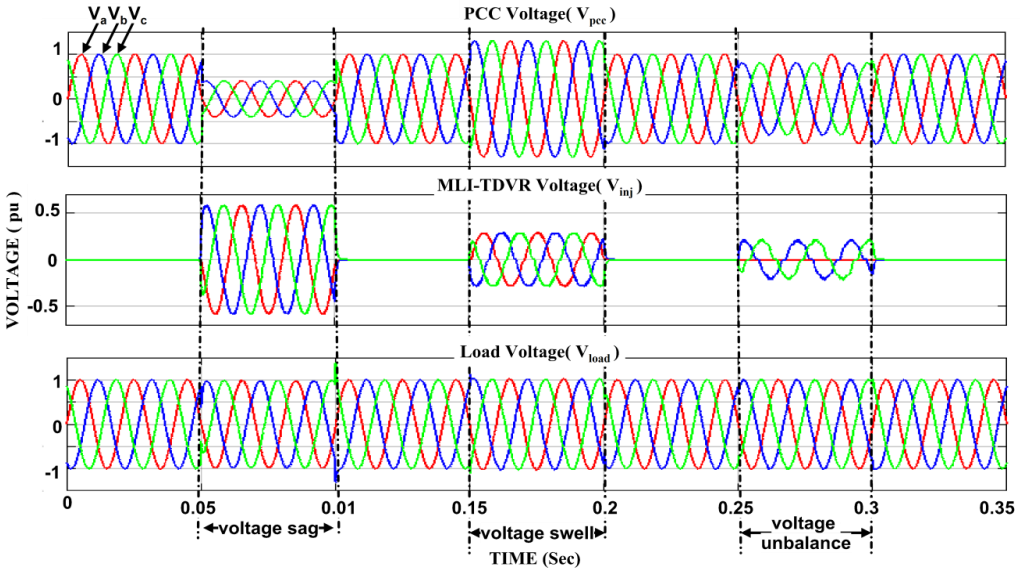


Fig. 4. Voltage Compensation of sag, swell, unbalance by SMLITDVR

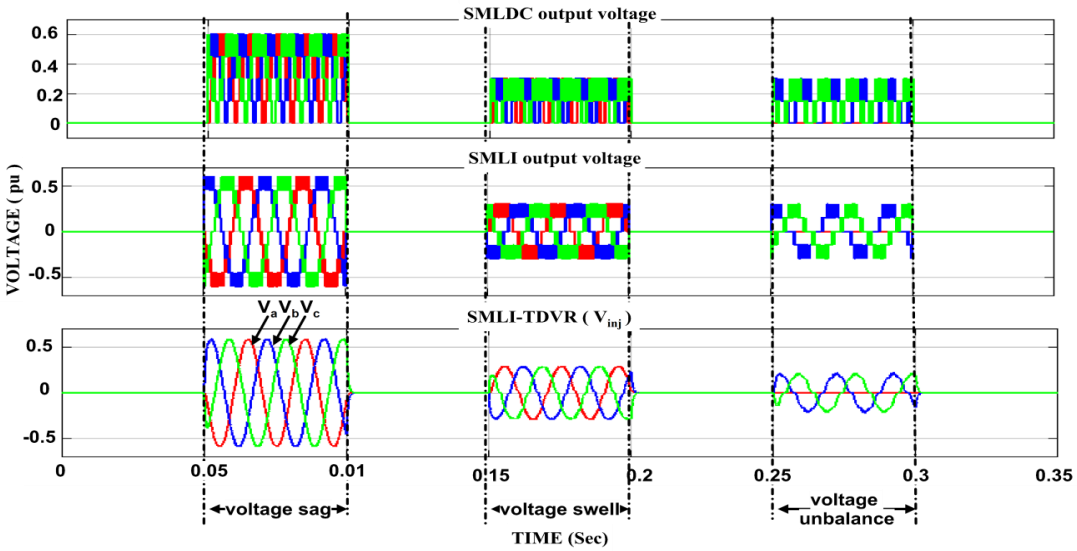


Fig. 5. Voltage injection of SMLI based TDVR during compensation.

Conditions	SMLI-TDVR		
	V_{pcc} *(pu)*	V_{inj} *(pu)*	N_{acm}
Voltage sag	0.6	0.4	9
Voltage swell	1.3	-0.3	5
Voltage unbalance	0.8	0.2	5

Fig 5 shows waveform of SMLDC output voltage, SMLI output voltage without filtered and SMLI with filtered. During 60% voltage sag 9 level output voltage generated by SMLI, during 30% voltage swell 5 level SMLI output voltage generated and during unbalance 5 level of output voltage generated by SMLI. Voltage level of SMLI during compensation given in Table III. Total Harmonic Distortion (THD) of SMLI output voltage with filter and without filter for voltage sag, voltage swell and voltage unbalance are given in Table IV.

Table- III: SMLI-TDVR voltage level

Table- IV: THD of SMLI-TDVR during compensation

Conditions	SMLI output voltage THD			SMLI based TDVR V_{load} THD %
	Without Filter THD %	*With filter THD %*	N_{acm}	

Voltage sag	9.4	1.61	9	1.1
Voltage swell	18.94	5.37	5	1.52
Voltage unbalance	28.87	11.71	5	2.32

Table- V: System parameters

Parameters	Value	Description
V_s	415 Vrms	Three phase
f_f	50Hz	Fundamental frequency
l_f	10mH	SMLI Filter inductor
c_f	10uF	SMLI Filter capacitor
V_{dc}	35V	SMLDC, Base voltage
f_{sw}	5KHz	Switching frequency
T_s	20KHz	Sampling frequency

IV. HARDWARE RESULTS AND DISCUSSION

Fig 6 shows configuration of P-HIL testing method [11]. Which includes a host computer with RT-Lab v11 is connected to a real time simulator (OP4500) through a server by means of TCP/IP.

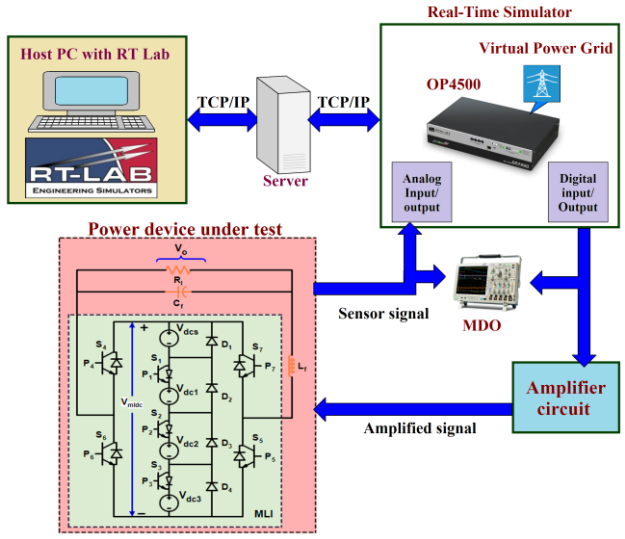
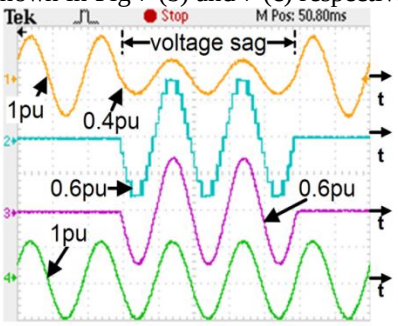
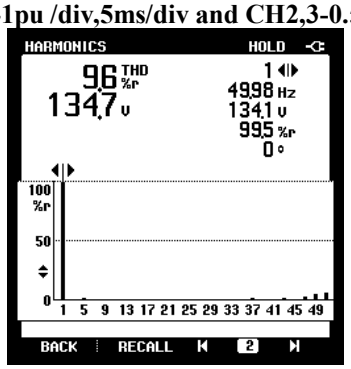


Fig. 6. P-HIL testing method.

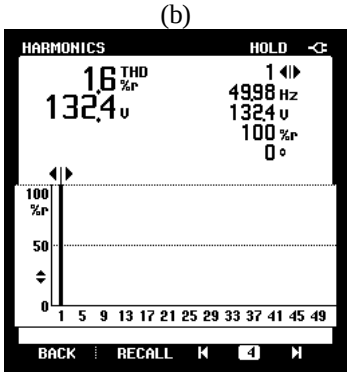
Computer modelled real time power system consist of sag, swell and unbalance problems and controller are made virtually built in OP4500. Real world communication of OP4500 with power device under test (SMLI with filter circuit) is achieved through Analog I/O (AIO) and Digital I/O (DIO) channels of OP4500. Amplifier circuit amplifies digital signal from OP4500 to the switches present in MLI. Analog signal from power device under test is sensed and given as analog input signal to OP4500 for closed loop operation of SMLI-TDVR. Thus dynamic performance of MLI-TDVR is validated in real time. Fig 7 (a) shows DSO waveform of SMLI-TDVR during voltage sag condition. Channel 1 shows V_{pcc} voltage generated by opalrt consists of 60% sag. Channel 2 shows SMLI output waveform without filter for compensation voltage sag. Channel 3 shows filtered sine wave for compensation. Channel 4 shows load voltage after sag compensation. THD of SMLI without filter and with filter shown in Fig 7 (b) and 7 (c) respectively.



(a) CH1-V_{pcc}, CH2-V_{smli}, CH3-V_{inj}, CH4-V_{load}. CH1,4-1pu /div,5ms/div and CH2,3-0.5pu/div

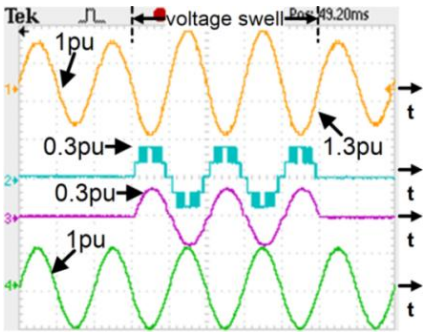


(b)



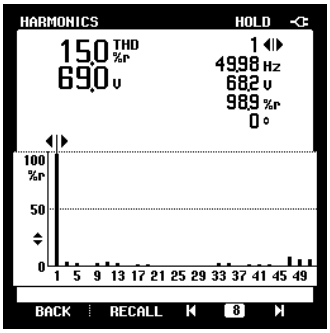
(c)

Fig. 7. (a) performance of SMLI-TDVR during 60% voltage sag. (b) THD of SMLI without filter,(c) THD of SMLI with filter.



(a) CH1-V_{pcc}, CH2-V_{smli}, CH3-V_{inj}, CH4-V_{load}.

CH1,4-1pu /div,5ms/div and CH2,3-0.5pu/div



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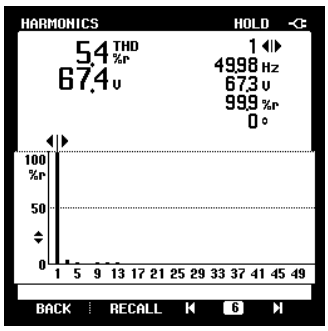

(c)

Fig. 8. (a) performance of SMLI-TDVR during 30% voltage swell. (b) THD of SMLI without filter,(c) THD of SMLI with filter.

Fig 8 (a) shows DSO waveform of SMLI-TDVR during voltage swell condition. Channel 1 shows V_{pcc} voltage generated by opalrt consists of 30% swell. Channel 2 shows SMLI output waveform without filter for compensation voltage swell. Channel 3 shows filtered sine wave for compensation. Channel 4 shows load voltage after swell compensation. THD of SMLI without filter and with filter shown in Fig 8 (b) and 8 (c) respectively.

V. CONCLUSION

VQ problems are compensated to make load voltage magnitude constant for protecting sensitive load. Dynamic performance of SMLI-TDVR verified using simulation and as well as hardware prototype. P-HIL testing method carried out for effective validation of SMLI-TDVR performance in real time using OP4500. Experimental results prove that SMLI-TDVR capable to compensate VQ problems such as voltage sag, swell and unbalance. It is found that presented SMLI-TDVR requires reduced filter size, reduced number of MLI components, lesser switching frequency and increased level of voltage compensation for better output.

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