

Design 10-Transistor (10t) Sram using Finfet Technology

Jyoti Verma, Abhiruchi Passi, Savita Sindhu, S.Gayathiri

Abstract: This paper discuss designing of low power, high-speed 10-Transistor (10T) SRAM and analysis of SRAM cell in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and FinFET technology. MOSFET is used widely in many areas, but below 40 nm technology control of channel region becomes extremely difficult. So there is a necessity for new innovative technology which allows designers to design below 40nm technology and can offer excellent control over gate thus reducing short channel effects. The designing of SRAM is analyzed using TANNER EDA tool and Microwind.

Keywords : VLSI, Micro Wind, Tanner EDA, VDD, SRAM, Delay, Power, Temperature.

I. INTRODUCTION

Very Large Scale Integration (VLSI) is the process of integration in which many transistors are packed on to a single integrated circuit. Initially, power dissipation was low due to low device density and operating frequency, but nowadays due to miniaturization of an integrated circuit, power dissipation is high and it has become a significant problem. Miniaturization of Complementary Metal – Oxide - Semiconductor (CMOS) becomes extremely difficult below 32nm as it leads to short channel effects (SCE). These effects arise when electric field lines from drain and source affect the channel region [Lu and Fossum, 2007; Sathe and Sarwade, 2014]. To resolve this problem, multi-gate device can be used as it offers better control over the channel region. FinFET (Fin-Field Effect Transistor) is the best device among all multigate FETs (Field Effect Transistor) as it has greater control over the channel region. FinFET has fins which act as gate and provide direction to electron between source and drain. This device has two gates in which 2nd gate is opposite to the 1st gate, offering negligible short channel effects. FinFET offers various design options. It works on several modes for instance shorted gate, independent gate, low power mode and hybrid mode which is a combination of both independent gate mode and low power mode [Wang 2009; Lin et al., 2011; Kato et al., 2013; Rajprabu et al., 2013]. From the Fabrications viewpoint, FinFET devices are same as CMOS device. Due to higher gate control, FinFET gives better performance advantages at very low power.

According to the International Technology Roadmap for semiconductor (ITRS), 2011 static random access memory (SRAM) uses 70% area of an integrated circuit, so the

ultimate performance of an integrated circuit depends on SRAM. FinFET is better than CMOS for SRAM designing as it will provide low power consumption and will be more reliable.

II. EXISTING 6T SRAM CELL

A. CELL STRUCTURE

The conventional DESIGN 6T SRAM consists of 6 transistors. It has 2 inverters and 2 access transistors. It performs three operations read operation, hold operation, and write operation. SRAM stores binary information and it do not need a refresh circuit as the RAM. One of the disadvantages of SRAM is it is expensive. So a combination of SRAM and DRAM is used in systems

1) 6T SRAM CELL OPERATIONS

a. HOLD OPERATION

In hold mode Word line $WL = 0$ and the access transistor M_5 and M_6 is turned off so data cannot be accessed by bit lines. The inverter continues to feed one another and data remains inside the latch provided that it is connected to power supply.

b. READ OPERATION

In this, BL and BLB are pre-charged to $V_{DD}/2$ and then the word line is set high i.e. $WL=1$. After that access transistor M_5 and M_6 are enabled, and the latch cell is connected to BL and BLB. Values stored in Q and QB is transferred to the BL and BLB. If logic '1' is stored in node 'Q', then the value of BL is pulled to V_{DD} , and BLB is discharged to logic '0' this process takes place via M_4 and M_6 transistors.

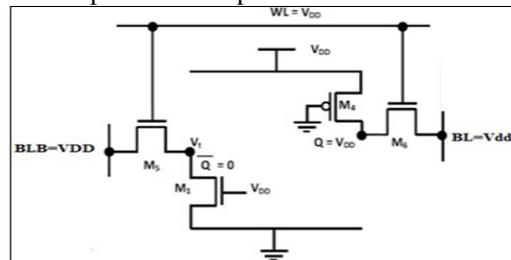


Fig. 1. SRAM cell Read Operation [Dani et al., 2015]

c. WRITE OPERATION

In this mode word-line $WL=1$. Data to be written is given to respective bit-Suppose logic "1" is stored and logic "0" is to be written then BL is lowered

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to 0V and BLB is increased to VDD line.

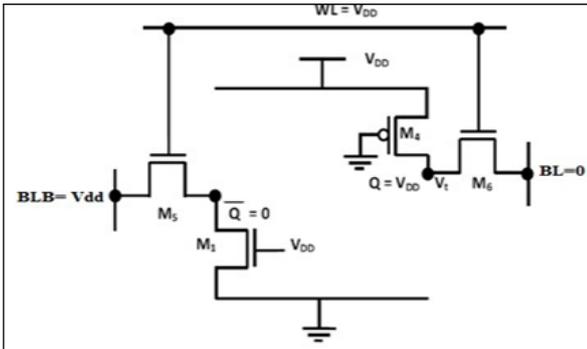


Fig. 2. SRAM cell Write Operation [Dani et al., 2015]

III. SRAM CHALLENGES

A. POWER DISSIPATION

Power dissipation leads to increase in device temperature. This increase in temperature affects the device even when it is turned off or on. Power dissipation adversely affects the performance of the memory. The FinFET technique helps to reduce power consumption in SRAM [Narendar et al., 2012; Khandelwal et al., 2013].

B. PROPAGATION DELAY

tp of the gate is measured as that delay when a signal is passed through a gate. It is expressed as the average of response time of gate for low to high transition and response time of gate for high to low transition.

$$\tau_p = \frac{(\tau_{PLH} + \tau_{PHL})}{2}$$

τ_{PHL} - response time for a low to high transition

τ_{PLH} - response time of gate for high to low transition.

Delay calculation is significant for any digital circuit. As the power supply is scaled down, delay is increased [Agostinelli et al., 2010; Mishra and Akashe, 2013; Moshgelani et al., 2013; Pappachanet. Al., 2013]. This delay should not be high as it affects the functioning of circuits.

IV. RELATED WORK DONE

In 2008, tawfik and kursun have proposed new latches and flip-flops based on independent-gate finfets to simultaneously reduce the power consumption and the circuit area and independently biased double-gate finfet sequential circuits. It help in reduction of the active power consumption, the clock power, the leakage power, and the circuit area. [tawfik and kursun , 2008]

After that, in 2013, Lourts et al. designed 6T SRAM for SG mode as well as IG mode of FinFET and saturation and linear current for different front gate bias (VFG) and back gate bias (VBG) also calculated with its drain current (IDS). In this paper comparison of bulk CMOS based 6T SRAM and FinFET based 6T SRAM for SG/IG mode has been carried out and leakage power, dynamic power, delay for writing and reading operation, and SNM for write operations are calculated. It can be concluded that the delay of CMOS based

SRAM design is more for read and write operation compared to FinFET based SG/IG modes. with FinFET based SG and IG modes, SG mode design is giving better performance at all the load level since IG mode has uneven pull-up and pull-down transistor which causes the unequal delay in the circuit [Lourts et al. 2013; Suryanshi et al., 2013]

Scaling of CMOS beyond 22nm offers some undesired features such as short channel effects. In 2014, Farkhani et al. have made comparison between FinFETs and 22-nm bulk CMOS to observe the challenges and the potentials of using FinFET and traditional bulk CMOS technologies for future electronic devices. Result analysis shows that FinFETs are the promising replica especially for applications for which lowest process variations, lowest leakage power consumption is crucial. [Farkhani, H et al. 2014]SRAM has primary design problems for instance high speed, low power. To improve efficiency and performance of system the speed and stability of SRAM are important issues. Stability of the SRAM depends on the static noise margin (SNM). so the noise margin is also important parameter for the design of memory because the higher noise margin confirms the high speed of the SRAM cell. One of the most important design objective for SRAM is power reduction. In this paper, a low power, low delay and high SNM SRAM cell is designed. Moreover power consumption and delay of the improved 8T SRAM cell is analysed and compared with that of conventional 6T, 7T, 8T and 9T SRAM cell. The new proposed 8T SRAM cell have shown improvement in delay and static noise margin. There is a significant reduction in delay and an increase in static noise margin in hold state. [Singh and Jain, 2015; Nalamwar and Bhosale, 2015; Saranya and Kalarani, 2015; Verma et al., 2015]In most recent times Stability is a critical parameter for SRAM. Since bulk CMOS cannot be scaled beyond certain size because of the issues it offer. A new device can replace bulk CMOS because of the numerous advantages it offers over bulk CMOS. Along these lines, FinFET SRAM comes as the other option to substitute Si-bulk SRAM. FinFET because of two gates have better control over OFF current is used in memory array. In present scenario, memories occupies a huge part of SOC and mobile applications. However, design of SRAM became more challenging in deep technology. We have leakage mainly from big memory arrays in idle state and it is because of the process variations of the device and SECS. The Si bulk CMOS in deep nano-meter is no longer stable and also not able to meet the design standards. Stability and leakage power are more significant factors in deep scaling. In this paper FinFET devices schemes are assessed and compared. Also, different types of FinFET SRAM schemes are evaluated and compared [Darwich, M. et al 2016; Kumar, V. et al. 2016; Kaur, N., et al. 2016]SRAMs occupy most of the area on system-on-a-chip (SOC). so while designing SRAM various parameters needs to be taken care of. CMOS were mainly used to design SRAM cells but with the advancement in technology and the growing demand of devices in nanometer regimes arises the need to further scale CMOS. which resulted in problems like current leakage, because of short channel effects we cannot scale CMOS beyond 22nm. FinFET is most prominent multi-gate after field effect transistor. In 2016, Kaur et al. designed a 10T SRAM using "Threshold voltage" technique. This technique is used in read out path in order to reduce source body voltage and leakage power. For this

P-MOS is used at read-out path. This technique reduces read access time and has large static-signal-to-noise ratio as compared to 6T SRAM. This technique is able to significantly reduce the power delay product, leakage current in comparison to traditional 6T SRAM cell [Kaur, N., et al. 2016]

V. METHODOLOGY FOR DESIGNING SRAM WITH FIN-FET TECHNOLOGY

In proposed technique we have smaller size transistors in input circuitry which result in reduction in switched capacitance and clock load hence the power consumption of independent gate FinFETs is reduced as compared to circuits with tied gate. Moreover, with the help of proposed technique area is reduced significantly.

A. 6-TRANSISTOR SRAM

The proposed 6T SRAM consists of six transistors, and one data bit can be stored in a 6T cell. 6T SRAM is commonly used since it occupies very less area, but it has some stability issues. It has two cross-coupled inverters and two access transistors. For proper operation of the cell, there is word line (WL), bit-line (BL) and bit-line-bar (BLB). When WL=1 only then the access transistors are enabled and read/write operations can be performed

Fig. 3 shows 6T FinFET SRAM it has two inverters. First inverter is made if M1 and M2 transistor and second inverter is made if M1 and M2. There are two access transistors M5 and M6. For read and write operation bit-line, world-line, bit-line-bar is also present.

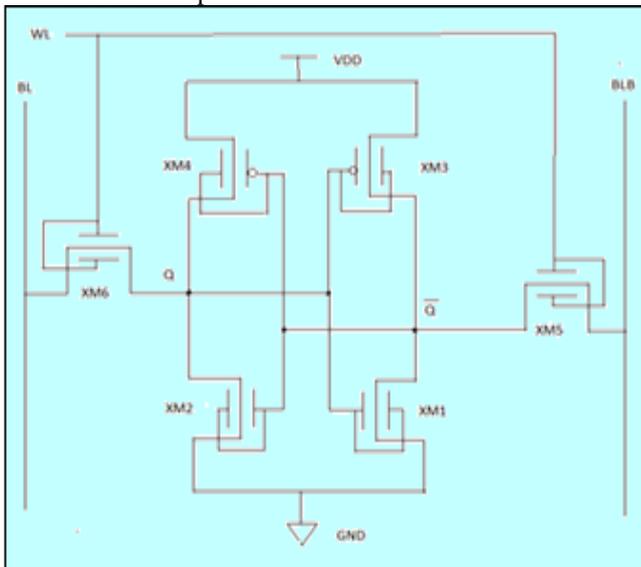


Fig. 3. 6T SRAM FinFET

Fig. 3 shows 6T FinFET SRAM it has two inverters. First inverter is made if M1 and M2 transistor and second inverter is made if M1 and M2. There are two access transistors M5 and M6. For read and write operation bit-line, world-line, bit-line-bar is also present.

B. 8-TRANSISTOR SRAM

8T SRAM has an almost similar structure as 6T SRAM, in addition, it has two NMOS transistors. In 6T SRAM there were stability issues to overcome this problem two additional transistors are used in 8T SRAM. It is useful in multimedia application. For read operation in 8T SRAM read-bit-line

(RBL) is pre-charged to full swing. Assuming $Q = "0"$ then transistor M6 and turned on and RBL is discharged via M5 and M6 to ground. The sense amplifier detects the decrease in voltage of RBL. In read "1", $Q = "1"$ and transistor M6 stays in off state. And there is no discharge of current flow in read path. Write operation of 8T is same as it is in 6T SRAM but write driver is present in place of pre-charge circuit.

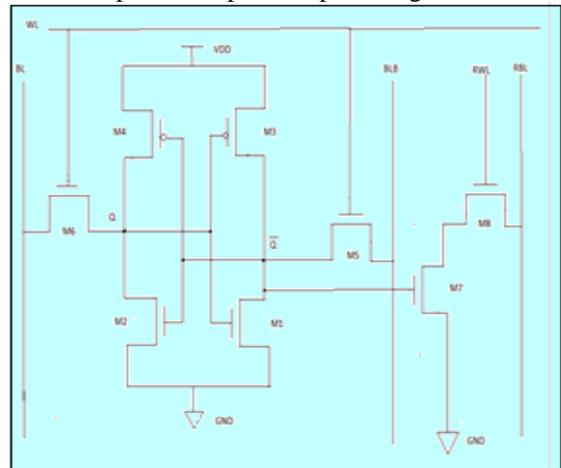


Fig. 4. SRAM 8 T

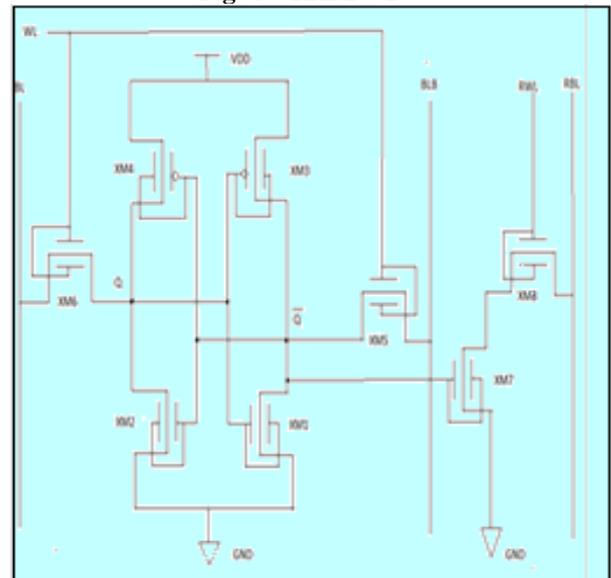


Fig. 5. SRAM 8TFinFET

C. 10-TRANSISTOR SRAM

10T SRAM has ten transistors in which there are two inverters. The first inverter is composed of M1-M3 transistors. The second inverter is made up of M2-M4 transistors. In this cell, M5 and M6 are access transistors. M7 and M8 provide a way for the read operation. To connect read path to any of write bit line M9 and M10 transistors are used. Word line (WL) signal controls M5 and M6 transistors, and it is enabled during the write operation. Read-word-line (RWL) controls transistor M7 and M6. And row decoder controls word line and read-word-line signals.

Fig. 8. SRAM 6T FinFET (Write) In the write operation, WL is high which turns on M5 and M6 transistors. In 10T SRAM write operation is similar to 6T SRAM. In read operation RBL is pre-charged to full swing and read-word-line is asserted and after that M7 and M9 are turned on. If $Q = "1"$, M8 is turned off, and current discharge

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via read path but when Q='0' then M8 is on, and read-bit-line discharge and sense amplifier detect this fall in voltage of read-bit-line.

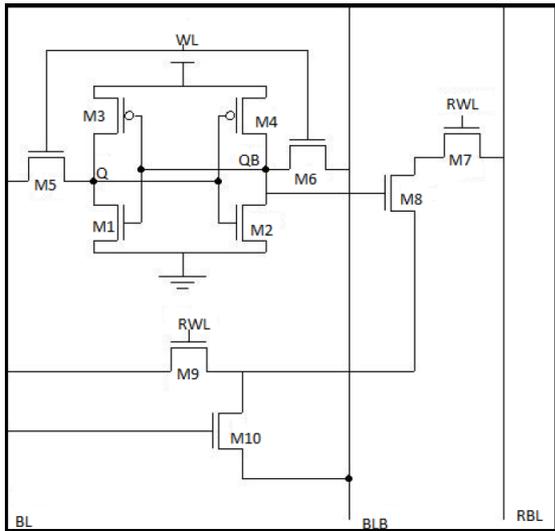


Fig. 6. 10T SRAM cell MOSFET Technology

VI. POWER REDUCTION TECHNIQUE

There is a problem when read '1' operation is performed, a small leakage current flows known as bit line leakage. To overcome this problem, one more transistor is used in read path. By using another transistor bit line leakage is reduced and this process is called stacking effect.

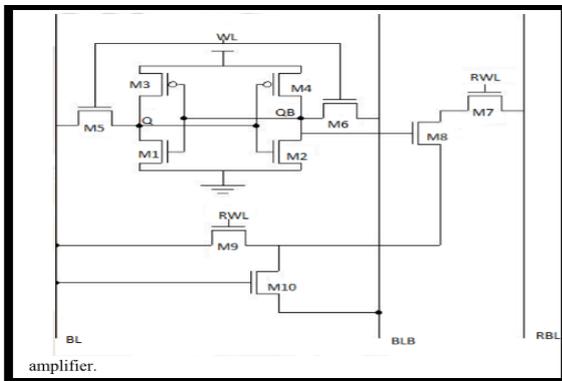


Fig. 7. 10T SRAM cell

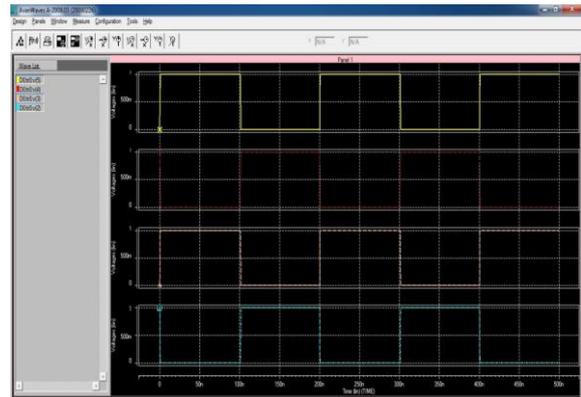
To decrease read power, RBL swing is reduced. When read '0' is performed charge sharing is done between RBL and BLB or RBL and BL accordingly whether last data written is '1' or '0' respectively. RBL is not discharged properly because of charge sharing, and it remains at middle-level of voltage, during next cycle pre-charge circuit uses less power. The bit line is driven from middle-voltage value to full swing voltage.

To decrease write operation power write driver is used. The bit line is driven high or low using write driver according to the data value. When read '0' is performed the read discharge flow via read path and M9 to BL, so BL is somewhat charged. During next write '1' BL is driven to '1' from middle-level voltage using write driver. This decrease the power and this can only be done after read '0'.

VII. SIMULATION RESULT

A. SRAM WRITE OPERATION

1) 6T SRAM & 8T SRAM



2) SRAM 10T

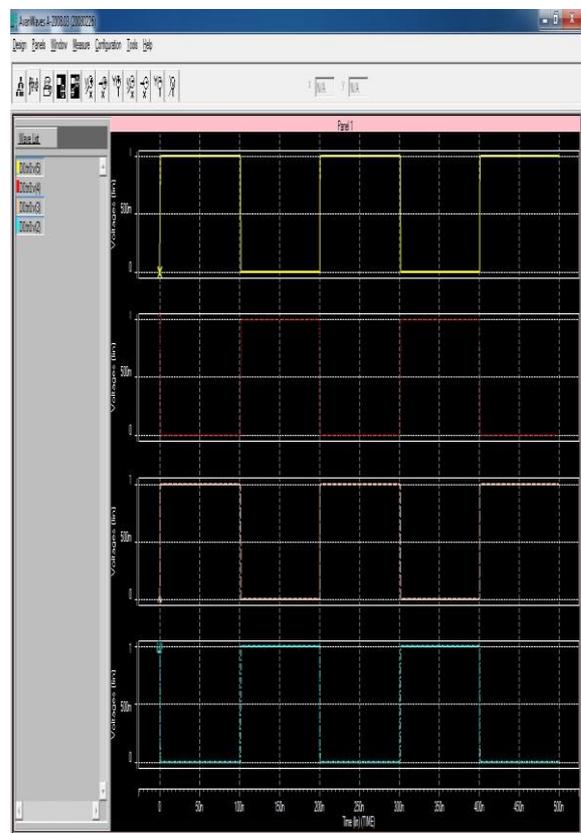


Fig. 9. SRAM 10T FinFET (Write)

B. SRAM READ OPERATION

1) SRAM 6T

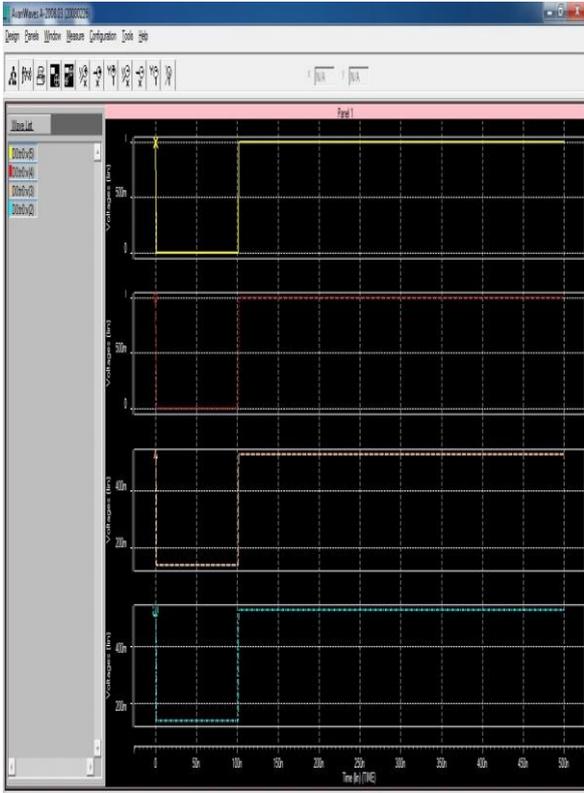


Fig. 10. SRAM 6T FinFET (Read)

B. SRAM 10T

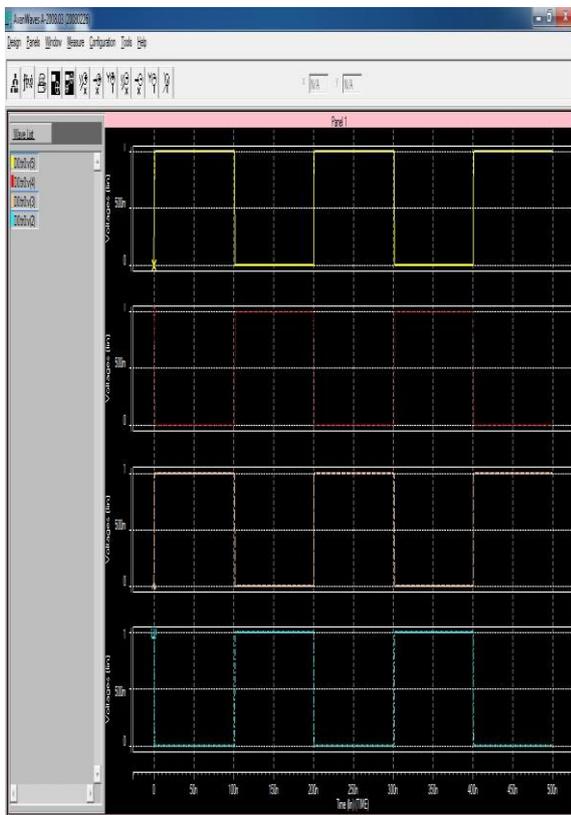


Fig. 11. SRAM 10T FinFET (Read)

C. AVERAGE POWER & DELAY CALCULATIONS

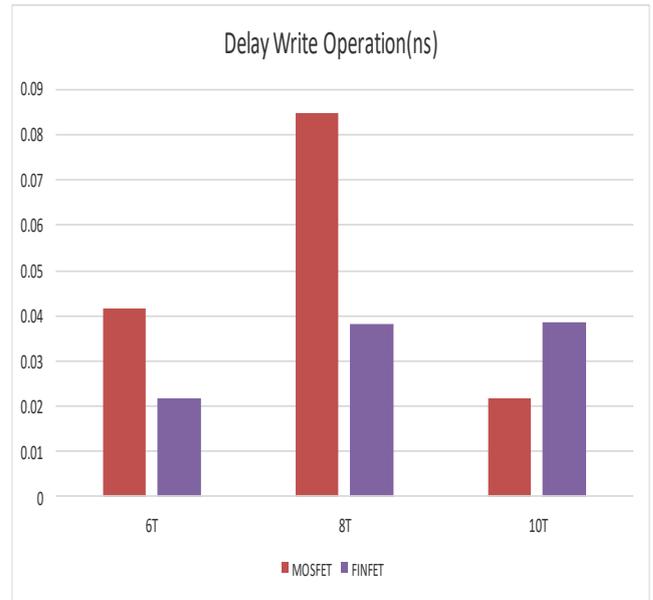


Fig. 12. Average power comparison in write mode

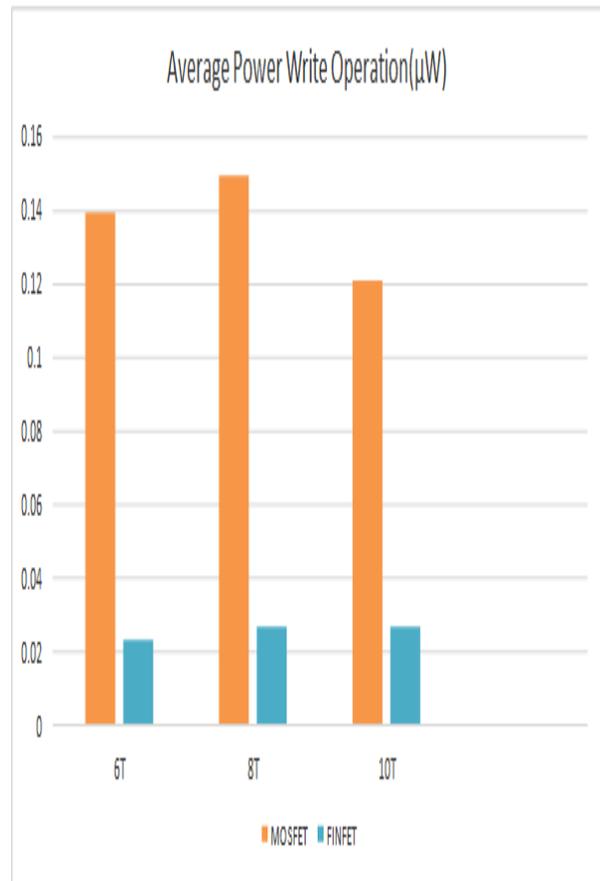


Fig. 13. Delay comparison in write mode

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Table- I: Write Mode

SRAM CELL	TRANSISTOR TYPE	POWER (μ W)	DELAY (ns)	PDP (μ W x ns)	% POWER IMPROVED
6T	MOSFET	0.139	0.0417	0.00580	83.058
	FINFET	0.0236	0.0219	0.000516	
8T	MOSFET	0.1498	0.0849	0.012718	82.109
	FINFET	0.0268	0.0383	0.001026	
10T	MOSFET	0.1214	0.0216	0.002613	77.792
	FINFET	0.02696	0.0385	0.001037	

Table- II: Read Mode

SRAM CELL	TRANSISTOR TYPE	POWER (μ W)	DELAY (ns)	PDP (μ W x ns)	% POWER IMPROVED
6T	MOSFET	23.5	0.097	2.279	21.744
	FINFET	18.39	0.1344	2.471	
8T	MOSFET	34.48	0.0776	2.675	46.664
	FINFET	18.39	0.1049	1.929	
10T	MOSFET	27.91	7.816	218.144	34.109
	FINFET	18.39	0.1417	2.605	

VIII. CONCLUSION

Simulation of 6T, 8T, and 10T SRAM memory cell has been performed in TANER EDA Tool. In simulation work, operations were analyzed through waveforms and output files obtained. FinFET is a promising substitute for MOSFET below 32nm technology. By using FinFET, the average power consumption is decreased, and FinFET offers better control of gate and very less short channel effects due to which average power is improved. The experimental results obtained by simulation shows that write power is improved by 83.058%, 82.109% and 77.792% for 6-Transistor, 8-Transistor and 10-Transistor SRAM cell respectively in FinFET technology as compared to MOSFET technology. For Read operation, there is an improvement in delay for constant average power using FINFET technology.

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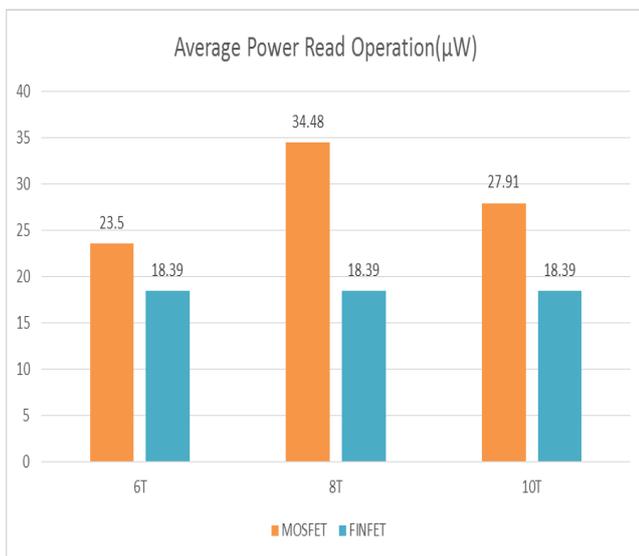


Fig. 14. Average power comparison in read mode

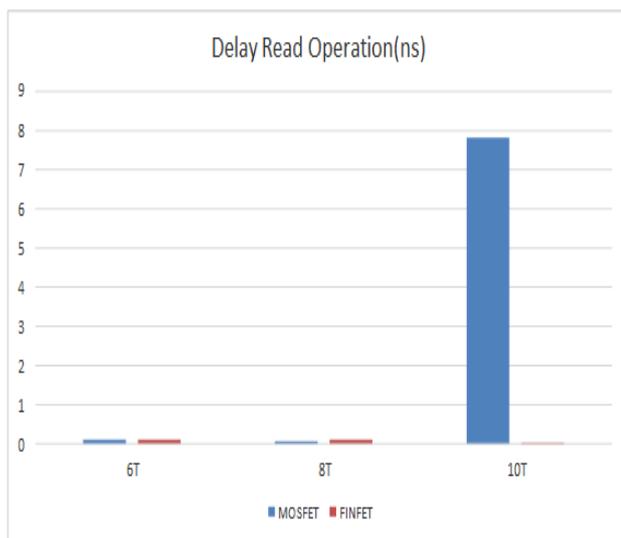


Fig. 15. Delay comparison in read mode

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