Multiport DC-DC Boost Converter for Utilization in PV System with Improved Gain

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Abstract*: Consumption of energy is progressively rising at a regular rate. To accommodate the demand for electric supply with the exhaustion of typical resources like fossil fuels, renewable energy sources like solar power, wind farms and fuel cells are preferred. DC-DC multilevel converters with high gain appear a crucial segment of the renewable energy system. When compared with common topologies the multilevel DC – DC converter has low harmonic distortion, less stress in voltage, minimum EMI noise, and a raised efficiency. To use photovoltaic (PV) systems for standalone applications or micro grid applications, the low output voltage should be boosted to a certain level, i.e a 400V micro grid will be fed with a boost converter having 20V input voltage and gain of 20 to have 400 V at its output.

***Keywords:* multilevel converters, multiport high gain, boost converter, microgrid**

I. INTRODUCTION

The energy consumption is steadily expanding on a daily basis. Since the natural energy resources like fossil fuels exhaust rapidly, renewable energy sources such as solar power, fuel cells and wind farms turn into prominent energy suppliers, to meet the demand for electric supply [1]. High gain DC–DC multilevel converters form an important component of the renewable energy system. When compared with common topologies, the multilevel DC – DC converter has low harmonic distortion, less stress in voltage, minimum EMI noise, and a raised efficiency. To use PV systems in standalone applications or micro grid applications, the low output voltage should be boosted to a higher level [2]. A high gain multiport DC-DC boost converter is suggested in this paper, to draw continuous current from a pair of multiple sources or from a single source using interleaved topology. The voltage measured at the output of the renewable energy sources like solar photovoltaic panels or fuel cells is very low. For example : Output voltage of single photovoltaic cell is 0.5 Volt which is very low so in order to have good output voltage of 10 to 12 Volt PV panel, we require at least 36 solar PV cells that will produce around 17 Volts peak output voltage. Design for the control fed dual active bridge converter, (CF-DAB) enforced on PV systems, and various other applications having a wide variation in input voltage [3]. A photovoltaic system with resonant switched capacitor converters and also dual phase-shift full bridge converter is suggested [4]. The suggested system can be in reliable action both in grid-connected mode and islanding mode. The switching mode depends on output bus voltage which is found to be adequate. A resonant topology of the Isolated DC-DC converter whose applications are in on-board charger for plug-in hybrid electrical vehicles is discussed to achieve the zero voltage switching (ZVS) for switches at the lower leg of the converter with the assistance of resonant circuit. The resonant inductor accommodated in the circuit lessens the power losses. In addition the leakage inductance of the transformer helps in accomplishing zero current switching (ZCS) [5].

So, in order to have the voltage level high for any practical application high gain DC-DC converters are required. In the proposed topology of multilevel boost converter two switches, two inductors and four stage voltage multiplier stages are implemented. In micro grid applications the proposed converter is used as DC link. By using this proposed topology high gain, continuous input current and high conversion ratio are achieved. The continuous input current helps the converter to achieve the gain of 20. The converter which is proposed is simulated using PSIM software and also the hardware prototype is realized to validate the analytical results. A novel Double-Duty-Triple-Mode (DDTM) converter arrangement which is transformer-less and having extensive duty ratio range is proposed with high voltage gain for DC micro grid application [6]. Reviews on the layout and assessment of different DC-DC converter arrangements for Battery Electric Vehicles (BEVs) and Plug-in Hybrid Electric Vehicles (PHEVs) are well presented [7]. A non-confined soft-switching bidirectional DC-DC converter for interfacing the facility to store energy in DC micro grid engaging a half-bridge boost converter at the input port which comes before a LCC resonant tank to aid soft-switching of switches and diodes is suggested [8]. The converter is made to function at high frequency to get lower output voltage ripple, less magnetics and filters [8]. A simple dual-switch boost DC-DC converter topology has been implemented to facilitate voltage matching among the cell stack and power batteries in fuel-cell-poared [9]. Scrutiny of steady state of bipolar switching resonant DC-DC converter is proposed for hybrid electric vehicles [10]. ZVS is accomplished for high side and low side of the converter.

II. CIRCUIT DESCRIPTION

At the input, the diode capacitor multiplier stages are present with two boost stages. The high gain multilevel DC-DC boost converter is motivated by Dickson charge pump [11].

Fig.1 depicts the circuit diagram of the recommended multiport converter. V_{in1} *and* V_{in2} are two input sources.

Revised Manuscript Received on October 15, 2019.

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The converter has four VM stages and the gain of 20 can easily be achieved with the advantage of having continuous input current. Two boost units are implemented in the topology which further ensures the continuous input current to achieve higher gain. The circuit has different modes of operation and it is explained in the next section.

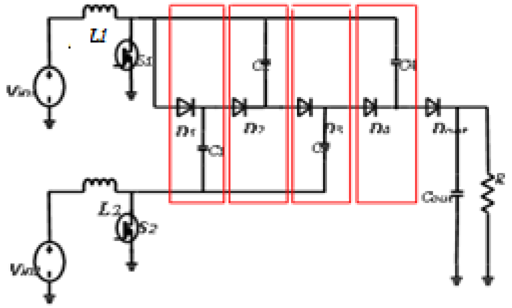

Fig.1 Circuit diagram of the proposed converter

III. OPERATION OF THE CIRCUIT

The objective concerned with the converter is either to attain high gain or high voltage conversion ratio. The gain of the converter confide in the number of VM stages as well as the duty ratio of the switches. In Fig.1 there are four VM stages present in the circuit. The operation of the circuit has three modes. For typical operation of the converter there is a point in time when both the switches will conduct and also one of the switches should conduct at a given instant of time. In Fig. 2 the switching pattern of the switches are shown. There are three modes of operation. These modes of operation differ with respect to the condition of the switch. In the first mode both the switch conducts. The second mode of operation begins when the *S1* is switched OFF and *S2* is switched ON and the third mode of operation begins when *S1* is switched ON and *S2* is switched OFF. The converter can also work with smaller duty ratio and the overlapping time between the switches can also be eliminated but it will lead to lesser gain. The three modes of operation is discussed in details in the next sub-section.

Mode-I: In this mode of operation both switches *S1* and *S2* will be ON and the inductors in both boost units will be charged from their sources *Vin1 and Vin2*. Current in both the inductors surge linearly. Since the diodes present in all the VM stages are reverse biased they stop conducting. The voltage in the VM capacitor remains consistent. The diode at the output *Dout* is reverse biased. Load in this mode of operation is served by the output capacitor *Cout*. Fig.3 shows the operation in mode-I.

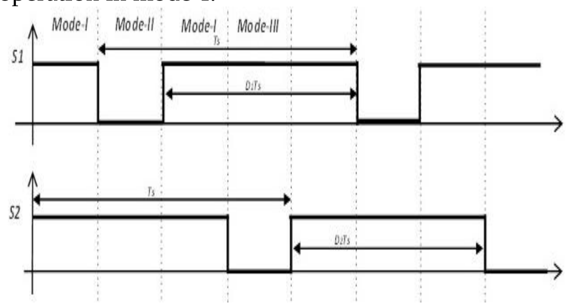

Fig. 2. Switching pattern of the converter

Mode-II: In this mode of operation, the switch *S1* is kept in OFF position and *S2* is kept in ON position. The diodes which are odd numbered are biased forward and the current through inductor is through the VM capacitors charging the odd number of capacitors (*C1, C3,..*) while the even numbered capacitors (*C2, C4,..*) starts discharging. The output diode *Dout* charges the capacitor *Cout* at the output which supplies the load. The Fig.4 shows the operation of the converter in mode-II.

Mode-III: Switch *S1* is switched ON and *S2* is kept OFF in this mode. In this case, the diodes which are even numbered are biased forward while the current through the inductor flows along the VM capacitors and at the same time odd number capacitor gets discharged. The output capacitor supplies the load and the diode at the output Dout *is* biased reverse and. Fig.5 shows the operation in this mode.

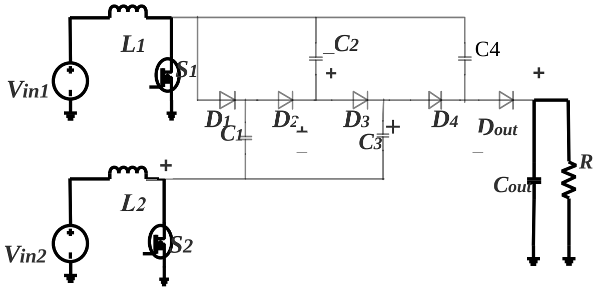

Fig 3. Mode-I Operation of Converter

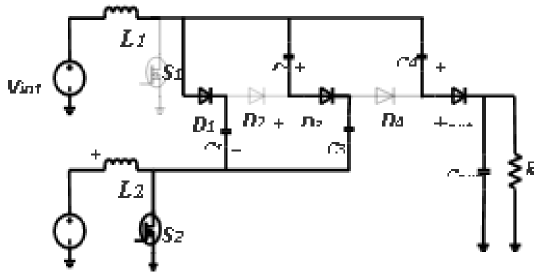

Fig 4. Mode-II Operation of Converter

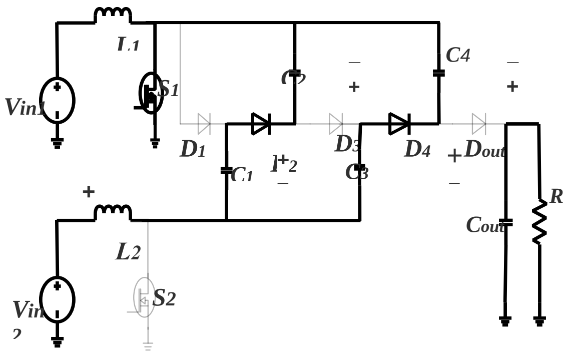

Fig 5. Mode-III Operation of Converter

VI. DESIGN OF MULTILEVEL BOOST CONVERTER

The progressive increment of the charge from capacitors present in the VM stages provides much higher gain as compared to the conventional boost converters [8]. The voltage gain of the proposed converter can be obtained from the volt-sec balance of the converter (Boost Converter).

For inductor L_1, the voltage can be drafted as:

$$V_{L1} = 0 \quad (1)$$

From mode-II of operation, the voltage equations can be derived using the capacitor of upper boost unit. The voltage equation can be written as:

$$V_{C1} = V_{C3} - V_{C2} = V_{out} - V_{C4} = \frac{V_{in1}}{(1-d_1)} \quad (2)$$

here $d1$ is the switching duty cycle of switch S_1. Similarly, from the volt-sec balance of the lower boost converter unit the capacitor voltage can be written as:

$$V_{C2} - V_{C1} = V_{C4} - V_{C3} = \frac{V_{in2}}{(1-d_2)} \quad (3)$$

here $d2$ is the switching duty cycle for the switch *S2*. From the equations (2) and (3), the capacitor voltage of all the stages of the converter can be derived as:

$$V_{C1} = \frac{V_{in1}}{(1-d1)} \quad (4)$$

$$V_{C2} = \frac{V_{in1}}{(1-d1)} + \frac{V_{in2}}{(1-d2)} \quad (5)$$

$$V_{C3} = \frac{2V_{in1}}{(1-d1)} + \frac{V_{in2}}{(1-d2)} \quad (6)$$

$$V_{C4} = \frac{V_{in1}}{(1-d1)} + \frac{2V_{in2}}{(1-d2)} \quad (7)$$

From equation (2), the output voltage can be derived as

$$V_{out} = V_{C4} + \frac{V_{in1}}{(1-d_1)} \quad (8)$$

$$= \frac{3V_{in1}}{(1-d1)} + \frac{2V_{in2}}{(1-d2)} \quad (9)$$

The converter also works in an interleaved manner with single source at the input. The duty ratio of the switches is chosen to be equal (*d1 = d2 = d), then the voltage at the output is as given by

$$V_{out} = (N+1) + \frac{V_{in}}{(1-d)} \quad (10)$$

For inductor, current can be calculated as

$$I_{l1,avg} = \left(\frac{N+1}{2}\right)\frac{I_{out}}{(1-d_1)} \quad (11)$$

$$I_{l2,avg} = \left(\frac{N}{2}\right)\frac{I_{out}}{(1-d_2)} \quad (12)$$

N is the number of VM stages (in this case it is 4). From equation (11) and (12) the average current in the inductor *L1* is larger than the average value of the current in *L2* if the duty ratio of both the switch are equal. The value of the inductor selected by considering the ripple current is given by

$$L1 = \frac{V_{in1}\, d_1}{\Delta I_{L1}\, f_{sw}} \quad (13)$$

$$L2 = \frac{V_{in2}\, d_2}{\Delta I_{L2}\, f_{sw}} \quad (14)$$

MOSFET selection is in the same style as that of normal boost converter. The peak blocking voltage of both the switches is given by

$$V_{s1} = \frac{V_{in1}}{(1-d1)} \quad (15)$$

$$V_{s2} = \frac{V_{in1}}{(1-d2)} \quad (16)$$

The current stress in the switch depends on the count of VM stages. And the average value of the current in both the switches is given by

$$I_{S1,avg} = \left(\frac{(N+2)d_1}{2(1-d_1)} + \frac{N}{2}\right) I_{out} \quad (17)$$

$$I_{S2,avg} = \left(\frac{Nd2}{2(1-d2)} + \frac{N}{2}\right) I_{out} \quad (18)$$

For even number of VM stages the value of the current in the switch *S1* is greater than the current through *S2*. The selection of the diode depends on the capacitor voltages because of the voltage stress created by the capacitor through VM stages. The mode-I (Fig.3) and mode-II (Fig 4) both create the conditions in which alternatively even and odd number diodes are in reverse condition. For normal operating condition the reverse blocking diode voltage is given by

$$V_{Dn} = \frac{V_{in1}}{(1-d_1)} + \frac{V_{in2}}{(1-d_2)} \quad (19)$$

The output diode conduction pattern is different from the VM stage diodes. The diode at the output conducts during mode-II of the operation and its peak blocking voltage is given by

$$V_{Dout} = \frac{V_{in1}}{(1-d_1)} \quad (20)$$

There are two different capacitors present in the circuit the first one is the capacitors *C1,C2,C3,C4* are connected in the VM stages and second is the capacitor present in the output (*Cout*). Since the capacitors present in the VM stages can contribute to the series resistance during continuous charging and discharging, it should be selected in such a way that their equivalent series resistance is low and at the same time the capacitance should be at reasonable levels. It is desirable to choose the VM stage capacitors such that they have low value of ESR to reduce the losses. Fig.6 depicts input voltage, gate pulse, output voltage. Fig.7 shows the voltage stress on the switches. Fig 8 depicts the inductor current waveform. The VM stage capacitors is selected by assuming the ripple voltage and is given by

$$C_n \Delta V_{Cn} = \frac{I_{out}}{f_{sw}}(1-d) \quad (21)$$

The capacitor at the output is based on the charge to be transferred to the output considering the voltage ripple and it is given by

$$C_{out} \Delta V_{out} = \frac{I_{out}}{f_{sw}}(1-d) \quad (22)$$

V. SIMULATION

The simulation of the converter is presented using PSIM software. The simulation results obtained for duty ratio of 0.75 and switching frequency of 100 kHz gives an output voltage of about 400 V and an output current of 1 A. Different waveforms such as input voltage, gate pulses, output voltage, voltage across switch, input current, output current are taken and are shown in Fig.5.

Closed loop operation of the converter is performed using voltage mode controlled type-3 controller. The crossover frequency is 46.2 and phase margin is 57.3. The other parameters of the controller are shown in Table 1.

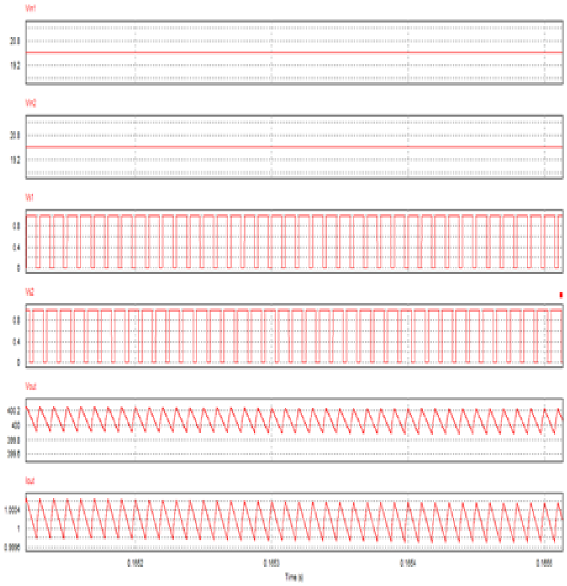

Fig.6 Input Voltage, Gate Pulse, Output Voltage

Fig.7. Gating pulse and voltage Stress across the switches

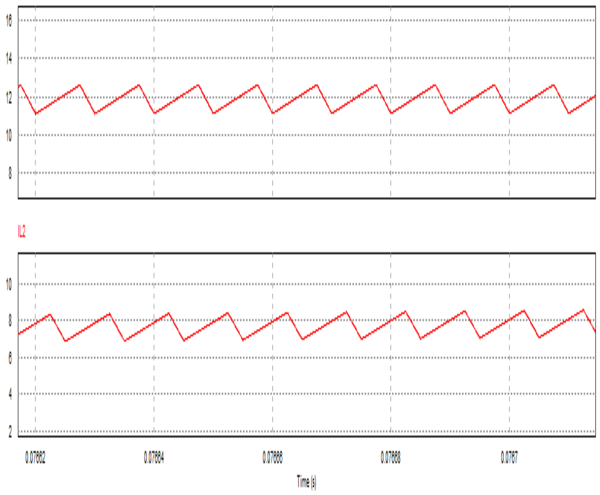

Fig.8. Inductor current waveform

Fig. 9 depicts the closed loop circuit configuration of the converter. The input and output voltage of the closed loop circuit are shown in Fig.10.

Table 1. Parameters for Closed loop operation

Parameter	Value
Switching Frequency(F_{sw})	100kHz
Reference Voltage (V_{ref})	60 V
Gain	10
Resistance (R1)	14.7 Ω
Resistance (R2)	8.2 Ω
Capacitor (C1)	25.9 nF
Capacitor (C2)	76.35 μF
Capacitor (C3)	108.2 μF
Gmod	1

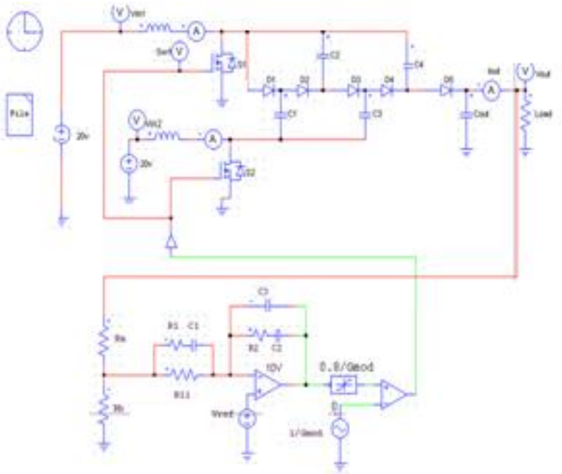

Fig .9 Closed loop configuration of the converter

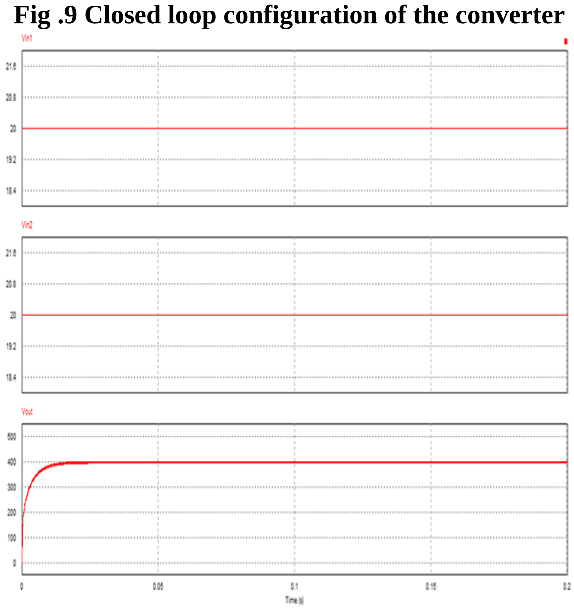

Fig.10. Input and Output Voltage

IV HARDWARE DETAILS

The verification for the simulation results is done by designing hardware model for the converter is shown in Fig.11. Inductor and capacitor used in the circuit are taken according to the value obtained from the design equations. Components used are listed in Table 2.

Table 2. List of components

Component	Rating	Quantity
Inductor [L0451-AL]	180 µF	2
MOSFET [IPA075N15N3G]	150V, 40A	2
Diode [MBR40250T]	250V, 40 A	5
Capacitor (VM Stage)	20uF, 450V	4
Capacitor (C_{out})	22uF, 450V	1
Gate driver	IR2110	2

The hardware model is tested for a low voltage of around 5 V providing an output of 90 V. The supplied input current of 4.77 A and an output current of 0.58 A is obtained. The current through switch *S1* is greater than the switch *S2* which is followed by equation (17) and equation (18). The gain of the experimental prototype is 18 and the efficiency is 69%.

Fig.11 Hardware prototype

The gate pulse to MOSFET for a total period of 180 µs with switching frequency of 100 kHz is shown in Fig.12. PICKIT 3 is used to generate input pulses to the gate driver circuit.

Input voltage and output voltage waveforms taken with DSO from the hardware circuit can be seen in the Fig.13 and Fig.14. The waveforms are taken for input voltage of 5 V and 10 V and an output voltage of 90 V and 205 V is obtained respectively. Fig.15. shows waveforms for an input voltage of 12V and input current of 10.6A, the output voltage obtained is 205V with an output current of 1.90A.

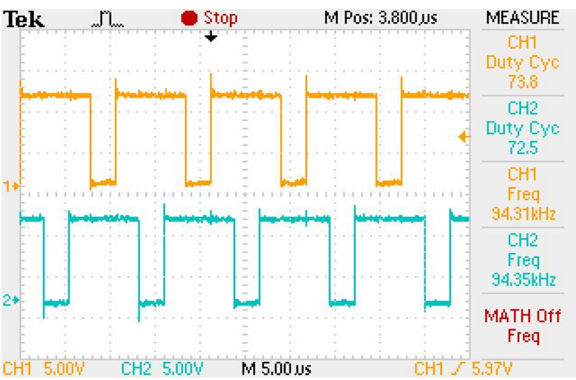

Fig.12.Gate Pulses from Gate Driver Circuit

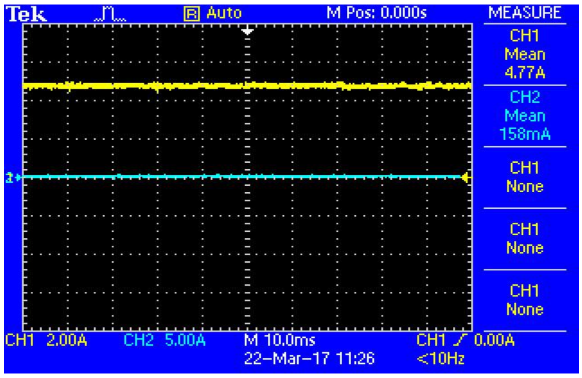

Fig 13. Input current and Output current waveforms

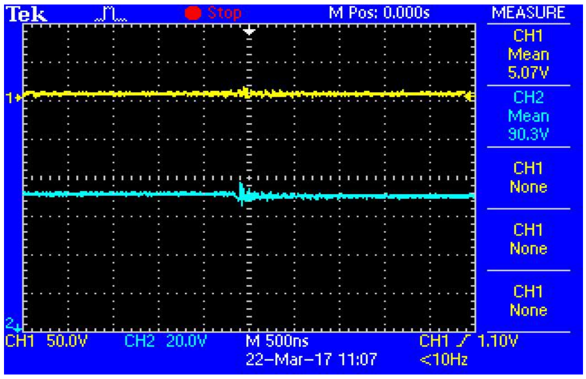

Fig 14. Input Voltage and Output Voltage waveforms

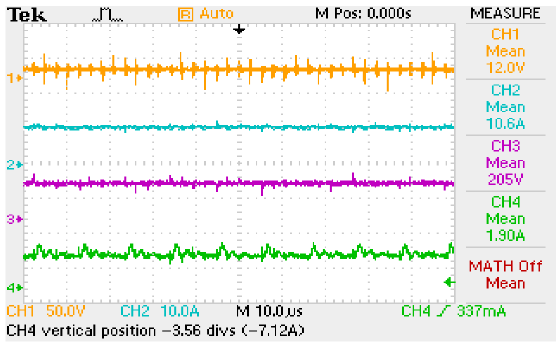

Fig.15. Input Voltage, output voltage and current waveforms.

VII. CONCLUSION

Thus, the topology is studied and given set of specifications is first verified on PSIM Software which provided the simulation results accordingly. Further, the calculated values for inductor and capacitor are used in the process of making hardware design for the topology. So, the hardware design is checked by applying low voltage of 5V for convenience purpose which provided input current of 4.77A and output voltage of 90 V is obtained. A voltage gain of 18 is obtained from the topology which ensures that the topology can be used for high gain applications.

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