Eightdirectional Smart Reconfigurable Router Design for Network on Chip (Noc)

Himani Mittal Gupta, Yogendera Kumar

Abstract: ***Designing N.O.C routers are based on performance parameters like power dissipation , energy , latency[2] .These performance are usually defined during design time.Taking under consideration all parameters as buffer size while designing lead to higher side of power dissipation and higher latency . Large size buffers lead to good performance but at the same time cause excess power dissipation. In this paper our aim is to design a router which supports heterogeneous data .***

Keywords: Network on Chip (NoC); Heterogeneous Reconfigurable Router; Buffer; Latency; Power dissipation; Register Transfer Level (RTL) Design, Low Power, Low Area , Throughput ,Latency ,Critical time path.

I. INTRODUCTION

Network on chip configuration requires a complicated structure by integrating processor cores; memory units to yield excel efficiency and performance. It's the scalable characteristics of NoC that lead to high level error free communication and thus its design part. Today's technology is no doubt are well defined meeting demands but design sophistication makes it difficult to implement in on chip links or interconnections.In this work we proposed a semi buffer or buffer less concept in reconfigurable routers to optimize its area space as well as power dissipation. In our work goal is to provide an NoC router with a certain amount of reconfiguration logic, so that maximum amount of buffer space can be utilized. The principle is that each input channel can lend/borrow buffer units to/from neighboring channels in order to obtain a determined bandwidth.

II. LITERATURE REVIEW

Discuss that power, area, and performance of the NoC architecture are tightly integrated with the design and optimization of the link, router (buffer and crossbar), and topology. Recent work has shown that adaptive channel buffers (on-link storage) can considerably reduce power consumption and area overhead by reducing or replacing the power-hungry router buffers [2].

It discusses the drawbacks of buffers and hence introduce buffer less [4] Network-on-Chip. The major component of a Network-on-Chip architecture is the router, which affects the data transmission latency, chip area and power consumption. Inside the router, buffers occupy a significant amount of power and a large partition of chip area. Therefore buffer less NoC, which discards the buffers in the routers, has been proposed for solving the power and area problem.

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[3]discussed latest XY algorithm for implementing reconfigurable routers on NoC. To prevent deadlock and collisions this method is fast way for communication in NoC.

III. DIFFERENCES BETWEEN PROPOSED AND ORIGINAL RECONFIGURABLE ROUTER :

1. In proposed architecture four more directions(North East, North West, South East, South West) are included thus leading to multidirectional.
2. Data of newly added directions share fifo from their neighbor to store its data.
3. Data from one direction can now be route to seven direction in comparison of previous one in which data from one direction can be routed to three direction only.
4. The Newly designed architecture provides more route to router to route the data thus can be helpful in decreasing critical path length of an design and help in increasing the speed of IC.
5. Now with this newly designed architecture , we can also follow rectilinear stennier tree path to shorten the data path to router.

IV. NEW FEATURES ADDED IN INNOVATIVE RECONFIGURABLE ROUTER :

- We have implemented the control circuit by including features like acknowledge for writing ,acknowledge for reading, request and grant signals for writing in another channel's FIFO.
- We have maintained a counter to indicate the number of memory locations that are currently being used. When the count value becomes zero we say that the FIFO is empty and when the count value becomes equal to the total locations available in the memory the FIFO becomes full.
- Use of tag bits for indicating the direction of output from the crossbar. In an 8 bit packet ,the first two bits are used to indicate the address of the next router on the NOC.

V. PROPOSED WORK

In the proposed router Fig.1, the four diagonal paths are added NE , NW , SE , SW . In an 8 bit packet ,the first two bits are used to indicate the address of the next router on the NOC. Four new directions added support buffer less storage which leads to improvement in performance .In this work, designing the block diagram as shown in Fig. 1. is the first step taken. Designing the block took ideology from the previous versions of homogeneous routers that had all the resources allocated at static time and those couldn't be altered at the design run time which posed problem of longer bit data rejection when used at different communication channels and hence was ineffective in handling different

versions of flowing data. Then second step was using a Hardware Description Language (Verilog in this project) to help realize the project to be environment ready that is to conceptualize the ideology so that it can be fulfilling for further steps. Thirdly, to be ready for real time industrial environment the HDL file was then made to simulate to obtain the optimum result.

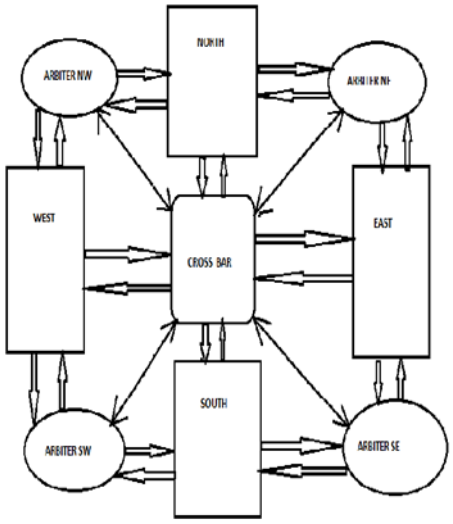

Fig. 1. Proposed Heterogeneous Router Architecture

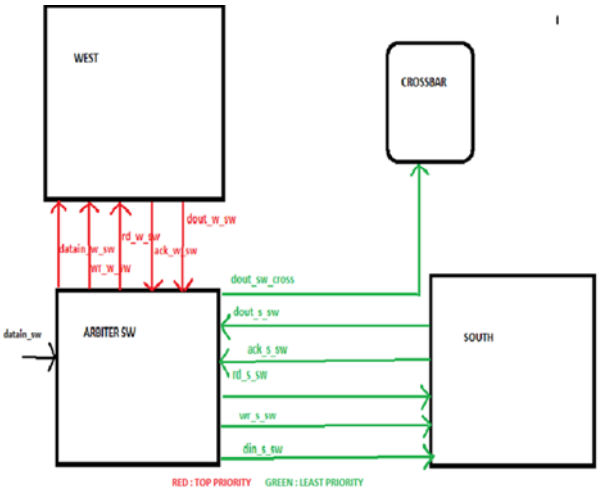

Fig. 2. Detailed Block Diagram of South West Module

Fig.2. shows all detailed connections of South West Module .Similarly we can do for other four modules.

VI. ALGORITHM FOR PROPOSED ROUTER:

1. Data from another router to S, E and W will get store in S, N, E&W channel respectively.
2. In case, when data in any direction exceeds than its F.I.F.O size in its respective channel then it will request its neighboring channels for storing its data in neighbor.
3. As soon as any channel receive sharing request from its neighbor, it will first check whether its F.I.F.O is full or not.

3.a If it is not full & it has received sharing request from both the neighbor then it will give grant to right neighbor on priority basis .

3.b. If it has received sharing request from any one of the neighbor then it will grant to that neighbor.

3.c If F.I.F.O of the respective channel is full then it will grant to any neighbor.

4. As soon as the requesting channel receive grant from one of its neighboring channel , then it will pass its data to neighboring channel (left channel on priority) with write signal..

VII. BUFFER SELECTION:

Table 1: Buffer Selection

Position of Arbiter	Buffer Select
Bottom_right	Right
Bottom_left	Left
Top_left	Right
Top_right	Left

Table 1 shows which buffer is selected depending on the position of arbiter. If Bottom_right arbiter is selected then right buffer is selected . Similarly left buffer is selected if the position of arbiter is Bottom_left. Similarly right and left buffer is selected with arbiter position as Top_left and Top_right.

VIII. FLOWCHART & CHANNEL INTAKE:

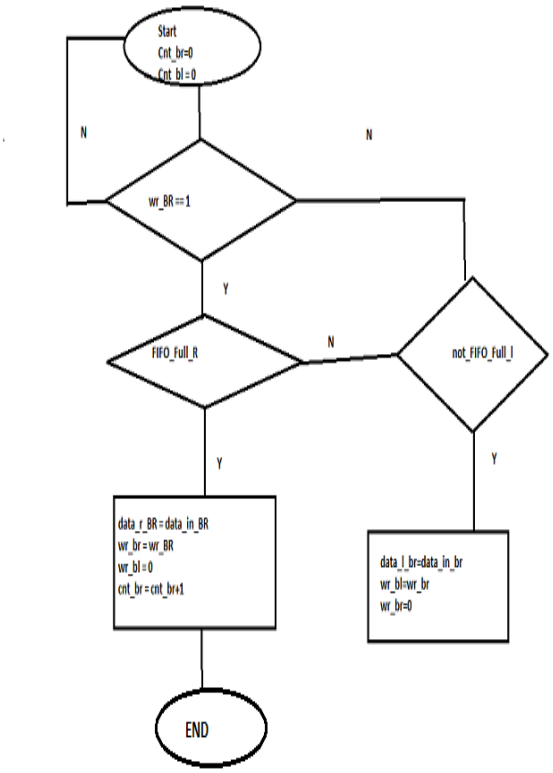

Fig.3 Flowchart for Bottom Right writing.

Fig.3. shows the flowchart for communication in Bottom right module SE. Similarly communication can be done in other thress modules SW , NE and NW .

IX. RESULTS:

A. SIMULATIONS :

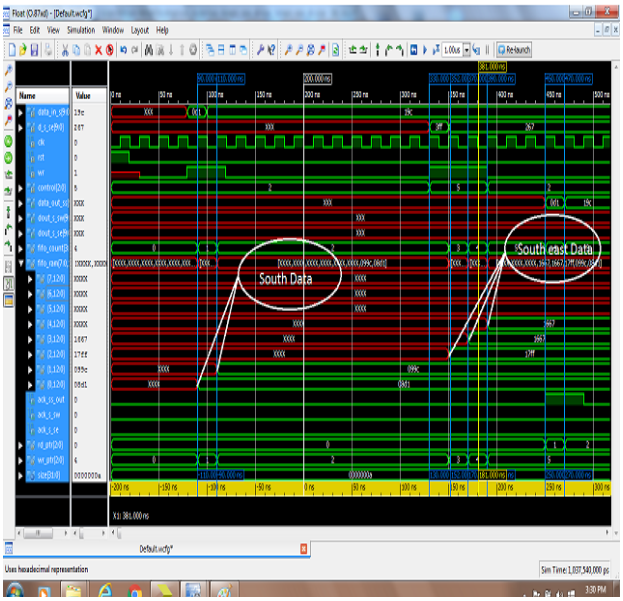

Fig.4. Simulation of Proposed Router.

Fig.4. shows that South data can be read twice supporting heterogeneous property of our innovative reconfigurable router.

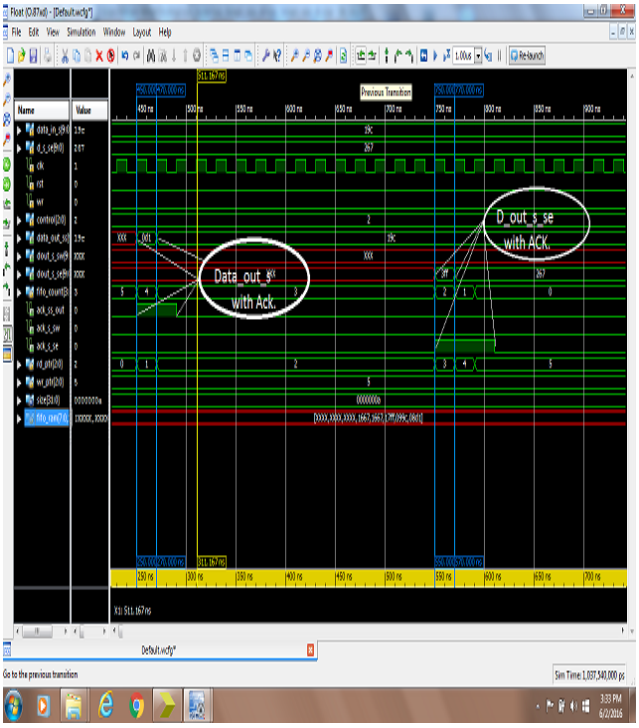

Fig.5.South channel output new direction.

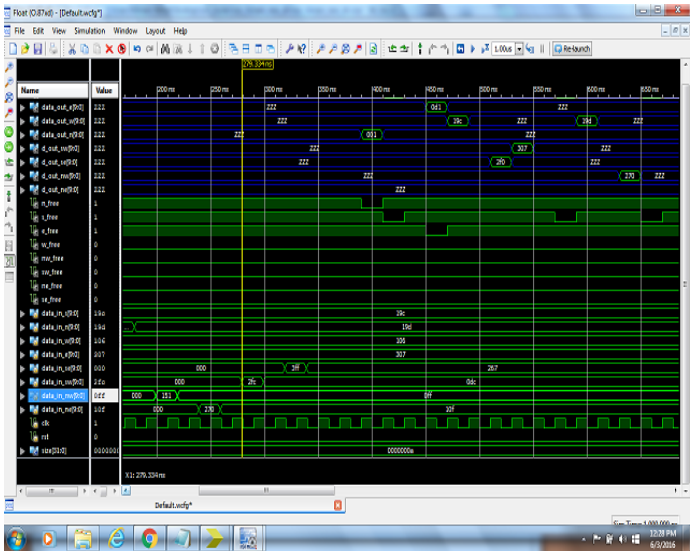

Fig.6.Top Router New Direction

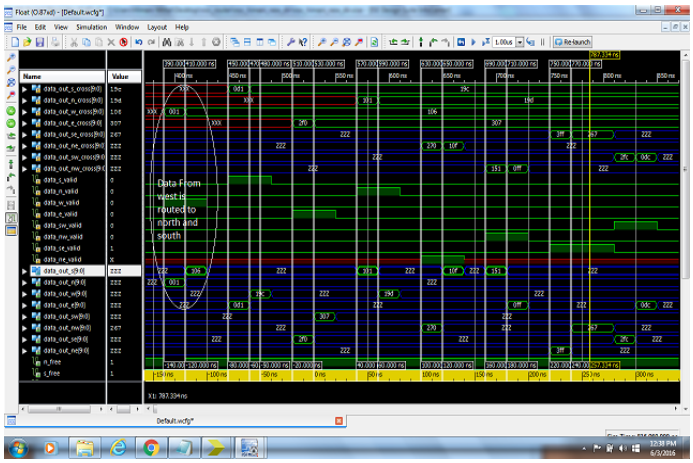

Fig.7. Crossbar New Direction

B. SYNTHESIS :

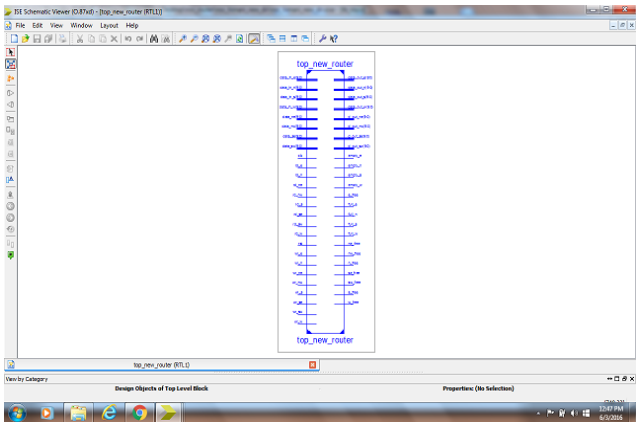

Fig.8. Top level schematic of new direction

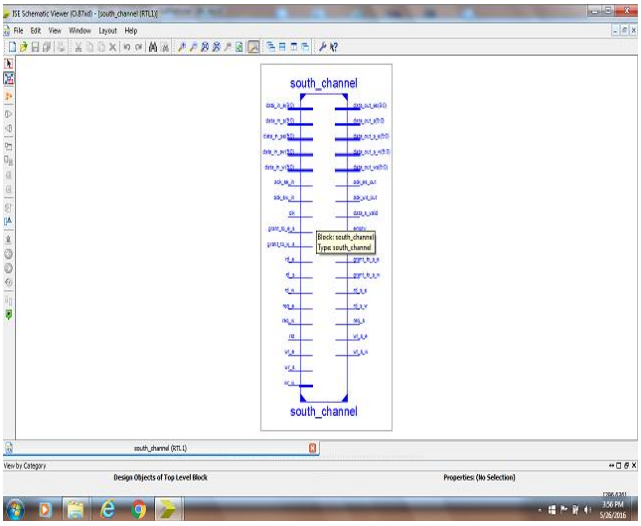

Fig.9.South channel schematic

C.DESIGN UTILIZATION SUMMARY:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	549	30064	1%
Number of Slice LUTs	1198	15032	7%
Number of fully used LUT-FF pairs	343	1404	24%
Number of bonded IOBs	194	226	85%
Number of BUFG/BUFGCTRLs	1	16	6%

Fig. 10. Design Utilization summary .

Fig.10. shows the device utilization summary of proposed router in terms of number slice registers , LUT'S , bonded IOB's .*D. POWER ANALYSIS BY XILINX POWER ANALYZER TOOL (XPA).*

Total power for our proposed heterogeneous reconfigurable router is 45mW as shown in Fig.11which is bit more because of addition of four more directions but its critical time path is drastically reduced along with delay of 7.1ns which in turn leads to more speed at a increased frequency of 140Mhz as compared to 100 MHz. in original reconfigurable routers[8] . Hence power is reduced by 5mW in our proposed architecture.

X. CONCLUSION

The new router, while reaching better performance than the original architecture, can obtain a slight increase in power consumption though it gives more switching speed [5] , less critical time path , high frequency[6] hence high throughput . In addition now data can be routed to right directions unlike only four directions in the previous version. Because of more routing possible it provides more route to router to route the data thus can be helpful in decreasing critical path length of an design and help in increasing the speed of IC .Also with this newly designed architecture , we can also follow rectilinear stennier tree path to shorten the data path to router.

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