2D And 3D Based Network On Chip For A Stream Of Data using Label Switching Technique

Mamatha N, Sridevi S, G Indumathi, K Venkateswaran

Abstract: *Universal interconnection networks are prime performance tailback for high performance SoCs (Systems-on-Chip). Since shrinking the size of the ICs (Integrated Circuits) is the main aim, NoC (Network-on-Chip), being a segmental and mountable design tactic is a propitious substitute to outmoded bus-mode architectures. NoC combined with 3D-Routers and label switching technique can guarantee low power consumption, QoS along with less latency. In the proposed work, 3D NoCs are proven to be more advantageous by achieving 39.9% reduction in Area, 1.7% reduction in Power Consumption, and 11.3% reduction in Memory usage.*

Keywords: 2-D NoC, 3D-NoC, XILINX ISE, Data stream, Label Switching, Label Switched-NoC.

I. INTRODUCTION

As stated by Moore's law the number of transistors incorporated onto an integrated circuit is coarsely doubled every eighteen months due to reduction in the transistor sizes. As the number of cores rises, bandwidth tailback issue arises and achieving the communication is a critical task when multi-core designs. NoCs are segmental and mountable design strategy is a promising substitute to outmoded bus-mode architectures. NoCs can provide a mountable solution to the paradigm shift problem between communication and computation entities [1].

Communication link, router and network interface/adapter together forms a NoC, Links provide physical interconnection between the nodes in the network, routers generally implement the logic of communication protocol, and Network adapter (NA) provides the logic assembly between Network and Intellectual Property (IP) cores [2]. Network topologies provide the information about how a network is organized and structured and also how the entities of the network are interconnected, Performance metrics generally considered are throughput, bandwidth and latency. QoS is all about expectedness of behavior of a network and it can be evaluated through quantitative analysis. QoS is the highest when all the

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performance parameters are at its best values [3]. 2-D NoCs are considered as a first priority when it comes to fabrication. Even though 2-D NoCs are highly scalable and flexible, there exist a trade-off between system design cost and the system complexity. Also increased number of nodes, wires, hardware implementations (to assure hard QoS) results in increased net delays, high latency, which in turn elevates area overhead and power consumption. 3-D NoCs are introduced as a solution. These reduce the number of universal interconnections; it also aims at reducing the length of the interconnect nets [4]. As time proceeds the Network design ages, the performance of the network degrades. As it depends on durability and reliability of the design. Resistance to heat and temperature diminishes as the design gets older, 3-D NoCs are proven to be extra tough than 2-D NoCs when it comes to aging [5].

II. II.LITERATURE SURVEY

Manoj Singh Gaur has proposed "Network-on-chip: Current Issues and Challenges." Explains Moore's law, which states that the compactness of an integrated chip doubles each year as the size of the transistor is reducing day by day. Dur to this there exist a patterned shift from designs that concentrate on computation alone as well as designs that concentrate on communication aspects as well. Also, when the network topologies are considered, a trade-off between computation/communication speed and its cost exist [1].

Cota E, de morais armory and Soares lubaszewski M, has proposed in "reliability, availability, serviceability of Networks-on-chip" about the design platform of the planar Network-on-Chips, main building entities of an NoC. NoCs tactical display place is pointedly larger when related to a bus-based outcome. NoCs integrates a distinctive idleness which assistances in tackling the gridlocks of defects, tasks involved communication. This verdure the network designer a design platform in which suitable results to system constraints, features and requirements can be found out [2].

Konsantinos Tatas, Kostas Sizios, DimitrosSodris and Axel Jantsch, has proposed in "Designing 2D and 3D Network on- Chip Architectures" about the network topologies. Upon various available topologies determining one topology which is effectual and pledges superior performance depends on nature of conclusion, cost requirements. Quality of Service is the certainty that the communication among any two nods is successful.

In order to achieve high QoS, performance parameters such as throughput, latency and bandwidth are to be monitored and optimized so that its values are at its highest [3].

Basavaraj Talwar and Bharadwaj Amrutur has explained in "Traffic engineered NoC for streaming applications", that current NoCs aim at good QoS and performance metrics. Packet switching techniques makes use of Importance based scheme to ensure bandwidth and latency performance parameters. But these priority-based schemes work accurate only when the tasks have active priorities going on. Circuit switching techniques makes use of resource allocation schemes to ensure QoS constraints. Since in circuit switching the connection has to be made prior to communication, it is hard to add new components to the circuit during communication i.e. scalability is deprived, the connection utilization is also poor. Circuit switching uses handshaking signals to achieve the communication between two nodes. Label switching makes use of a unified NoC administrator in order to retain the advantages of both circuit and packet switching. Label-Switched NoC administrator provides path latency that can be regulatable, and meets the required performance metric constraints. LS NoC manager also makes use of contention-free paths/pipes which guarantees both QoS and Performance Constraints [6].

III. COMMUNICATION ARCHITECTURE

A. *Comparing the Switching Techniques:*

When a Network of routers having a set of input channels and a set of output channels is considered, switching is used to transfer the stream of data packets from one router to other.

In case of circuit switching a connection has to be setup between source and the destination to achieve the communication. i.e., it is connection-oriented. Pros include data flow with very less or no delay, also provides design reuse. Cons include more bandwidth requirement, more connection establishment time, inability to transfer the data even when the connection link is free, insufficient circuit utilization, poor scalability. In case of streaming application Circuit Switched-NoC implements resource reservation mechanism to guarantee QOS [6].

In packet switching data stream is broken up into packets, every packet will be containing a header which in turn consists of destination address and route information. Provides high throughput, high interconnect utilization. Cons include high Transmission delay. packets might arrive in wrong order, high memory required. In case of streaming application Packet Switched-NoC implements priority-based mechanism to guarantee latency and bandwidth constraints [6].

Making use of label switching can guarantee hard bandwidth and throughput necessities for data streaming claims. Pros include single cycle traversal delay during contention-less traffic, Broadcast and multicast capable, can enable circuit switching without the need of a globally synchronous clock leads to reduction in power [6]. Label switching also considerably reduces the area overhead and complexity of communication between the routers, labels can

be chosen at each node based on the desired destination node label switching can integrally back traffic issues.

B. *Comparing the Switching Techniques:*

In this work a central NoC Controller is made use. It recognizes congestion free, resource rich paths to assure hard performance metrics. Also, the NoC Controller exploits algorithms under flow identification category in order to identify contention-free, high bandwidth paths. The state of label-switched NoC is transparent to Label Switched-NoC Controller.

Fig 1 shows 2-dimensional view of a network that has 3*3 routers. The network controller is placed at the node 1. Also, a brief insight of a single node is shown. Each node consists of a label switched router and a processing element (can be either a memory element or a processor or any module). It is not mandatory that all processing elements are same, it can be customized according to requirements of the designer.
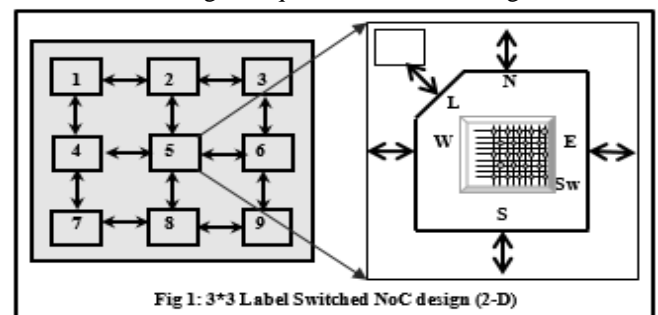

Fig 1: 3*3 Label Switched NoC design (2-D)

Similarly, a 3*3 label switched 3-Dimensional NoC can be designed as shown in figure Fig 2. Lines shown in between the nodes are nothing but pipes.
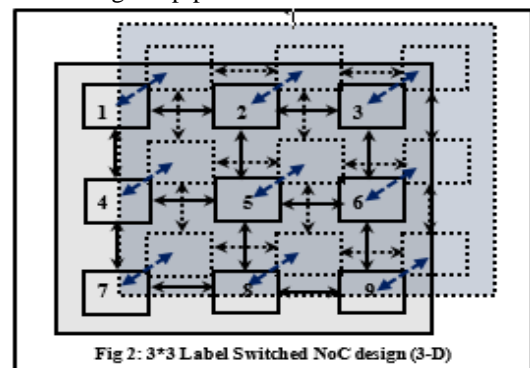

Fig 2: 3*3 Label Switched NoC design (3-D)

The functional insight of a particular node is same as shown in fig 1 but there exist two more ports in addition in order to achieve the communication between the top and bottom layers.

Fig 2.2 shows the in what detections the routers in the network are interconnected. Having a close look at the planar network considered in figure 2.2, we conclude that there are 12 ports that are externally connected out of which 6 are input ports and 6 are output ports. So, the random data generated can be given as an input to any one of the 6 input ports.

For instance, Consider north port of node 1 as source and east port of node 9 as sink node. There are total 6 possible paths to transfer the data from source to sink, they are 1-2-3-6-9, 1-4-7-8-9, 1-2-5-8-9, 1-4-5-6-9, 1-4-5-6-9, 1-4-5-6-9. Out of which one path has to be chosen to provide least path weight.
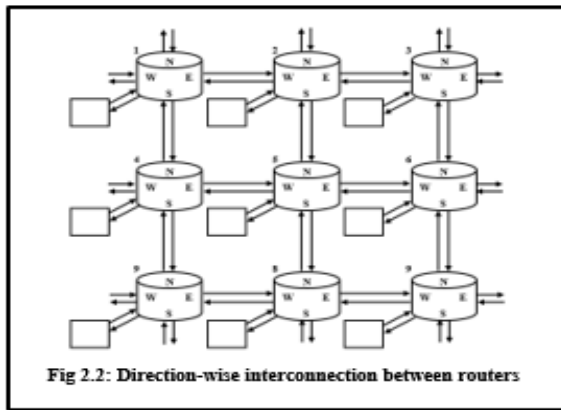
Fig 2.2: Direction-wise interconnection between routers

C. Router for label Switched NoCs:

Figure 3 shows the design for communication between input port to output port in a single router. A pseudo random generator is used to generate a stream of data. In this work an 8-bit Linear Feedback Shift Register (LFSR) is made use. The data generated by LFSR is given to the input port of the router as an input.

Main components included in input port are input register, FIFO buffer, 2*1 mux, routing table and FIFO control block.

Role of the input register is to concatenate the data and label; label is an identifier which indicates which output port is to be chosen. As shown in fig 3, valid signal acts as reset. valid at the output of register goes high only when there is a valid output data.

FIFO is used to store the data streams to prevent loss of information in case of traffic. Control block checks the status of FIFO and produces a signal that acts as a select line to the mux.

Steps included to decide the next node are given as

STEP 1: Define the data, Path weights and Node values.
STEP 2: De-concatenate the data from multiplexer and separate the data, label values.
STEP 3: Check for the Current Node by Comparing it with label value.
STEP 4: Compare the East and South path weights, choose path with less weight.
STEP 5: Check if any Valid Data is available at North and/or West Input ports.
STEP 6: If data is available and path weight is less, then transfer the data, modify the label_out and Valid_Route_Out values.

Arbiter used in the output port of the router acts as a output port allocator.

Principle of arbiter is round robin scheduling. In a case where there are intermediate nodes between source and destination node, arbiter helps to decide the target ID. Based on the valid route selected by the arbiter.

The mux in the output port chooses which input port to choose the data from. The same data is forwarded to the output register de-concatenated there and is available at the main output.

Simulation results of pseudo random data generator, single cycle data transmission, 2-D and 3-D 3*3 NoCs are discussed in the next section.
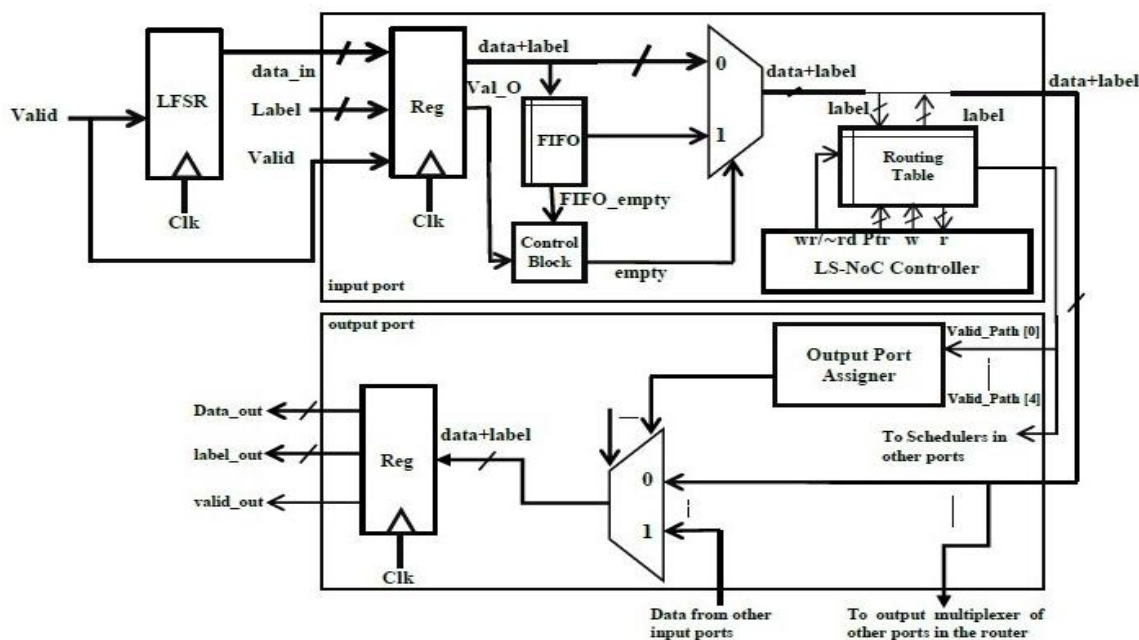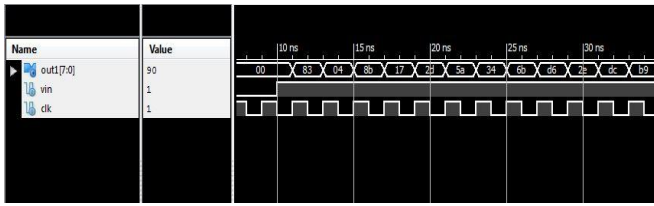

Fig 3: A Label Switched Router (LSR) [6]

If it is empty data from input register is chosen else the data from memory element is chosen and passed on to the output port.

In order to choose which is the next node that has to choose to transmit the data, a routing algorithm (Shortest Path First algorithm) is implemented as a routing table.

IV. SIMULATION RESULTS

A. Simulation of 2-D LSR and LS-NoC:

The random Sequence of data generated by a LFSR is shown in fig 4.0. it uses an active high reset.

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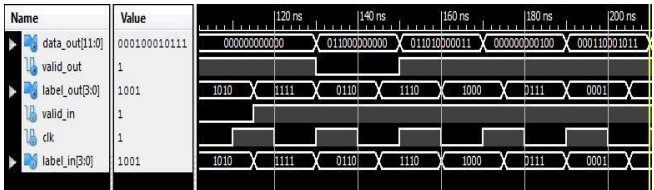*Blue Eyes Intelligence Engineering*
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LFSR used in Fig 3 is constructed for a polynomial equation $x^7 + x + 1$. The logic is that, XOR gate is placed only wherever x term is present, XOR gate is not considered for the terms that are absent in the polynomial equation.

Fig 4.0: Simulated response of LFSR

This data from LFSR is given as input to the label switched router that is discussed.

Fig 4.1: Simulated response of Circuitry between single input-output port of an LSR

Since the design considers single input and output port in the design, the communication between single input-output port is as shown in figure 4.1.

So Far, the simulation of circuitry between a single input port and single output port is considered and simulated. For the further simulation we will be taking all four input and output ports of the router into consideration as shown in fig 2.1.

It is reported to have 10μsec of time to transmit a data packet from an input port to the output port and is shown in fig 4.3. analyzing the output waveform shown in Fig 4.3 the active reset goes low at 24 μsec, and the moment reset goes low the input data is taken into consideration by the design. And the output ports display this data at 34 μsec.

Latency is calculated using an equation mentioned in Eq (4.1)

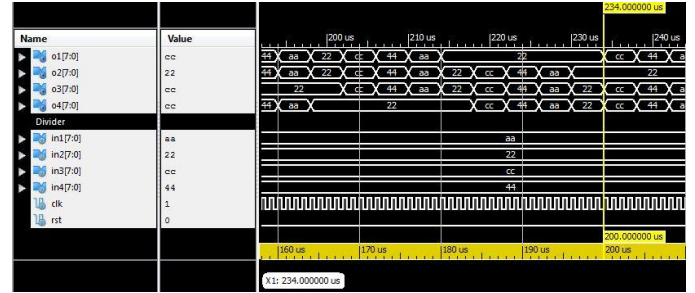Latency=Data available Time - Data Introduction Time ..(4.1)

Substituting the values discussed in equation 4.1

Latency = 34 μsec- 24 μsec = 10 μsec

Fig 4.2: Latency in Single LSR (2-D).

In the same way, Fig 4.3 shows the simulation of a single LSR when the data is given at all the input ports.

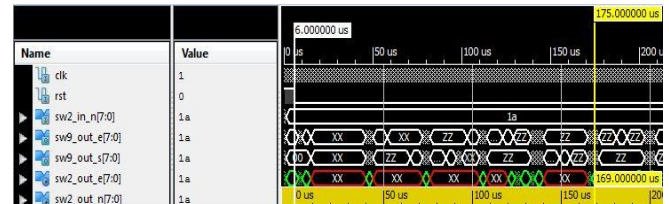**Fig 4.3: Simulation of a Single LSR**

The input data sequence is given to the north port of switch/node 2 (node 2 is Source node) and the output has to be collected at east port of node 9 (node 9 is Sink node). Figure 4.4 shows how the transmission of data packet from switch 2 to switch 9 occurs. The time taken for the data packet to reach east port of switch 9 from north port of switch 2 is 169μsec and is shown in fig 4.5 (and is calculated using equation 4.1 as discussed earlier in this section).

Substituting the values from fig 4.5 in equation 4.1

Reset goes low at 6 μsec and output appears at 175 μsec.

Latency = 175μsec- 6μsec = 169μsec.

Even though the destination considered is east port of node-9, the data appears at the south port of the router at the same time instant.

Fig 4.4 Simulation response of a 2-D NoC

Analysis and Simulation of 2-D label Switched Router and Label Switched NoC are discussed in the section IV (A). Further section IV (b) describes the analysis of 3-D LSR and LS-NoC

B. Simulation of 3-D LSR and 3-D LS-NoC

Considering Fig 2.2, which describes how the interconnections between the LSRs are made and in what directions, the LSR considered in here is a 2-D LSR which has four directional ports and one local port which is connected to a processing element. So, this interconnection represents a 2-D NoC.

In order to construct a 3-D NoC we have to make use of a 3-D router as shown in Fig 2.1, which has a total of seven ports out of which 6 are direction ports and other is a local port which can be connected to a local port.

And hence a top port and a bottom port are considered in the design and simulation of 3-D LSR and LS-NoC Based on the label value one particular output port is chosen and the data is transmitted.

It is reported to have 17μsec is required to transmit a data packet from an input port to the output port of the router and is shown in fig 4.5.

Substituting the values from fig 4.5 in equation 4.1

Reset goes low at 5 μsec and output appears at 22 μsec.

Latency = 22μsec- 5μsec = 17μsec.

Fig 4.5 shows the minimum possible latency of a 3-D LSR, other possible values are tabulated in Table I: Different possible Latencies in 3-D LSR.

Table 4.1 is calculated by analyzing and referring to the

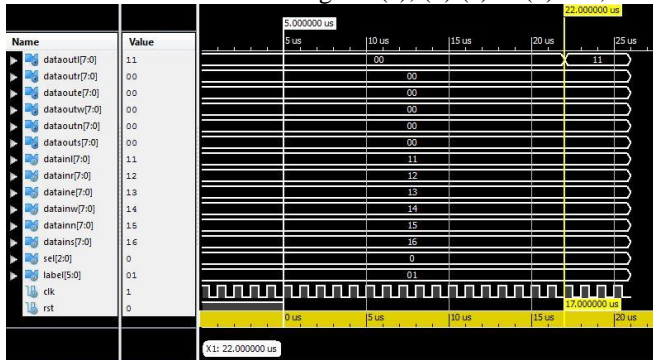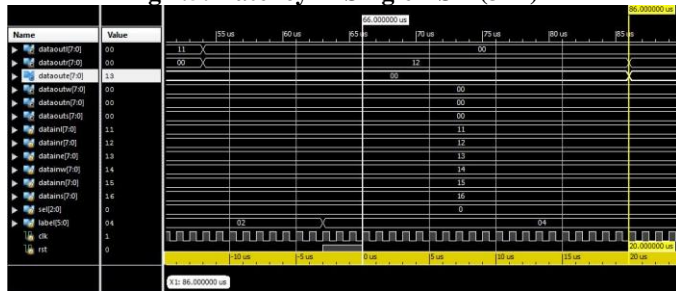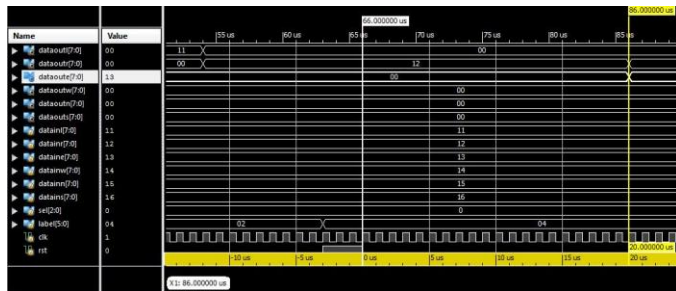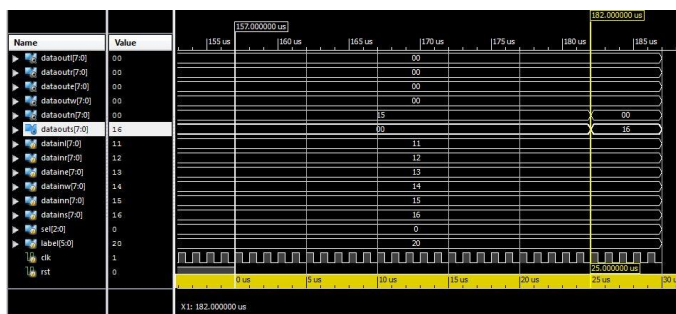simulation results shown in fig 4.6 (a), (b) (c) & (d) etc.,

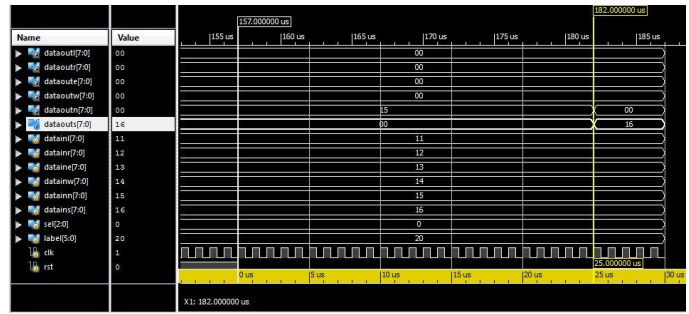**Fig 4.5: Latency in Single LSR (3-D)**

(a)

(b)

(c)

(d)

(c)

Fig 4.6: Different possible Latencies in 3-D LSR.

TABLE I
DIFFERENT POSSIBLE LATENCIES IN 3-D LSR.

Fig Number	Latency Value
4.7 (a)	24 µsec
4.7 (b)	20 µsec
4.7 (c)	23 µsec
4.7 (d)	25 µsec
4.7 (e)	21 µsec

Fig 4.7 shows the simulation response of 3-D NoC when the same example is taken into account. i.e. North port of node 2 as source node and east port of node 9 as destination node. It is reported to have a latency of 58µsec to reach the destination from source.

Fig 4.7: Simulation response of a 3-D NoC

C. Evaluation of Performance metrics:

Throughput can be calculated using the formula mentioned in Equation 4.2.

$$Throughput = \frac{(Operating\ Frequency) * data\ size}{Latency}$$

(4.2)

Where Operating Frequency = 1MHz

Data Size = 8 bits

Latency = Respective calculated latencies.

Table II represents the List of few parameters considering 2-D & 3-D LSRs & NoCs

TABLE II
PARAMETER LIST

Design Parameter	LSR-2D	LSR-3D	NoC-2D	NoC-3D
Area (IoBs)	59	85	69	107
Power (mW)	450	459	461	475
Memory (kB)	283.4	250.7	260.8	266.3
Latency (µS)	10	17	46	58
Throughput (Bps)	800G	470.6G	174G	137G

V. CONCLUSION

This work links a 3*3 2-Dimensional NoC and 3-Dimensional NoC in terms of data stream transmission and performance parameters. The NoCs are designed to transmit an 8-bit data along with 4-bit label (for 2D NoC), and 6-bit label (for 3D NoC) using Label Switching Technique.

In order to transmit the data from one node to the next node, Shortest path First Algorithm is implemented which compares the path weights and chooses a path with least path weight.

Considering the performance parameters of 2-D Label Switched Router (LSR) provides area utilization of 12%, whereas 3-D LSR provides area utilization of 22%. When 2-D NoCs are taken into account, a 3*3 LSNoC Provides 14% area utilization, whereas 3-D NoCs provide 17% area utilization. Hence there is a trade-off between area utilization and the number of IOBs used.

3-D LSR shows considerable reduction in area, Power Consumption and Memory Usage. i.e., 39.9% reduction in Area, 1.7% reduction in Power Consumption, and 11.3% reduction in Memory usage.

Since 3-D NoCs are able to achieve Less Latency, low Power Consumption and High throughput, 3-D NoCs are said to have High QoS.

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