Fractional Order Darwinian Particle Swarm Optimization based K-Best Detection Algorithm for Mimo Communication

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ABSTRACT--- This paper describes the hardware implementation prototype for the recent massive Multiple In and Out communication. In the entire MIMO communication system, decoder plays an important role in reducing the complexity of system. The objective is to recast the operating K-best detection methodology by forwarding the backwash wrapped up in organizing the path metrics to enhance aptness for the implementation of hardware with very durable BER performance. A 8x8 MIMO and 64 QAM FODPSO K-Best decoder using Schnorr-Euchner (SE) enumeration and new parameter Rlimit is proposed for reducing the complexity, thereby provides a better performance. The architecture for reducing the BER to 0.3 dB with list size K and Rlimit to 4 is designed for a word length of 16 bits. The proposed architecture is synthesized using XST in 45nm CMOS technology and coded in Verilog for a Maximum frequency of 181.8 MHz, 1090.8 Mbps through and a power consumption of 782mW and latency of 0.044µs.

I. INTRODUCTION

Recent days MIMO provides good reliability and diversity gain by transmitting and receiving signals from all directions due to the presence of multiple antennas at both the ends. MIMO provides highly reliable communication by transmitting more identical information through multiple antennas. Wireless standards, such as IEEE802.11n [1] (10^{-6} maximum BER) , IEEE802.16e provides higher Data rates and reliability with minimum bit error rate (BER) and good quality of service (QoS). MIMO is appreciated for its receiver designed with low-power, low-complexity, high-throughput and high-performance. The purpose of MIMO communication system is to design a receivers. Number of procedures has been proposed to report the problem, offering diverse trade-offs between performance and complexity. Maximum- likelihood (ML) detection is one of the transcendent detection methodology that depreciates the BER through out-and-out exploration, while its complicacy upsurges rampantly with respect to the diverse antennas at the transmitting and receiving end [2,3] compared with zero-forcing (ZF), the minimum mean squared error (MMSE) techniques that has low complexity, high BER and significant performance loss. The other category of receivers is sphere decoder (SD) algorithm which [5], [6] extremely decreases the complexity and high performance for Multiple In and Out detection. The SD procedures have an indefinitely large number of execution approaches, i.e., K-best [7] and K-best Schnorr-Euchner (SE) [8], [9].

The K best Schnorr-Euchner (SE),is complex K-best iterative method with computational complexity and gain using a tunable parameter Rlimit as well list size, K. The SE K-best iterative method bestows 6.9 to 8.0dB improvement through space K-best decoder and 1.4 to 2.5dB better execution compared with K-best complex decoder of 4x4 and 64 QAM with Rlimit varying between 1 to 4 for a 8x8 MIMO. A MATLAB simulation is organized on iterative LR-aided K-best decoder for perpetrating fixed point conversion for reducing the bit length thereby reducing the cost, area and power by optimizing the design of individual sub module of K-best decoder. The simulation results bestows that a BER within limit of 0.3 dB for Multiple In and Out with different intonation is possible only with 16 bit of word length. It is a stochastic optimization method based on population in which PSO has been determined with manual stray solutions (particles). The ultimate desideratum of this technique is to determine the finest solution through an iterative step. In this research paper, a low complexity hardware strategy of iterative complex K-best decoder using Fractional Order Darwinian Particle Swarm Optimization (FODPSO) is portrayed. This proposed work can daze the control path which is diverse from existing K-best detector. The proposed architecture is coded in Verilog and synthesized in 45nm CMOS technology for a 8x8 MIMO and 64 QAM with k and Rlimit as 4. This research paper is prepared as follows. Section 2 describes the FODPSO based MIMO detection method. Section 3 describes the Architecture design for K-best detector. Section 4 exhibits the tabulation of results, and Section 5 concludes the paper.

II. FODPSO BASED MULTIPLE INPUT AND MULTIPLE OUTPUT DETECTION

Consider a Multiple Input and Output setup that operates in M-QAM and having X_T transmit antenna and Y_R receiving antenna as:

$$p=Hv+m, \quad (1)$$

where $v=[v_1,v_2,\ldots.v_N]^T$ is an optimizing nonlinear function. PSO as the name suggest is malleable and omnipotent seek method which is based on the idiosyncrasy of a army or cram of insects or a herd of birds or a scrum of fish is pertained for a range of seek and optimization problems. Each particle in PSO is analogous with a posture and rapidity. Based on the objective function the best position is identified from the design space where the particles are randomly distributed. The posture and rapidity

Revised Manuscript Received on 14 October, 2019.

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of the particles are adjusted on the accumulated excel values. For an un restricted escalation problem, the objective is to escalate f(*Y*) with $Y^l \le Y \le Y^U$, where T^l represents the lower edge and T^U represents the upper edge. Considering the rapidity of swarm the initial repidity of the entire group is denoted as $U_I = [U_1, U_2, U_3, \ldots\ldots U_N]^T$ .The rapidity vector is obtained using the equation given below.

$$U_{n+1}^i = wU_n^i + \sigma_1\gamma_1\left(\widehat{g_n^i} - Y_n^i\right) + \sigma_2\gamma_2\left(\widehat{l_n^i} - Y_n^i\right) + \sigma_3\gamma_3\left(\widehat{m_n^i} - Y_n^i\right) \quad (2)$$

Where $i = 1,2,3,\ldots\ldots g_n^i$, l_n^i and m_n^i ,are native best, region best and universal best values.

The posture vector is represented as follows

$$Y_{n+1}^i = Y_n^i + U_{n+1}^i \quad (3)$$

The coefficients *w, σ_1,σ_2, and σ_3* represents inertial influence, the universal best, the native best and the region best respectively. The parameters *γ_1, γ_2 and γ_3* represent the stochastic vectors and its value ranges between 0 and 1. The inertial influence parameter 'w' is set less than 1. The parameters *σ_1,σ_2, and σ_3* are constants representing "cognitive" and "social" components. The parameters changes depending on the application and mostly the region best (σ_3) is assigned 0. Due to its best optimization PSO placed a vital role in the field of robots, electrical systems and sport but failed in some instance. To overcome this instance comes the next technology Darwinian Particle Swarm Optimization (DPSO). DPSO is similar to PSO except the chance of existence at a given time by regulating the collection of swarms. The superiority of DPSO is the capability to work with multiple swarms in a given time in any discrete search space and escape of local optima which becomes complicate in PSO. The proposed DPSO algorithm is a binary PSO algorithm which runs many PSO simultaneously where each PSO depicts a swarm by discarding swarms as the search leads to optimization within the native. The aptness of all swarms are estimated and updated.

In the growth of PSO further survival was the Fractional Order Darwinian Particle Swarm Optimization (FODPSO) proposed by Couceiro et.al in [6], here the convergence rate is controlled by fractional calculation of the proposed algorithm which is compared with DPSO and PSO [9]. In addition to this a multi-tiered threshold based FODPSO was proposed in [7] which favoured FODPSO. In literature [3], magnetic resonance brain image segmentation based on FODPSO was proposed and with a accuracy of 99.45% which is about 2.5%higher than DPSO (97.08%). The concept of fractional differential with fractional coefficient σ ϵ C of a general signal *x(t)* proposed by Grunwald–Letnikovdefinition is depicted as

$$D^\alpha\left[x(t)\right] = \lim_{h\to 0}\left[\frac{1}{h^\alpha}\sum_{k=0}^{-\infty}\frac{(-1)^k\Gamma(\alpha+1)x(t-kh)}{\Gamma(k+1)\Gamma(a-k+1)}\right] \quad (4)$$

The DT execution of the above equation is given as

$$D^\alpha\left[x(t)\right] = \left[\frac{1}{T^\alpha}\sum_{k=0}^{-\infty}\frac{(-1)^k\Gamma(\alpha+1)x(t-kT)}{\Gamma(k+1)\Gamma(a-k+1)}\right] \quad (5)$$

The formulation of FOPSO for multi-tiered threshold is depicted below

$$D^\alpha\left[v_{n+1}^i\right] = \sigma_1\gamma_1\left(\widehat{g_n^i} - Y_n^i\right) + \sigma_2\gamma_2\left(\widehat{l_n^i} - Y_n^i\right) + \sigma_3\gamma_3\left(\widehat{m_n^i} - Y_n^i\right) \quad (6)$$

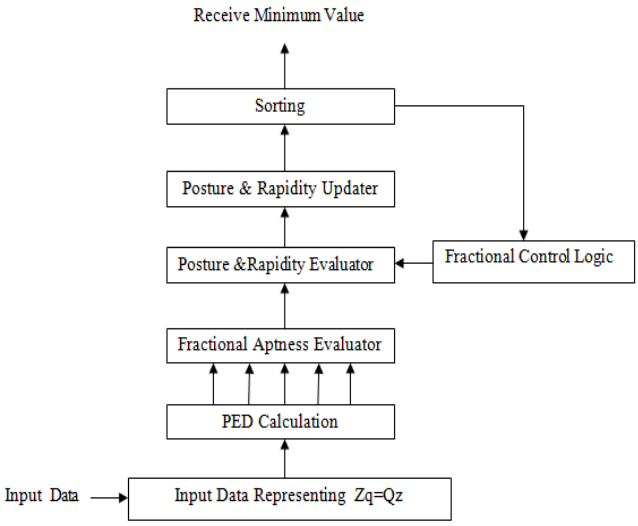

Fig.1. FODPSO based MIMO system model

The calculation complicacy amplifies in linear way with γ, FODPSO prompts a O(γ), storage requirement. For γ = 4, f18 is the derivative and it is given as

$$v_{t+1}^n = \alpha v_t^n + \frac{1}{2}\alpha v_{t-1}^n + \frac{1}{6}\alpha(1-\alpha)v_{t-2}^n + \frac{1}{24}\alpha(1-\alpha)(2-\alpha)v_{t-3}^n + \rho_1\gamma_1\left(\widehat{g_t^n} - x_t^n\right) + \rho_2\gamma_2\left(\widehat{x_t^n} - x_t^n\right) + \rho_3\gamma_3\left(\widehat{n_t^n} - x_t^n\right) \quad (7)$$

The fractional calculus is denominated by the criteria α and DPSO with α =1, is a specific case of FODPSO,

III. HARDWARE ARCHITECTURE DESIGN FOR FODPSO BASED MIMO DETECTION

The proposed architecture is a 8×8 MIMO and 64QAM, iterative complex K-best low power hardware decoder with K and Rlimit as 4 and also a pipelining eight levels structure for abolishing dependency and achieving higher data rate. The lower level fetches the information from both antenna and receiver whereas the other 7 levels do the same from the immediate corresponding registers. The proposed architecture includes two path blocks the Data block and Control block where the former performs arithmetic, logical and sorting operation whereas the later provides synchronization and control signal respectively. The schematic diagram of the projected design is shown in Figure.2.

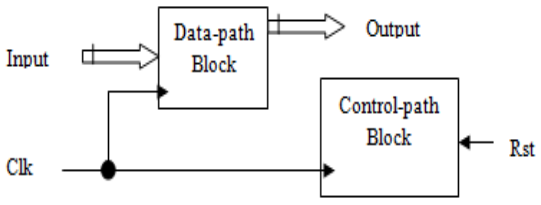

Fig.2. Schematic diagram of projected Design.

Fig.2 shows the Architecture of proposed work with *y* and R as input and the output specifies the best node and Cumulative PED. Clk represents the system clock and other initialization for the architecture is done through Rst, the set signal.The generalized illustration of proposed data-path architecture design is explained below in Fig.3.

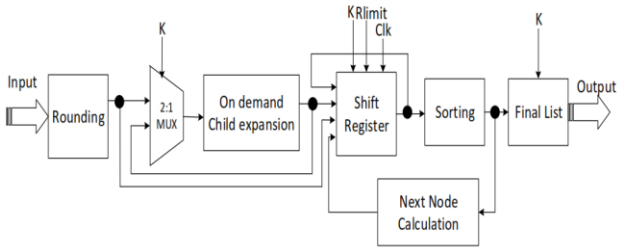

Fig.3. Flow diagram of data-path block.

Fig.3 explains the flow diagram of the Data-path block where rounding is done initially after receiving the input. The initial K-best node is calculated using a demand child expansion along the axial and then moved to the shift register following by sorting for selecting the node with minimum distance which is the node for next level. Using demand expansion method the final node is selected for final list along the imaginary axis and the next child is calculated and it updates the register for the particular index and the procedure repeats till k-best nodes get selected for upcoming candidates of the next level. Reforming of register is done using the following four process such as rounding, calculating the initial nodes, calculating the node in imaginary domain, and retrieving the previous value. The above structure is the stable hardware design for all the eight leveld.

. The generalized illustrations of updated shift register are given in Fig.4.

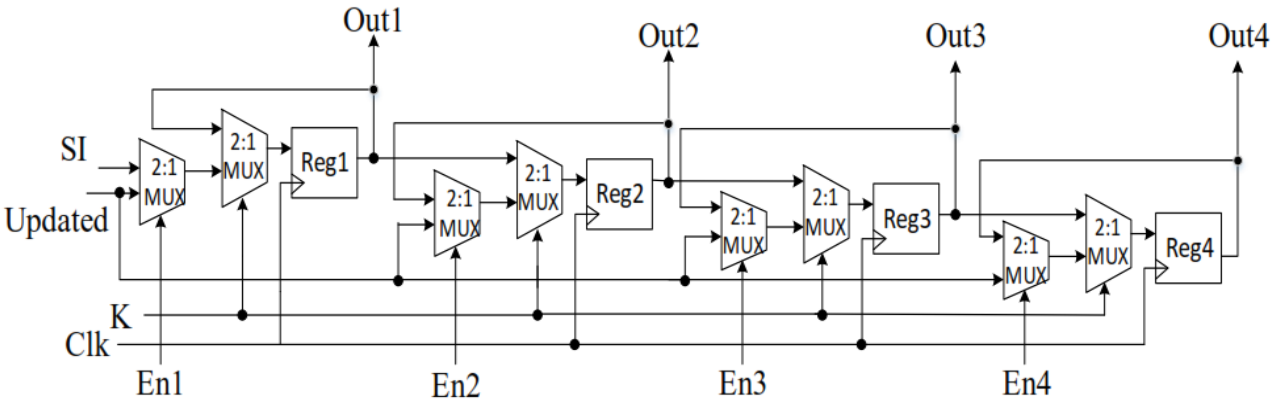

Fig.4. Flow diagram of the updated shift register

Fig.4, portrayed the operation of updated shift register. After on demand child expansion for K times the shift registers are updated by serial input (SI). Best node of four register gets loaded to their corresponding register after the sorting process gets completed and the enable signals decides the register which is to be updated. Fig.5 exhibits the cycle flow for all the eight levels. In level1 the initial k-best nodes are calculated from input and shifted to register1. While level1 operates with new input the next level2 fetches the value from register 1 and performs in parallel and the process continues till the last level fetches value from Register 7 and obtains its final output. The proposed algorithm is sequential thus increases the data rate and eliminates the complexity of hardware by eliminating multiplier and divider thereby reduces the cost in terms of power consumption. Fig.5 presents pipelined architecture of 8x8 MIMO.

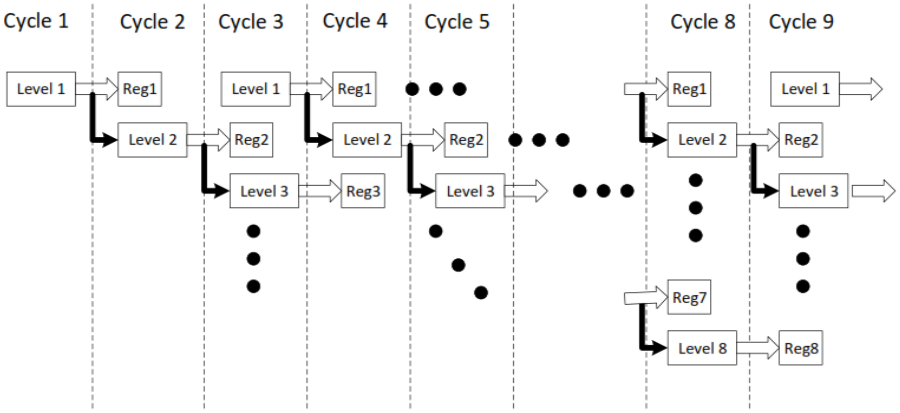

Fig.5. Design flow of the proposed VLSI Architecture.

IV. RESULT

The architecture is proposed for 8x8 Multiple Input and Multiple Output and 64 Quadrature Amplitude Modulation with both K and Rlimit as 4 is coded in verilog and synthesized in 45nm CMOS technology. Simulation and verification for fixed point realization of repetitive LR-aided K-best decoder is conducted in MATLAB and Xilinx. Reduction of cost, power and area is obtained by performing fixed point conversion to minimize the bit length and choosing the best fit architecture for all the sub modules of K-best decoder. The simulation results bestows that a BER within limit of 0.3 dB for Multiple Input and Multiple Output amend disparate modulation is possible only with a word length of 16 bits thereby suited for best design and implementation. For requirement of IEEE802.16e, FODPSO on demand K-best decoder includes computing stage and complex operations such as sorting, PEC calculation etc and multiple clock cycles at all level. In the proposed architecture every stage requires eight clock cycles (K+Rlimit) times. The proposed architecture is synthesized using XST in 45nm CMOS technology and coded in Verilog for a Maximum frequency of 181.8 MHz, 1090.8 Mbps through and a power consumption of 782mW and latency of 0.044µs. A gate count of 63.75kG is obtained by dividing the area by area of NAND gate. The normalized hardware efficiency (NHE) is obtained as 0.0585 after performing required analysis.

NHE(kG⁄Mbps)=corearea (kG)/scaled throughput(Mbps) (8)

Existing Techniques	2007 [8]	2010 [6]	2010 [9]	2010 [3]	2011 [4]	2011 [10]	2013 [7]	Proposed work
Modulation	16QAM	16QAM	64 QAM	(4–64) QAM	64QAM	64 QAM	64QAM	64QAM
Antenna	4×4	4×4	4×4	4×4 – 8×8	4×4	4×4	4×4	8×8
Methodo -logy	K-best	SISO-SD	K-best	MBF-FD SD)	SISO MMSE-PIC	K-best	Modified K-best	FOD-PSO K-best
Zone	Complex	Complex	Real	Complex	Complex	Real	Complex	Complex
Process	0.13um	90nm	65nm	0.13um	90nm	0.13 um	0.13um	45nm
K	64	Not Applicable	5-64	Not Applicable	Not Applicable	10	10	8*
f(max) (MHz)	270	250	158	198	568	282	417	181.8
Throughput (Mb/s)	100	90	732-100	285-431	757	675	1000	1090.8
Gate count (kG)	5270	96	1760	350	410	114	340	63.75
NHE (kG/Mb/s)	52.7	1.6	4.81-35.2	1.23-0.81	0.78	0.17	0.34	0.0585
Power (mW)	847	Not Applicable	165	57-74	189.1	135	1700	782
Latency (us)	Not Applicable	Not Applicable	Not Applicab	Not Applicable	Not Applicable	0.6	0.36	0.044
Hard/soft	Soft	Soft	Hard	Soft	Soft	Hard	Hard	Hard

The table exhibits the comparison of proposed architecture with other available architecture requires low power, less latency, gate count and higher data rate for both hard and soft domain. Comparing proposed architecture with architecture in [4] for 4x4 MIMO with 64 QAM and k as 10 using 0.13µm technology the proposed one is less size, high throughput, power consumption is 2.17 times less and gate requirement is reduced to of 1/5th approximately equal to 340 KG

V. CONCLUSION

The proposed research paper, pipelining based VLSI architecture of FODPSO K-best decoder has reduced complexity based on-demand child extension also includes the parameter Rlimit for obtaining better BER by compromising complexity which is scalable to any MIMO Configuration. The proposed architecture 8×8 MIMO with 64QAM modulation scheme for K and Rlimit equal to 4 is synthesized using XST in 45nm CMOS technology and coded in Verilog for a Maximum frequency of 181.8 MHz, 1090.8 Mbps through and a power consumption of 782mW and latency of 0.044μs using MATLAB and Xilinx for simulation and functional validation and verification.

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