

Performance of Asynchronous Queasy Delay Insensitive (QDI) Circuit Templates

Srikanth Gimmadi, Bhanu Murthy Bhaskara

Abstract: Asynchronous Queasy Delay Insensitive (QDI) is the more promising solution for the reducing the effect off power consumption due improvement in the fabrication technology. In literature there were proposed many QDI techniques but Precharged Half Buffer (PCHB), Autonomous Single Validate Half Buffer (ASVHB) and Sense Amplifier Half Buffer (SAHB) are efficient techniques. In this paper author implemented the templates of PCHB, ASVHB and SAHB. Simulation results are verified, and results are compared. From the result it is observed that SAHB will consume the less power and takes the less area for constructing the template when compare to other two methods.

I. INTRODUCTION

Synchronous methodology is used for the designing many digital applications where the devices operated above the sub threshold voltage and clock signal power consumption is not dominating parameters. Today all the Transistors are designed with an operating voltage less than 1 volt where clock signal power become major issue. As the chip density increases, the clock signal distribution is very much complex, and the clock signal power consumption is also more. Modern devices are battery operated which demands the circuits which operated at Low power to increase the battery life.

There are many power reduction techniques proposed such as clock gating, Power gating and multi threshold techniques.

Asynchronous design technique is the best solution for the reduction of clock signal power when compare to the Synchronous design Technique.

The most important advantage of Asynchronous design technique is clock skew avoidance [1]. They also provide the advantage of higher performance and low power consumption. The main challenges are to design the templates by using the slandered EDA commercial tools, higher area required and testing complexity.

In this paper section 1. describes the asynchronous design concept and implementation. Different Half buffer techniques are explained in section 2. In section 3 implementation of basic templates of different half buffer gates are designed and simulated. Finally, in section 4 results were discussed.

II. ASYNCHRONOUS DESIGN METHODOLOGY

Asynchronous circuit design includes the two main blocks. One block is for establishing the communication between the peer which is known as handshaking protocol

and the second block for logical design. In handshaking protocol the bundle data will transfer between the two peers when the separate request and acknowledge signals were activated [2]. The protocol may use the 4-phase or 2- phase communication.

In 4- phase protocol sender sends the data by initiate request HIGH, receiver receives signal and sends the acknowledgement HIGH, sender respond by setting the request LOW and receiver acknowledge by setting acknowledgement LOW. At this point sender may initiate the next data transfer [9]. The same is shown in the fig 1.

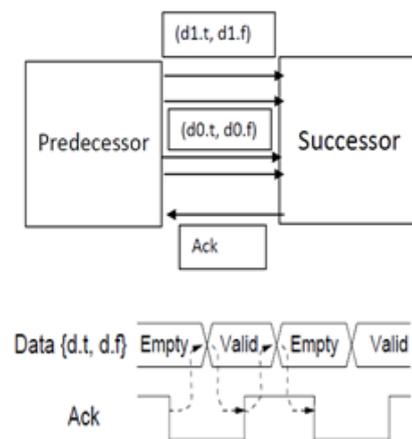


Fig 1. Delay Insensitive using the 4- channel

protocol

In 2- phase protocol sender sends the data by altering the request state LOW to HIGH and receiver acknowledge by setting HIGH to LOW which is shown in the fig 2. The 2-Phase protocol faster than the 4- phase protocol.

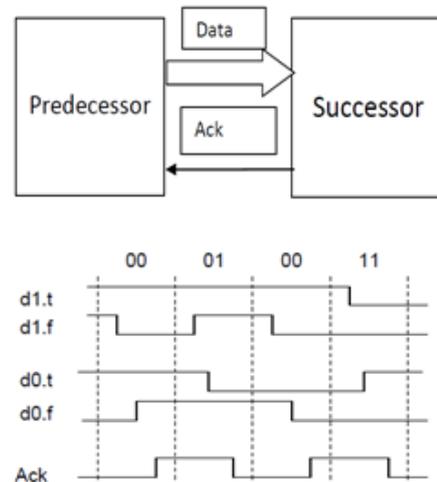


Fig 2. Delay Insensitive using the 2- channel protocol.

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Srikanth Gimmadi, Department of ECECMR Technical Campus, Hyderabad, Telangana, India.

(Email: gimmadisrikanth79@gmail.com)

Bhanu Murthy Bhaskara, Department of Computer Science and information Technology, University of Majmaah, Saudi Arabia.

(Email: b.bhaskara@mu.edu.sa).

In this paper we used the 2- Phase dual rail protocol. In 2-Phase dual rail protocol, the data represented in the form of true and false [6].

III. HALF BUFFER TECHNIQUES

Buffer is the circuit used to store the data before the data is going to be processed. In the half buffer technique, the communication between the two entities will takes place one at time. When one is sending the other can only receive and vice versa [3].

There are many half buffer techniques are proposed like Precharged Half Buffer (PCHB), Autonomous Signal Validity Half Buffer (ASVHB) and Sense amplifier Half Buffer (SAHB). Each of the technique is having their own advantages and disadvantages [7,8].

A. Precharged Half Buffer (PCHB)

In this technique the buffer is charged to certain voltage before the data is transferred between the two entities. This Design circuit consists of two block.one is called controlled block which generates control signal Rack, Lack. Left Code Detector (LCD) and Right Code Detector (RCD) as output code detector. The second block is called Logic block, where logic to be implement in logic1 and in logic 0 form. The circuit consist of pull-up and pull-down transistors and both are controlled by EN.. Pullup transistors are used to precharge the transistor and to take Output in True logic Q1 and Q0 is in False Logic, whereas the pull-down transistors for logic implementation [5]. A0, A1 and B0, B1 are the two inputs in true form and its complementary form as shown in fig3.

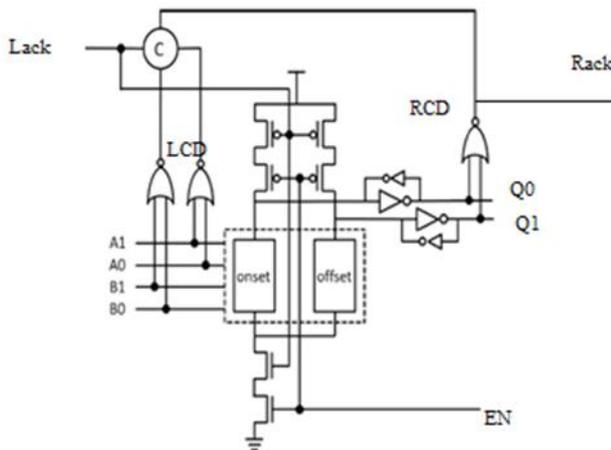


Fig 3 Precharged. Half Buffer Technique

To validate the inputs D1.T, D2.T and D1.F, D2.F, Input Code Detector (ICD) and to validate the outputs O.T, O.F, Output Code Detector (OCD) signal are used. S.T and S.F are intermediate outputs.

B. Autonomous Single Validate Half Buffer

In this technique data is validated by using the data validate signal and each bit will have individual data validate signal therefore it is called as an Autonomous Single Validate Half Buffer (ASVHB).

The AVSHB consists Functional block and Control block. Functionals block internally consists two rail sub block one is called as a True rail sub block, and another is False rail

sub block. Each sub block further divided into Hold block, Precharge block and Evaluate block. The Control block will generate the Control signals Rack and Lack. The Rack is the next stage signal acknowledgement and Lack is the previous signal acknowledgement as shown in Fig 4.

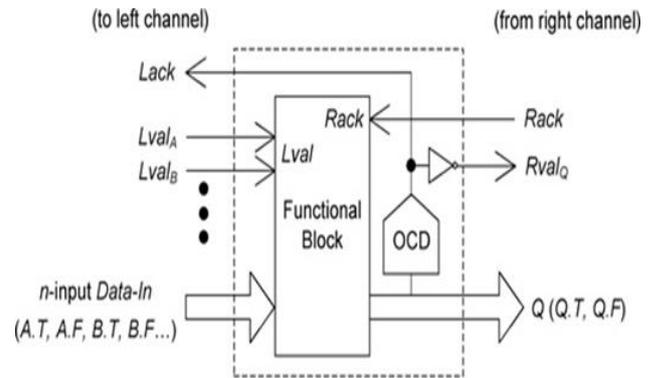


Fig 4 Autonomous Single Validate Half Buffer Block diagram

C. Sense Amplifier Half Buffer

In this Technique handshaking process is performed by A Sense Amplifier because this reason it is called as Sense Amplifier Half Buffer (SAHB) [4]. The cell mainly consists of two blocks, one is sense is called as amplifier block and second one is evaluation block to perform the required digital logic.

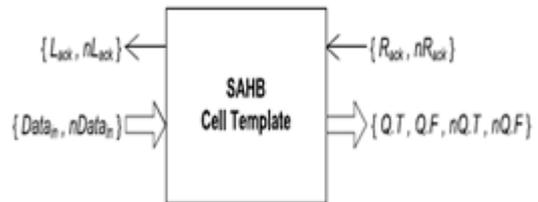


Fig 5: Sense Amplifier Half Buffer

Fig 5. represents basic sell template. Sense amplifier circuit involves cross coupled latch which generates the signal left channel acknowledgement Lack, nLack and signal right channel acknowledgement Rack, nRack. The data inputs are Datin and nDatin and Q.T/Q.F and nQ.T/nQ.F are the data outputs. Beginning Lack and Rack are set to logic "0". During the evaluation phase ,when valid input present at Datin and Rack logic "0" and output will be obtained at Q.T/Q.F and Lack stated to 1 indicates validity of the output. The same process will be repeated for the another set of input.

IV. LOGICAL IMPLEMENTATION & RESULTS

A. Precharged Half Buffer (PHB) Templates

The operation of 2-input NAND template is explained as follows. First, set all the data input (A/B) and data output (Q.0/Q1) is empty i.e., logic "0", the handshake signals (Lack & Rack), the control signal (En) and intermediate outputs are placed at logic "1". When valid data input is applied, the pull-down network evaluates the functional block which provides valid data output at

Q0/Q1. Now the completion of evaluation is acknowledged by setting Lack & En to logic“0” through LCD/RCD.

When data input & output are empty (Rack to logic “0”) then LCD/RCD reasserts Lack & En to logic “1”. After reset operation, a new process of the cell can be started by setting

Rack to logic“1” [5].The NAND/AND gate schematic and simulation results are shown in figure 6 and Fig 7 respectively. Similarly XOR/XNOR schematic and simulated results are explained in fig 8 and Fig 9 respectively.

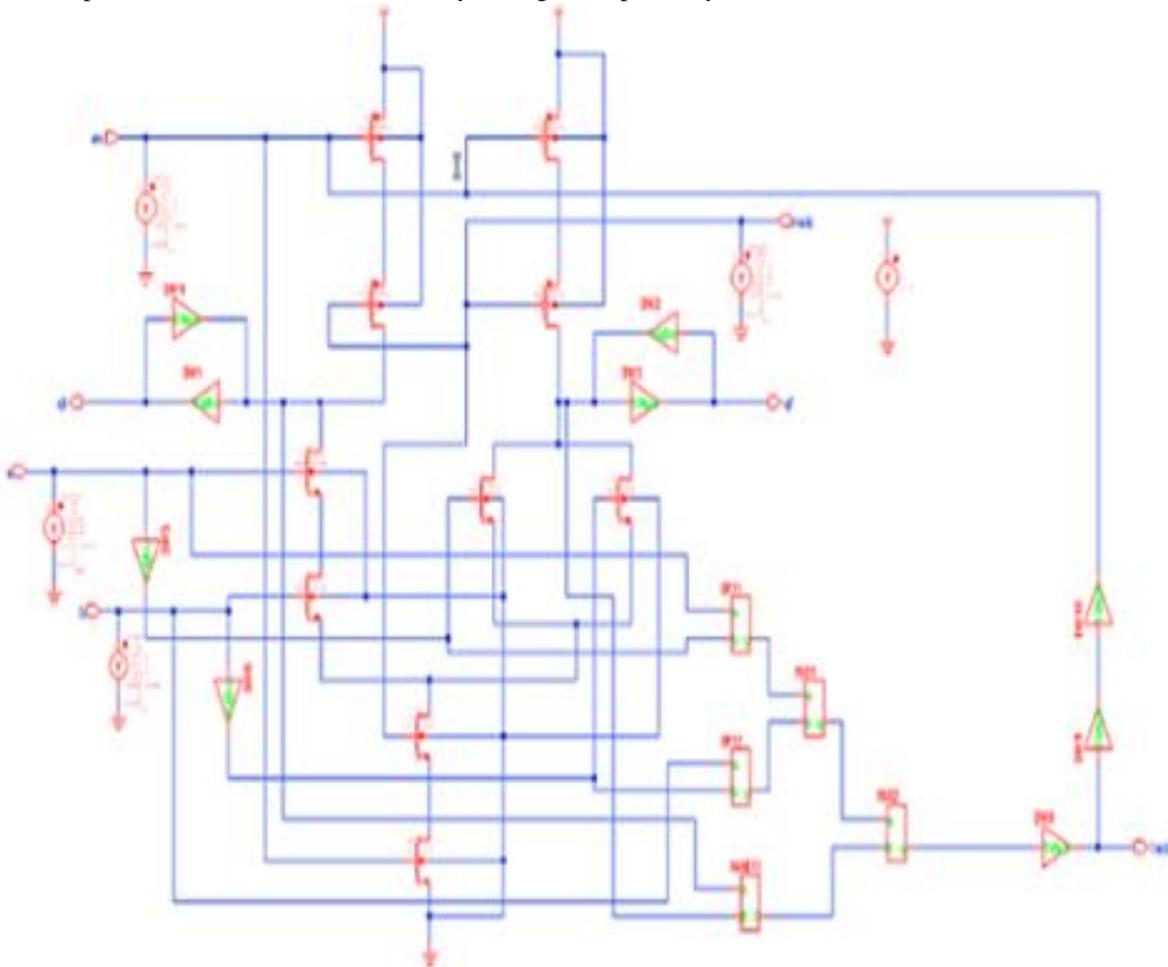


Fig 6. Two input NAND/AND PCHB Schematic

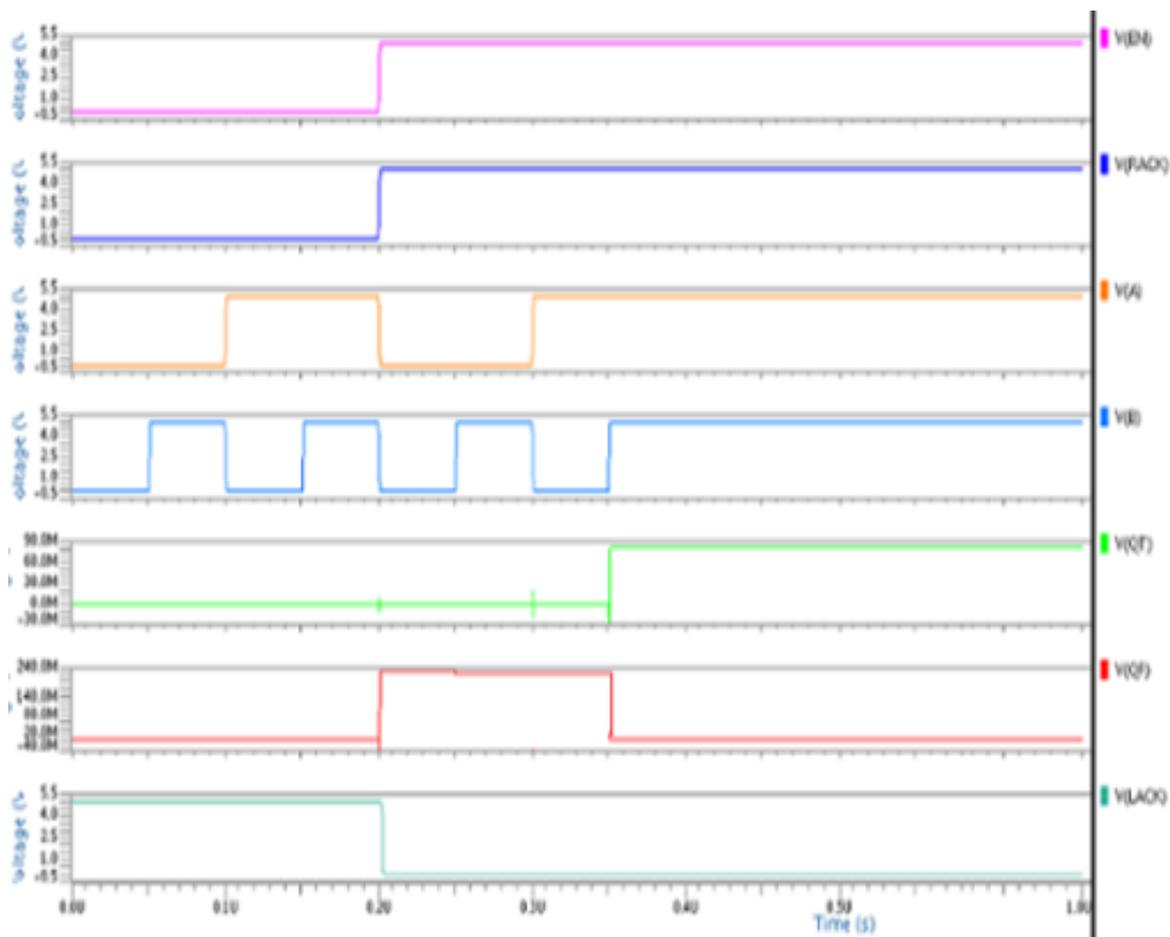


Fig7. Two input NAND/AND PCHB Simulated results

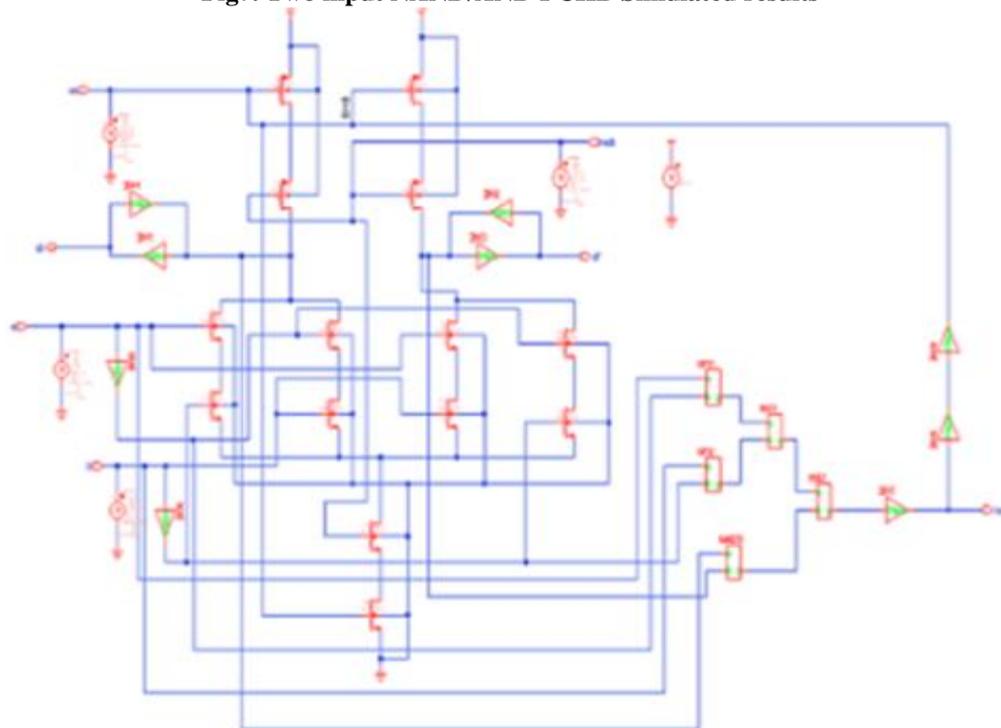


Fig 8. Two input XOR/XNOR PCHB Schematic

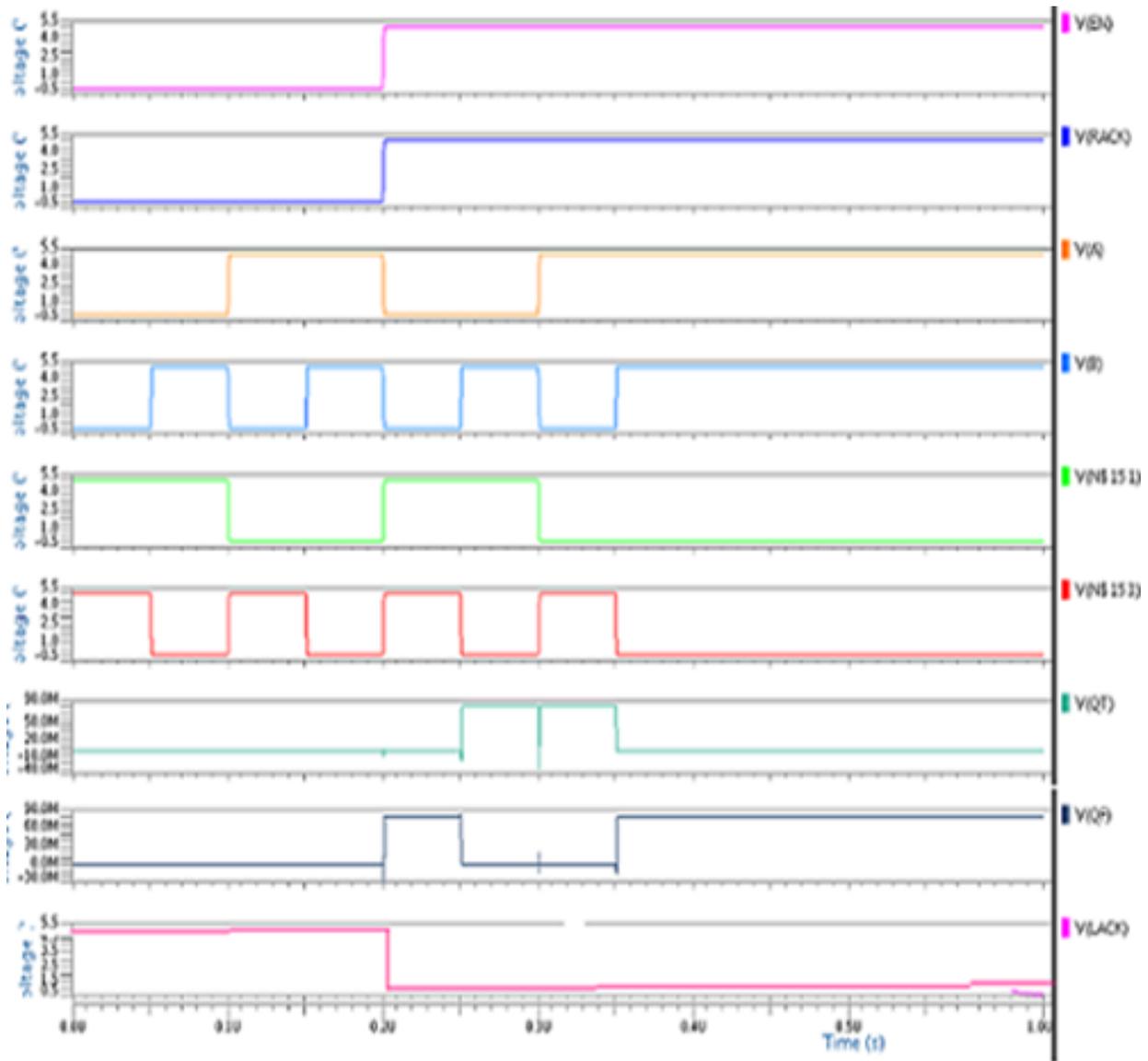


Fig 9. Two input XOR/XNOR PCHB Simulated results

B. Autonomous Single Validate Half Buffer templates

The basic templates of ASVHB Are shown in fig. The working of AVSHB AND/NAND cell is explained as follows. True subblock consists A.T, B.T as input and Q.T as an output is taken from cross coupled inverter. Inputs are D1, D2 are validated with LvalA and LvalB signal and similarly the False block circuit.

At the beginning input data A.T/A.F and B.T/B.F ,output Q.T/Q.F, LvalA and LvalB signal are kept at logic “0”. At this condition precharge block set the intermediate data (S.T/S.F) are at logic “1”. The hold circuit set the Rack and Lack to logic “1”. If inputs are applied at A.T=1 and B.T=1 then this will be evaluated in evaluation block , S.T will be changed to logic “0” and Q.T will be switched to logic “1”.This will make Lack to logic”0”.Similarly the same process will be repeated for the next data inputs [5]. The same is explained in Fig 10 and Fig 11.

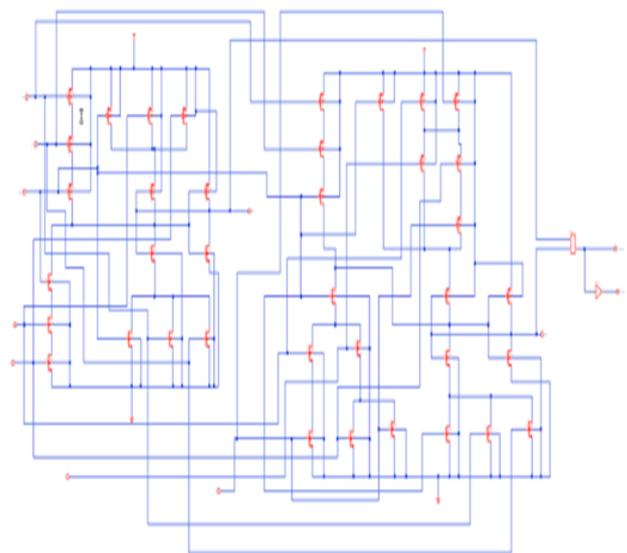


Fig 10. Two input AND/NAND AVSHB Schematic

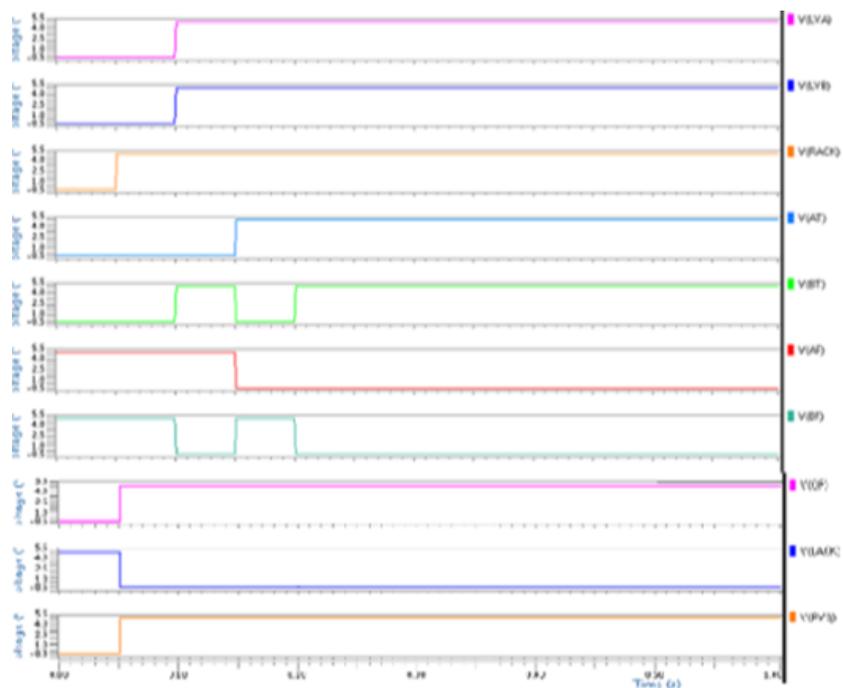


Fig.11. Two input AND/NAND AVSHB Simulation

c. Sense Amplifier Half Buffer Templates

The working principle of SAHB AND/NAND as follows. Initially Lack and Rack are reset to zero [9]. Data in and Q.T/Q. F are made empty. During the evaluation phase Lack and Rack are set to 1 by sense amplifier after checking the

correctness of data and $Q.T=0 / Q.F=1$. From the input combination $A.T=1, B.T=1$ the corresponding NAND logic output $N.Q.T=1$. Fig 11 and Fig 12 schematic and simulated results of SAHB AND/NAND.

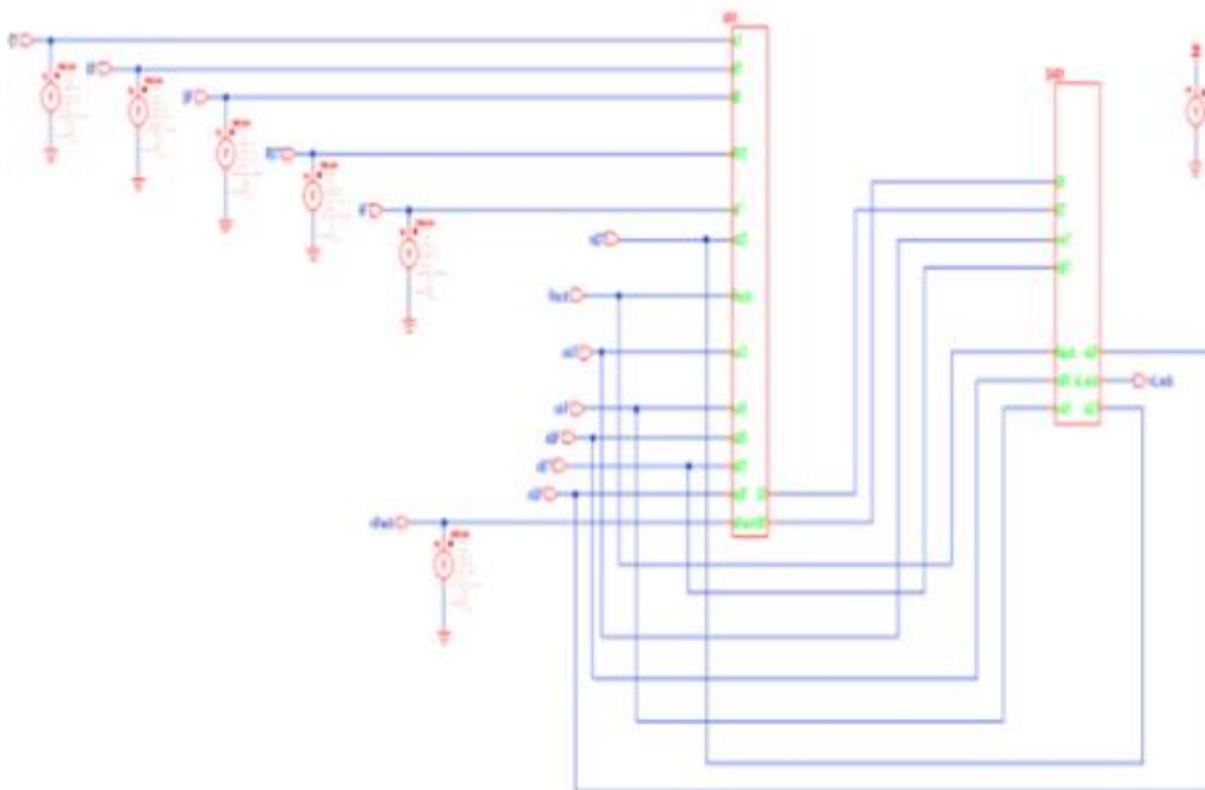


Fig 12. Two input AND/NAND SAHB Schematic

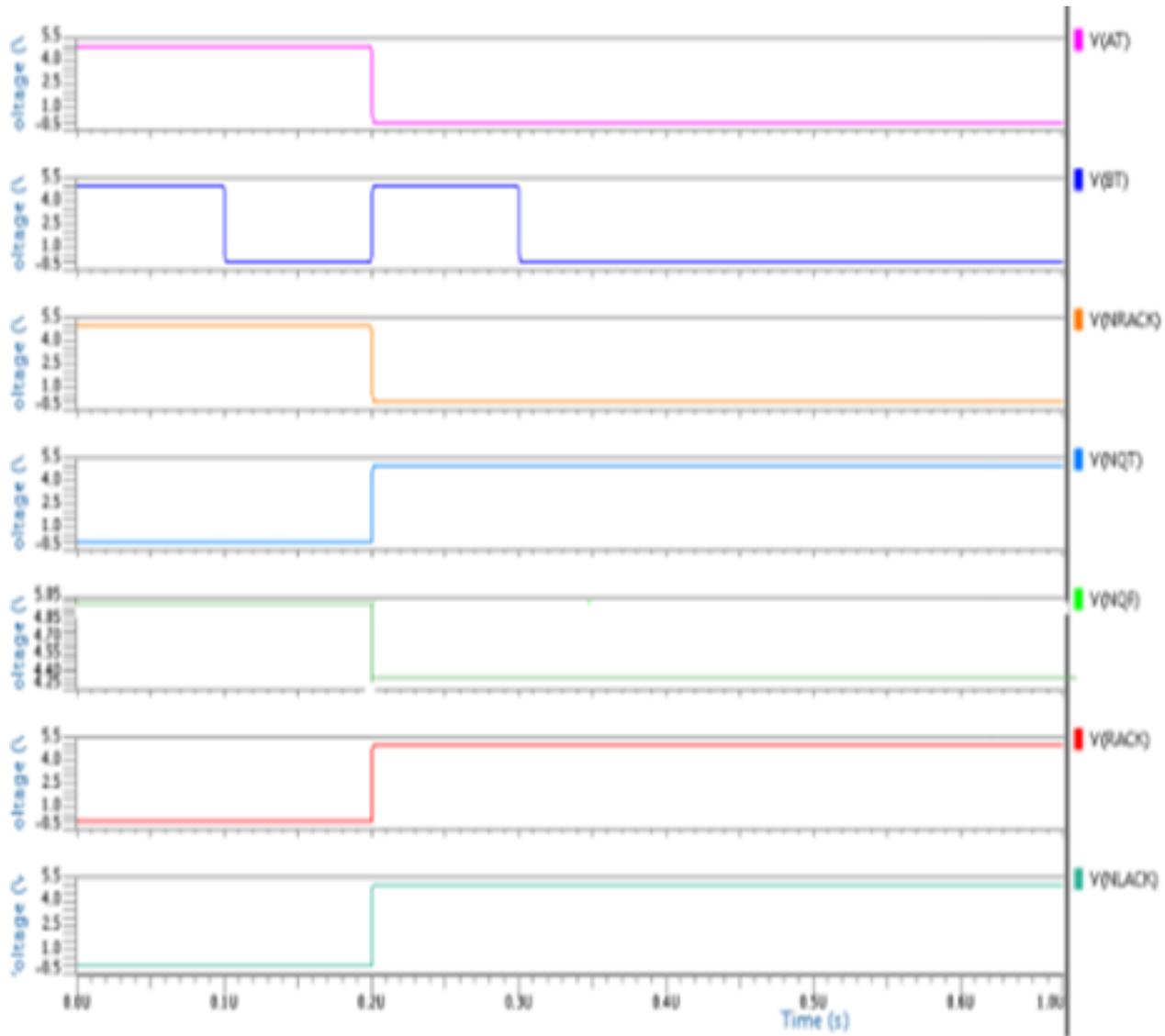


Fig 13. Two input AND/NAND SAHB Simulation

V. RESULTS AND CONCLUSION

Asynchronous queue Delay insensitive circuit templates are designed and analyzed using Mentor Graphic tool at 65 nm. The Comparison of performance parameter for 1-bit adder circuit is illustrated in the table 1. From the results Table 1. it is concluded that the area and power required for SAHB template is less when compare to other Techniques.

Parameters	SAHB	PCHB	ASVHB
Area (mm ²)	0.0006	0.0008	0.0010
Energy (fJ)	0.24	0.32	0.41

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