Performance Evaluation of an Efficient 5-2 Compressor for Digital Applications

N. Mathan, G. Jegan, M. SatyaSaiAvinash, M. Krishna Yadav

Abstract: ***This paper presents an efficient performance 5-2 compressor which consumes less power. The architecture of this compressor consists of full adder, XOR's, CGEN and MUX blocks. This architecture is mainly implemented based on Cout signals independent of Cin signals in order to reduce the carry propagation to a compressor. An efficient full adder is used to optimize the compressor architecture. In this design, an existing carry generator, XOR, MUX blocks configure with the proposed full adder circuit. The proposed design for full adder employs using pass transistor logic, which eliminates the weak logic in the circuit. This technique is mainly considerable for less power consumption. The parameters of proposed architecture is compared with other designs i.e. power-delay product, average-power, and delay. Simulations were done using HSPICE software in 130nm and 32nm technology. The simulation results show the improvement in the overall performance of the 5-2 compressor.***

Key Words: ***Compressors, Multipliers, Full Adder, HSPICE, CGEN.***

I. INTRODUCTION

In CMOS technology, the use of multipliers has been increased which made developers to concentrate more on the performance of multipliers that consumes low power and minimum delay. Demand for high-performance of arithmetic circuits in the applications like digital signal processing and algorithms i.e. filtering and convolution. Multipliers dictate the power dissipation and overall circuit's performance. Consequently, designing low-power and fast arithmetic circuits, including efficient multipliers made better improvement in performance.

The process of multiplication consists of three steps. In the initial stage partial products are generated by multiplying the multiplier and the multiplicand bit by bit. The second stage is Partial products reduction stage, which decides the performance of the overall multiplier. In the final stage addition with carry propagating out of which the second step utilizes the maximum power, area and delay. Compressors are used/implemented to decrease the latency.

The partial product reduction stage increases the use of power, delay and area. Compressors mainly implement at the second stage because they are used to reduce the latency in the critical path and the partial products which is important to maintain the performance of the circuit. The power consumption and performance of the multipliers will be directly proportional to the efficiency of the compressors. So, that demand on implementing high speed compressors are widely increasing. In this paper, the architecture of the compressor uses Cout signals are independent of Cin signals. In a full adder design pass transistor logic reduces the power as it is uses a single NMOS transistor as a PTL switch. The switch is considered closed when the voltage applied to the gate is logic high, and it is considered open when the voltage applied to the gate is logic low.

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II. FUNCTIONALITY OF 5-2 COMPRESSOR

The compressor optimizes the complex path, describing the complete circuit performance, due to which the requirement for low power and high speed compressors is gradually increasing. Basically, a 5-2 compressor has 5 inputs of the same weight, includes 5 main inputs and 2 carry inputs Cin1 and Cin2 that are received from a previous compressor of 1 binary bit lower. It has two outputs carry and sum, along with two carry outputs Cout1 and Cout2 of 1 bit higher.

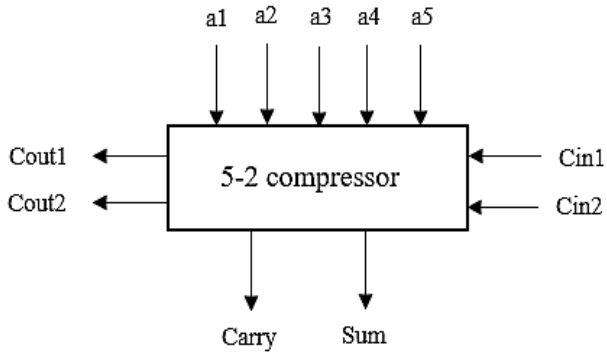


Fig. 1. Representation of 5-2 Compressor

It was governed by the following equation:

Cin1+Cin2+a1+a2+a3+a4+a5 = Sum + 2 (Carry+Cout2+ Cout1)

III. EXISTING DESIGN

Compressors are the main component in the arithmetic circuits. Mainly, three conventional full adders are cascaded having more delay i.e. 6Δ delay. In order to reduce the propagation delay many architectures are proposed. The main aim is to reduce the delay in order to increase the performance of the circuit. In this design, compressor consists of full adder, XOR, CGEN and MUX blocks. This architecture, mainly uses Cout1 must be independent of

Cin1 as well as Cin2. In addition, Cout2 must be independent of Cin2. Use of CMOS full adder block in the circuit improves 34% faster operation than two cascaded xor gates. The critical delay of this architecture is around 4Δ of mux/xor gates that limits the delay to a compressor. Further reduction of the delay is impossible in the compressor architecture.

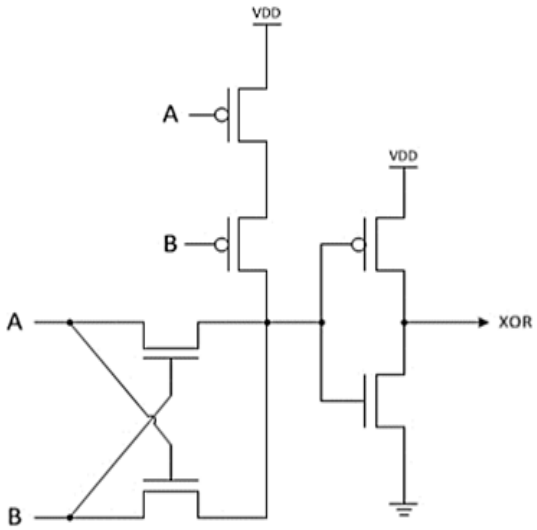


Fig. 2. Pass transistor XOR* block

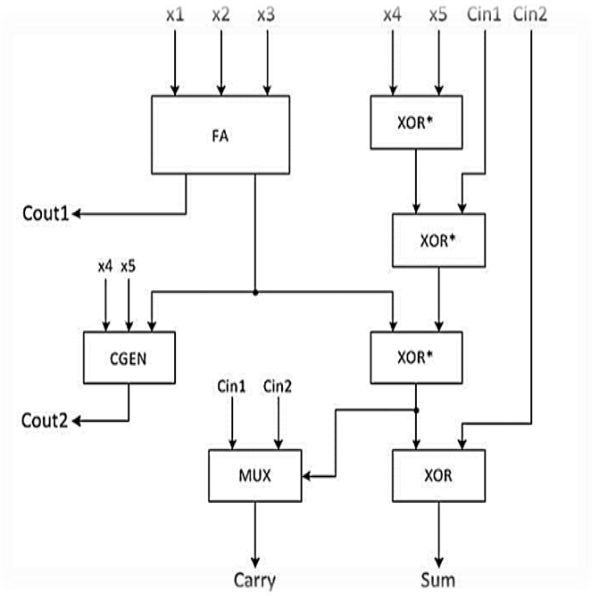


Fig. 3. Block diagram of 5-2 Compressor

In this design, x1, x2 and x3 are the inputs to the full adder block and the remaining inputs given to the XOR* blocks. The final sum output is obtained from the conventional xor gate in order to avoid the static CMOS inverter delay in XOR* block. Further CGEN blocks are used to generate the carry output signal cout2. The conventional MUX block is used to generate carry signal from the Cout signals of the previous compressors.

Here, Transmission gate logic full adder is used in the full adder block. Six transistors Pass transistor logic XOR is used in XOR* block eliminates weak logic. Conventional MUX block and XOR gates have been implemented in XOR and MUX blocks.

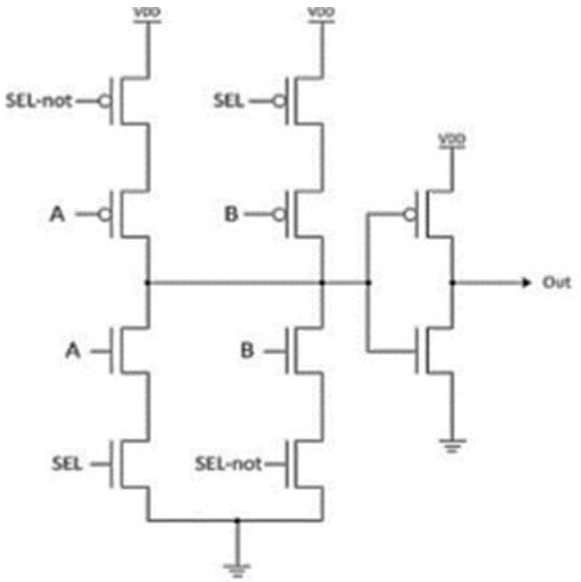


Fig. 4. Implementation of MUX block

IV. PROPOSED DESIGN

The functionality of a conventional FA can be replaced by various FAs. Transmission gate full adder uses a less number of transistors compared to static CMOS logic full adder. It passes data on both 0 and 1. When PMOS is OFF and NMOS is ON then it will pass data on logic '1'. Similarly, when NMOS is OFF and PMOS is ON then it will pass data on logic '0'. Using both PMOS and NMOS in transmission gate power dissipation is more. To reduce power dissipation and energy pass transistor logic is proposed. Here, two NMOS are used instead of two transmission gates by using a static inverter the data of logic '0' is passed.

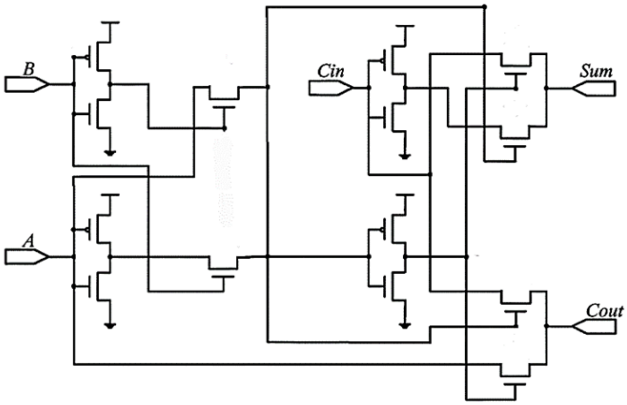


Fig. 5. Proposed Full adder using pass transistors

V. SIMULATION AND RESULTS

5.1. Simulation Environment

Simulations are implemented in HSPICE tools and the parameters, i.e. power, delay, power-delay Product are calculated using COSMOSCOPE tool which is included in HSPICE tool. The simulations are targeted in 130nm and 32nm technology for supply voltage of 0.9V and 3.3V.

5.2. Simulation Results

Comparison of Existing and proposed compressors by implementing them in 32nm and 130nm. The supply voltage of 32nm is 0.9V. Similarly, supply voltage of 130nm is 3.3V. Output waveforms of the modified 5-2 compressor shown in fig. 6.

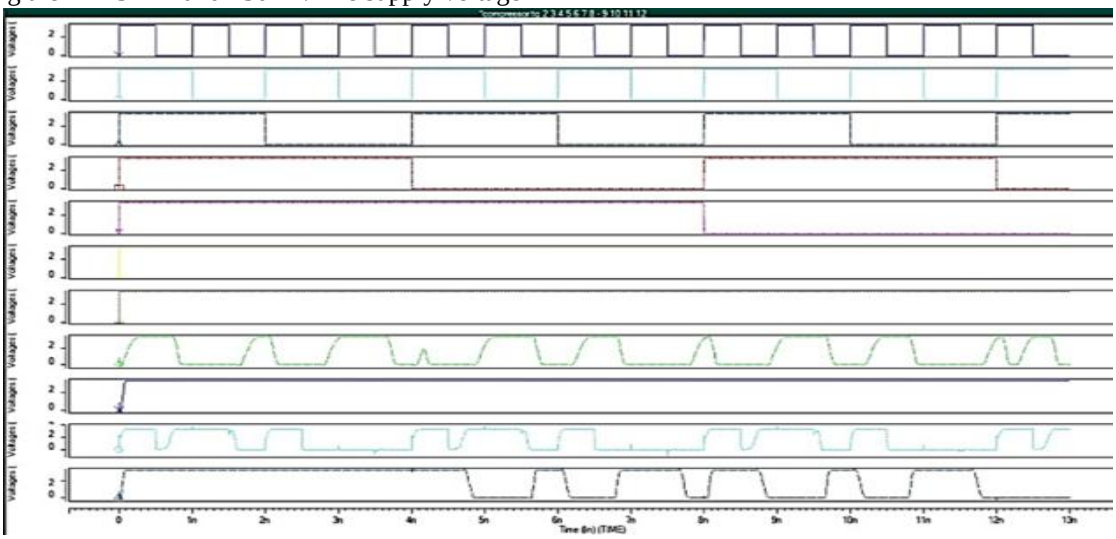


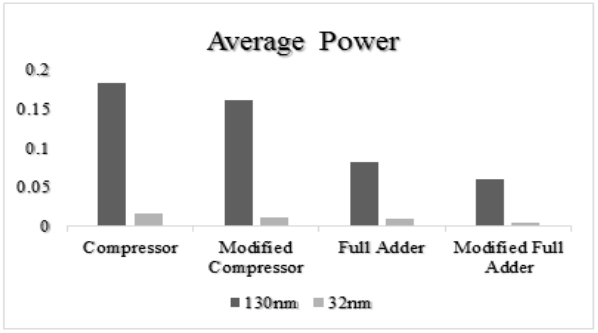
Fig. 6. Output waveforms of Proposed 5-2 Compressor

Table 1: Comparison of existing and proposed 5-2 compressor

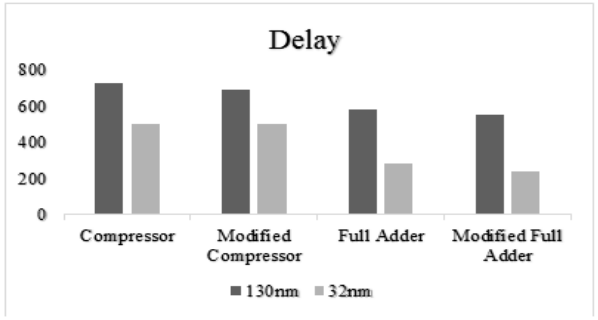
Properties	Average Power [W]	Delay [s]	Power-delay product [J]	Rise time [s]	Fall time [s]
Compressor	$1.838x10^{-04}$	$729.08x10^{-12}$	$134.04x10^{-15}$	$142.32x10^{-12}$	$77.45x10^{-12}$
Proposed compressor	$1.612x10^{-04}$	$691.42x10^{-12}$	$111.45x10^{-15}$	$138.15x10^{-12}$	$72.35x10^{-12}$

Table 2: Comparison of existing and proposed full adder

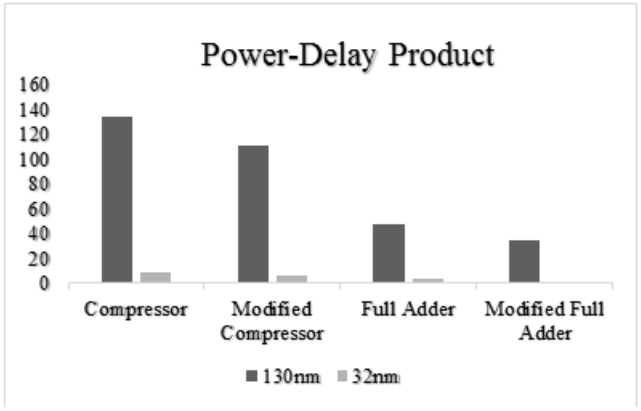
Properties	Average Power [W]	Delay [s]	Power-delay product [J]	Rise time [s]	Fall time [s]
Full adder	$8.217x10^{-05}$	$582.16x10^{-12}$	$47.83x10^{-15}$	$60.315x10^{-12}$	$104.21x10^{-12}$
Proposed Full Adder	$6.145x10^{-05}$	$554.09x10^{-12}$	$34.04x10^{-15}$	$55.81x10^{-12}$	$71.26x10^{-12}$



(a)



(b)



(c)

Fig. 7. (a) Power, (b) Delay and (c) Power-Delay product of Full adder and 5-2 Compressor

Fig.7 shows the performance chart of the existing and modified compressor, full adder. It compares modified compressor and full adders in different technologies i.e. 32nm and 130nm. The performance of the 5-2 compressor shows better improvement in 32nm technology than in 130nm technology.

Performance analysis of the modified 5-2 compressor in properties such as power, delay, power-delay product. It shows that modified compressor produces the better results where it consumes 12% less power compared to the existing compressor. The overall power-delay product of the modified compressor reduced by 18%. This shows the performance of the modified 5-2 compressor is better compared to the existing architecture.

VI. CONCLUSION

The architectures of the 5-2 compressor are analyzed using HSPICE tool and implementation of XOR gate and the Full Adder blocks using Pass transistor logic. Novel Full Adder circuit has been proposed and compared with the existing Full adders. Simulations of the 5-2 compressor architectures are done in 0.9V and 3.3V supply voltages. The performance of the proposed Full adder is better than the existing Full adder in parameters, i.e. average-power, delay and power-delay product in 130nm and 32nm technologies.

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