Performance Assessment of Different VLSI Architectures for Data Comparators for Cost-Effective Sorting Networks

Geetha V, Anbumani V, Ragakavya K, Navaladi P, Ponraj S

Abstract: Noise removal is one of the major requirements in image, speech and signal processing applications. Impulse noise removal in image processing uses median filters. For edge preservation in image processing this acts as one of the best alternative non-linear technique to linear filtering. Real time hardware implementation of median filters has major concern of sorting networks. Efficient VLSI implementation of sorting network in terms of hardware complexity is of greater importance. This work provides a comparison of existing six data comparators and also proposes three modified data comparators in terms of their hardware complexity, area, power and speed. All the comparators were designed using verilog HDL and were targeted for xilinx ISE 9.2i using Xilinx ISE 9.2i FPGA design suite. From the results Modified Twos Complement Based Data Comparator is the minimum area required architecture with maximum combinational path delay and also with minimum number of LUTs used. The drawback of this architecture is the maximum memory requirement. The Modified Multiplexer Based Data Comparator and Modified Decoder Based Data Comparator architectures are suitable for memory efficient design.

Keywords: Impulse noise, non-linear filtering, VLSI, data comparator.

I. INTRODUCTION

Image processing applications need filtering in order to give attention to specific features of the image. Noise removal in speech and signal processing uses median filter. There are various VLSI signal and image processing architectures [1]-[12]. Speed efficient pipelined and parallel filter for impulse noise removal architecture was developed by Karpagaabirami and S P Ramamoorthy [1]. Speed and power efficient comparator with two stages of CMOS operational amplifier was proposed by Aayisa Banu S et al [2].

Realization of non linear filters using positive Boolean functions in bit serial fashion was proposed by Keping Chan[5]. Various special types of comparators were designed and their static and dynamic characteristics were compared along with speed and output stability by Bharat et al in [3]. Mehamood ul Hassan and Rajesh Mehra [4] developed 1 bit CMOS comparator to minimise the area and power consumption about 50% and 35%. Pipelined parallel architecture for modified shear sorting algorithm for nine elements sorting was implemented by Vasanth et al [9]. Low-energy CSMT carry generators and binary adders were developed by Keshab K.Parhi[10]. VLSI implementation of eight bit data comparators which are used for the Rank ordering image applications were done by Sindhu.E and Vasanth.K [11].

Sorting networks are computationally costly function since it needs large area, speed and power. A sorting network consists of compare and swap operations. The compare and swap operation of two elements x and y needs a compare operation, a swap operation if needed and finally the result as x less than or equal to y. The number of compare and swap operations depends upon the number of elements to be sorted and it has fixed sequence of comparisons. The sorting of 3x3 matrix makes ascending order of the elements first and the fifth element is the median value of the sorted list.

If the number elements to be sorted are of minimum then sorting process is the most appropriate method for parallel processing. Speed of the sorting network is slowed down by the number of comparators required. Hence a suitable comparator is required along with the best sorting technique has to be formulated for the efficient sorting network. In this work, various effective VLSI hardware implementations of data comparators were done as an economical solution for sorting networks in terms of area speed, power.

The rest of paper is as follow: The different data comparators are discussed in section II. Section-III describes the hardware complexities of each data comparator. Results of each module using Xilinx ISE 9.2i FPGA design suite. are illustrated in section IV. Finally the paper is concluded in section V.
II. VARIOUS DATA COMPARATORS

Comparators are the useful combinational circuits which are used to determine whether the first number is greater or lesser when compared with the second. The comparators are classified into magnitude comparator and data comparator. Magnitude comparator finds out whether the number is greater or lesser. The data comparator finds out the greater value or lesser value.

A. Conventional Bitwise Data Comparator (CBWDC)

The architecture in Fig. 1 comprises of 8 bit comparator, sixteen numbers of 2-1 mux, two buffers each with 8 bit storage[11]. 8- bit data comparator is designed with 2 to 1 multiplexer, buffer and a NOT gate. The first buffer produces minimum value at the output whereas second buffer produces maximum value at the output.

B. Carry Select Logic Data Comparator (CSLDC)

Fig. 2 shows the Structure of 8-bit carry select logic data comparator[11] consists of a half subtractor, seven numbers of full subtractors, two numbers of 8 bit multiplexers and a Not gate. The half subtractor receives the LSB bit of both the inputs and its borrow is input to the series of seven full subtractors which also receives the remaining bits of inputs. The multiplexer which receives the borrow of the full subtractor finds the minimum value and multiplexer which receives the complement of the borrow finds the maximum value.

C. Borrow Look Ahead Logic Data Comparator (BLALDC)

The processing element (PE) is comprised of XOR, AND, OR, AND and NOT gates. There are eight processing elements arranged in series manner whose output is select line for the two eight bit multiplexers[11] is shown in Fig. 3. The LSB PE’s third input is connected with carry input with logic 0. The multiplexer which receives the output of the MSB PE finds the highest value and the multiplexer which receives complement of the output of the processing finds the minimum value.

D. Multiplexer Based Data Comparator (MUXBDC)

Each Processing Element (PE), is composed of an OR gate, AND gate and a 2 to 1 multiplexer. Output from the PE is the difference value. In the structure shown in Fig. 4, eight processing elements are connected in series manner [11]. Difference output from the MSB PE is given as select input to the two 8-bit multiplexers. The multiplexer with difference as select input finds the minimum value whereas the multiplexer with complement of the difference as select input finds the maximum value.
E. Decoder Based Data Comparator (DE CDC)

The structure of decoder based data comparator shown in Fig. 5, consist of XOR gates, 2-4 decoder, multiplexers and OR gates[11]. XOR gates to the decoder acts as buffers to pass the values of X and Y. XOR which receives X and Y produces enable line and select line to the multiplexer and enable line to the decoder. Among the outputs of the decoder 00 and 11 have no operation because of equality and 01 and 10 are used to find the maximum and minimum value of the comparison.

III. MODIFIED DATA COMPARATORS

A. Modified Multiplexer Based Data Comparator (MMUXBDC)

The Fig. 7 shows the structure of modified multiplexer based data comparator. It consists of eight numbers of processing elements (PE), two 2 to 1 multiplexers and an inverter. The processing element is a 4 to 1 multiplexer which receives the first and fourth input as carry-in input. The 2 to 1 multiplexer which receives the MSB PE’s output as select line receives finds the maximum value of output and the 2 to 1 multiplexer which receives the complement of the output as select line finds the minimum value of the input data.

B. Modified Decoder Based Data Comparator (MDECBDC)

Structure of modified decoder based data comparator is given in Fig. 8. This is composed of eight numbers of Processing Elements (PE), two numbers of 2 to 1 multiplexers and a NOT gate. The processing element is a 3 to 8 decoder. The 2 to 1 multiplexer which receives the MSB PE’s output as select line finds the maximum value and the 2 to 1 multiplexer which receives the complement of the output as select line finds the minimum value among the available inputs.
C. Modified Twos Complement Based Data Comparator (MTCBDC)

Fig. 9 Structure of Modified Twos Complement Based Data Comparator

Structure of Modified Twos Complement Based Data Comparator given in Fig. 9. Modified twos complement based data comparator which consists of eight numbers of Full Adders (FA), eight numbers of XORs gates, two numbers 2 to 1 multiplexers and an inverter. The FAs receive previous carry, complement of the second input and the first input and computes. The LSB FA receives the first input as 1. Carry out from the MSB FA is given as select input to the 2 to 1 multiplexer that produces the low output and its complement is given to the 2 to 1 multiplexer that produces high output.

IV. RESULTS AND DISCUSSION

A. Simulation results

The Simulation is done using ModelSim SE PLUS 6.5 and synthesis is executed using Xilinx ISE 9.2i FPGA design suite. The architectures are targeted for device (Devices xa6slx4-3-csg225).

Fig. 10 Simulation output of Modified Multiplexer Based Data Comparator

Simulation output of Modified Multiplexer Based Data Comparator is given in Fig. 10. In this simulation output a and b represents the two inputs and low and high represents the minimum and maximum among the two.

Fig. 11 Simulation output of Modified Decoder Based Data Comparator

Simulation output of Modified Decoder Based Data Comparator is given in Fig. 11. In this simulation output x and y represents the two inputs and low and high represents the minimum and maximum among the two.

Fig. 12 Simulation output of Modified Twos Complement Based Data Comparator

Simulation output of Modified Twos Complement Based Data Comparator is given in Fig. 12. In this simulation output a and b represents the two inputs and low and high represents the minimum and maximum among the two.

B. Hardware Comparison

The hardware requirement of the six different existing comparators and the three modified versions of the comparators are analysed in terms of total number of 4 input LUTs used, number of bonded IOBs, total equivalent gate count for design, maximum combinational path delay and total memory usage. The hardware comparisons of nine different comparators are listed in Table 1. From the analysis MTCBDC needs the minimum total equivalent gate count for design and next is BLALDC.
Hence area efficient requirement is possible with the help of MTCBDC. Maximum combinational path delay is for the same MTCBDC. Total number of 4 input LUTs used is 24 for both MTCBDC and BLALDC. But when the number of bonded IOBs and total memory usage in kilobytes are considered MTCBDC shows larger requirement. Whereas MMUXBDC and MDECBDC show less memory requirement. Memory efficient architectures may be designed with these two types of comparators.

### Table-1: Hardware comparison for the nine different types of comparators

<table>
<thead>
<tr>
<th>Parameters</th>
<th>CBW BDC</th>
<th>CSLDC</th>
<th>BLAL DC</th>
<th>MMUX BDC</th>
<th>DEC BDC</th>
<th>TCBDC</th>
<th>MDECBDC</th>
<th>MTC BDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total number of 4 input LUTs used</td>
<td>28</td>
<td>32</td>
<td>24</td>
<td>26</td>
<td>33</td>
<td>30</td>
<td>26</td>
<td>26</td>
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<tr>
<td>Number of bonded IOBs</td>
<td>32</td>
<td>48</td>
<td>33</td>
<td>33</td>
<td>52</td>
<td>34</td>
<td>33</td>
<td>33</td>
</tr>
<tr>
<td>Total equivalent gate count for design</td>
<td>174</td>
<td>192</td>
<td>147</td>
<td>159</td>
<td>358</td>
<td>183</td>
<td>159</td>
<td>159</td>
</tr>
<tr>
<td>Total memory usage (kilobytes)</td>
<td>472348</td>
<td>473240</td>
<td>473284</td>
<td>472320</td>
<td>473238</td>
<td>473204</td>
<td>472316</td>
<td>472316</td>
</tr>
</tbody>
</table>

V. CONCLUSION

For all the six existing comparators and three modified comparators the Simulation is done using ModelSim SE PLUS 6.5and synthesis is executed using Xilinx ISE 9.2i FPGA design suite. The nine architectures are targeted for device (Devices xa6slx4-3-csg225). From the results MTCBDC is the minimum area required architecture with maximum combinational path delay and also with minimum number of LUTs used. The drawback of this architecture is the maximum memory requirement. The MMUXBDC and MDECBDC architectures are suitable for memory efficient design. Hence this work all the nine comparators are implemented and their efficiencies in terms of area, speed are listed.

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