

Fractional-Order PID Controlled Unified Power Quality Conditioner System with Enhanced Response



SK. Abdul Pasha, N. Prema Kumar

Abstract: Recently, 'UPQC' has been urbanized as a FACTS controller near weak buses and buses with non linear loads. 'UPQC' can improve receiving end voltage and provide time harmonics to the load. The UPFC and 'UPQC' systems are compared to find a better FACTS controller. The recommended closed loop 'UPQC' framework is to augment dynamic response of 'UPOC' system using FOPID controller. Simulink replicas are extended for PI & FOPID controlled 'UPQC' frameworks. The denouements of PI&FOPID based 'UPQC' frameworks designate that voltage retaliation of FOPID is predominant to the denouement of PI managed 'UPQC' system. The investigation denotes that FOPID 'UPQC' framework has diminished settling time& steady state error.

Index Terms: Active filters, Dynamic Voltage Restorer, "UPOC", Total Harmonic Distortion, Wind Generator.

I. INTRODUCTION

It is the aspiration of the electric value to allocate its client with a pure sinusoidal voltage of rather a fixed enormity & frequency. The generator's that create the electric power produce a very close estimate to a sinusoidal signal. The preparation, design & maneuver of industrial & commercial power systems need numerous analysis to help in the assessment of the initial and future system performance, framework trust worthy, well being and the aptitude to produce with production & working needs.

Occasionally perverted wave shapes will be examined to investigative the symphonious parts of the Wave frames. Sinking voltage & current waveforms to satisfactory levels have been an issue in control framework plan from the close to the starting days of substituting current. Still, there are loads & appliances on the framework, which contain nonlinear attributes&consequence in harmonic contents of both the voltage & current signals. As supplementary nonlinear loads are imported inside a resource, these wave shapes get more warped. In the latest power framework owing to the extended exploit of nonlinear loads, it has fledged to be essential to ascertain criteria for blocking PQ

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problems.

These effort origination drops in system efficiency, poor power factor, non-operative electronic devices and fall in to the equipment mean days time. The DC loads inject the frequency distortion current through the system network and then distorts the voltage waveform. This inaccurate voltage waveform damage other loads system. To get away from this trouble &to defend the weights from misrepresentation, the harmonic constituents of the voltage & current ought to be reimbursed. As a outcome of inactive filters, the issue can be diminished but these have numerous annoyances for instance fixed compensation, more size, resonance problems.

To rise exceeding difficulty, the SAF were utilized with inactive filters [*1] [*2], however this technique does not diminish the potential harmonics. So as to handle voltage & current harmonic effects at once, one of the classiest device i.e., Unified Power Quality Conditioner ('UPQC') has been established [*2] [*3]. In section3, a two bus system deprived of 'UPQC' and with 'UPQC' is exhibited & fabricated and also relative analysis of simulation results is presented.

A. Problem Formulation

The exceeding writing doesn't covenant with comparison of UPFC and 'UPQC'. Closed loop control of 'UPQC' using FOPID controller is not reported in the literature. This work has proposed FOPID for the power quality improvement. It is required to improve the dynamic response of 'UPQC' based TBS using FOPID controller.

$$P = \frac{v_1 v_2}{x} \sin \delta \qquad (1.1)$$

$$Q = \frac{1}{x} (v_2 \cos \theta - v_1)$$
(1.2)

'UPOC' CONFIGURATION II.

'UPQC' framework must be organized in arrangement and shunt association of the shunt dynamic power channels allocating a typical DC connect. The 2dynamic power channels have more capacities. Arrangement capacitor is worked at a illicit voltage source to contain & separate voltage harmonics; similar case shunt capacitor goes about to a controlled current harmonic. This paper introduces a flat out appraisal of UPQC'. The Basic model of UPQC' is introduced in figure 1.



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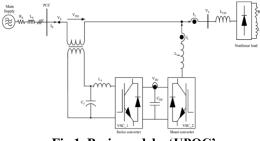


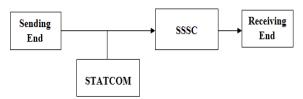
Fig.1. Basic model o 'UPOC'

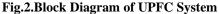
It reveals the essential arrangement of basic 'UPOC' which has 2 voltage source inverters: one works as an arrangement APF and second one works as shunt APF, which is coupled consecutive through dc interface capacitor. The arrangement APF that is connected to the source and purpose of association utilizing three single stage arrangement transformers have the ability of repaying the voltage THD, voltage flicker & humanizing voltage guideline[4]. A little pace aptitude capacitor filter is united diagonally to the derivative of each series transformers to abolish the elevated switching ripple contented in the series APF infused voltage[*5].

The shunt APF has the ability to stifle the present THD, remunerating responsive power, off putting arrangement present and control of the DC interface voltage among APF''s equally[4]. The SAPF is associated during a little evaluated limit inductive channel in characterize to expel the high exchanging swell savored the experience of the shunt APF infused current. Synchronize control approach for 'UPOC' in 3stage; 4wire frame work was given by Yong [5]. Improving Electric PQ utilizing 'UPQC' was given by Khadkikar [6] [8].

III. SYSTEM CONFIGURATION

A. Block Diagram





Schematic representation of UPFC system is delineated in Fig.2. A large battery is used to charge the capacitor of the STATCOM. The UPFC is a merge of STATCOM&SSSC. The STATCOM will deliver component of reactive power obliged by line& load.

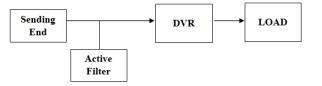


Fig.3.Block Diagram of UPQC System

The schematic presentation of 'UPQC' system block model is delineated in Fig.3. The Active Filter at the sending end supplies harmonics required by the nonlinear load. DVR injects voltage to improve the receiving end voltage.

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B. Analysis of 'UPQC' System

Procuring the values of V₁, I₁& frequency of MOSFET provides the design. Based on obligatory capacitor voltage, the duty ratio is estimated utilizing the equation

$$V_0 = \frac{\mathbf{V_1}}{(\mathbf{1} - \mathbf{a})} \tag{2.1}$$

Effectiveness of the converter to calculate the output current is

n

ΛV

$$= \frac{v_a l_a}{v_1 l_a} \tag{2.2}$$

The values of L & C are calculated by assuming $\Delta I \& \Delta V$ are

$$\Delta V = \frac{\Psi_{I} D}{fL}$$
(2.3)
$$\Delta I = \frac{I_{a} D}{fC}$$
(2.4)

Voltage to be infused is identical to IZ. The AF is intended to provide 5^{th} harmonic. The value of C₅ is assumed and L₅ is calculated with formula

$$f_5 = \frac{1}{2\pi (L_5 C_5)^{\frac{1}{2}}}$$
(2.5)

Pulse width for switches of DVR inverter is $\frac{T_0}{2}$. Pulse width for switches of AF inverter is $\frac{T_5}{2}$. The overhead information does not convenient with power quality enhancement in Wind generation based two bus system utilizing 'UPQC'. This effort recommends 'UPOC' for the PO enhancement in the multi bus system. The exceeding writing don't compare the response of PI &FO-PID controlled 'UPQC' systems. This work recommends FO-PID for the control of 'UPQC' system.

IV. SIMULATION RESULTS

Simulink setup of 2bus system-with UPFC" is delineated in Fig4.The comparison of TBS with Unified Power Flow Conditioner and 'Unified Power Quality Conditioner' for identical load &identical sending end voltage is given in Table 1. The comparison of UPFC and 'UPQC' simulation outcomes designate that the receiving end voltage, true power and imaginary powers are elevated with 'UPQC'. Real power increases from 1.31 to 1.72MW. Reactive power increases from 0.8 to 0.95MVAR. Voltage and current THD contents are diminished using 'UPQC'. Voltage THD content is diminished from 8.8% to 3.6% using 'UPQC'. Current THD content is diminished from 7.8% to 2.6 % using 'UPQC'.

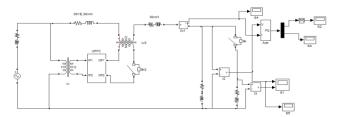


Fig4." Simulink setup for 2bus system with UPFC"



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PQ devic	V(volt s)	P (MW)	Q(MVA R)	V-TH D	I -THD
es UPF C	8200V	1.315	0.803	8.86%	7.83%
UPQ C	9920V	1.721	0.957	3.63%	2.76%

Table1: Comparative study of V, P, Q&THD with UPFC & 'UPOC'

A. Closed loop 'UPQC' system with PI-controller:

Block diagram model of PI controlled 'UPQC' is given in Fig5.The receiving end voltage is related with a reference voltage. The flaw is pragmatic to the comparator across a PI controller. The yield of comparator updates the pulse width useful to 'UPQC'. The transfer function of PI is as follows: According to Ziegler Nicholas Method,

$$T(S) = K_p + \frac{\kappa_i}{s}$$

Delay time (L) = 0.1

Rise time (T)
$$= 0.2$$

The values of K_p and K_i are designed as follows: $K_p = \frac{T}{L}$,

$K_i = 1.6L = 1.6x0.1 = 0.16$

The circuit layout of the closed-loop UPQC with PI controller is delineated in Fig6. The Receiving end peak voltage of PI controlled 'UPQC' system is delineated in Fig7 &its value is1*10⁴V.The RMS output voltage of PI controlled 'UPQC' system is delineated in Fig.8 &its value is 6700V. The reduction in voltage is scrutinized as a outcome of the addition of extra load. The increase in voltage is due to injection of voltage by 'UPQC'. The Real power of PI controlled 'UPQC' system is delineated in Fig.9 and its value is 4*10⁵MW. The reactive power of PI controlled 'UPQC' system is delineated in Fig.10 and its value is 6*10⁴MVAR. The increase in reactive power is due to the injection of voltage.

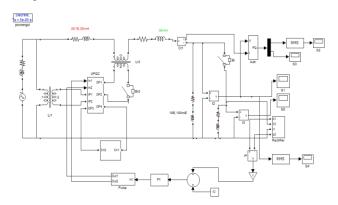


Fig.5.Circuit layout of closed loop UPQC system with PI controller

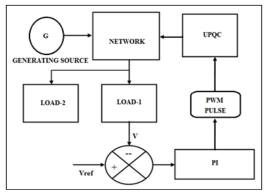


Fig.6.Block diagram of PI controlled UPQC system

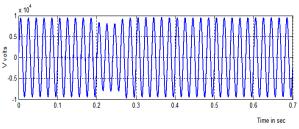


Fig.7.Receiving end voltage of PI controlled 'UPQC'

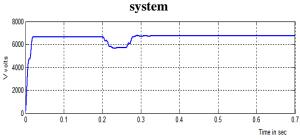


Fig.8.RMS receiving end voltage of PI controlled 'UPQC' system

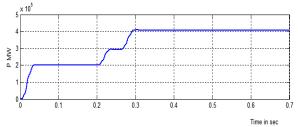


Fig.9.Real power of PI controlled 'UPQC' system

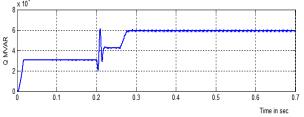


Fig.10.Reactive power of PI controlled UPQC system



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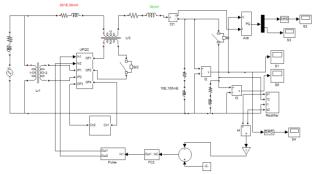


Fig.11.Circuitdiagram of closed loop UPQC system with FO-PIDcontroller"

B.Closed-loop UPQC system with FOPID controller

The drawback of PI is appropriate for linear frameworks &it has sluggish dynamic response. Hence, FOPID may be substituted with PI. The transfer function of FOPID is as follows:

$$T(S) = K_p + \frac{\kappa_i}{s^m} + S^n$$

The values of Kp &K_i are intended as follows:

$$*K_{p} = \frac{T}{L}$$
,
Delay time (L) = 0.1
Rise time (T) = 0.2
 $K_{i} = 1.6 L = 1.6x0.1 = 0.16$
 $K_{d} = 0.6 L = 0.6x0.1 = 0.06$

Circuit diagram of FO-PID controlled 'UPQC' is given in Fig.11. The receiving end voltage is related with a reference voltage. The flaw is pragmatic to the comparator across a FO-PID controller. The block-diagram model of the closed loop UPQC with FOPID-controller is delineated in Fig.12.The receiving end voltage of FOPID controlled 'UPQC' system is delineated in Fig.13 and its value is 1*10⁴V. The RMS receiving end voltage of FOPID controlled 'UPQC' system is delineated in Fig.14 and its value is 6700V. The reduction in voltage is due to the addition of extra load. The increase in voltage is due to injection of voltage by 'UPQC'. The Real Power of FO-PID controlled 'UPOC' system is delineated in Fig.15 and its value is 4*10⁵MW. The reactive power of FO-PID controlled 'UPQC' system is delineated in Fig.16 and its value is 4.5*10⁴MVAR.

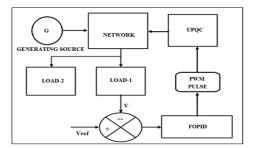


Fig.12.Block diagram of FO-PID controlled 'UPQC' system

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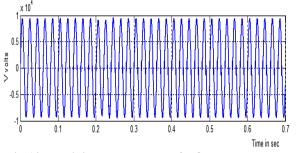


Fig.13.Receiving end voltage of FOPID controlled 'UPQC' system

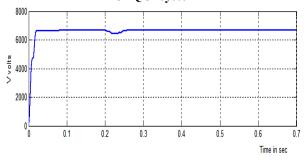
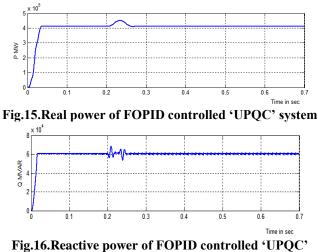


Fig.14.RMS receiving end voltage of FOPID controlled 'UPQC' system



system

The correlation of Time domain parameters is given inTable2.By using FO-PID controller, the peak time is diminished from0.25sec to 0.23sec;Risetime is diminished from 0.23sec to 0.21sec;settling time is diminished from 0.30 sec to 0.24 sec;steady state error is diminished from 5.8V to 2.6V.Comparison of time responses for PI &FO-PID" is given in Fig.17.

 Table 2: Comparison of Time domain parameters of UPQC with PI&FOPID controllers

Type of Controller	Rise time(s)	Peak time (s)	Settling time (s)	Steady state error (V)
РІ	0.23	0.25	0.30	5.8



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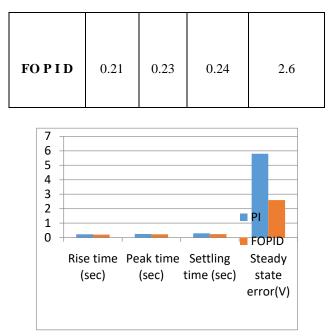


Fig.17.Comparison of time responses for PI &FOPID systems

V.CONCLUSION

The 'UPQC' system is successfully designed modeled, by utilizing MATLAB SIMULINK.'UPQC has improved

receiving end voltage and provided time harmonics to the load. The UPQC systems in closed loop with PI &FO-PID controllers are simulated and the outcomes are given. The steady state error in receiving end voltage is diminished from 4.53V to 1.78V. Therefore, FOPID controller based 'UPQC' system may be a feasible substitute to the existing 'UPQC' system. The diminution in steady state error is elevated in terms of FO-PID controlled system.

The settling time is diminished from 0.35Sec to 0.33Sec. The benefits of the recommended system are diminution in steady state error & settling time. The negative aspect of 'proposed 'UPQC' system' is it needs two inverters.

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