

Low Power AVLS-TSPC based 2/3 Pre-Scaler

Anirvinnan P., Vaishnavi S Parashar, D. Aneesh Bharadwaj, Premananda B.S.



Abstract: The technology has grown at an ultra-fast pace along with the world. Small devices with less power and high efficiency are in demand. As the circuit size gets smaller, the power requirement increases due to a greater number of transistors. A pre-scaler is a circuit which reduces the high frequency signal to a low frequency signal by integer division. A new approach to low power pre-scaler is proposed in this paper, which is an add-on to the conventional pre-scaler circuit. A true single-phase clock (TSPC) circuit reduces the skew problems in the clock and is used to realize latches and flip-flops. The objective of low power is fulfilled by incorporating the Adaptive Voltage Level Source (AVLS) to TSPC based circuit. The proposed AVLS-TSPC based pre-scaler was analyzed for a frequency of 10 MHz with a supply voltage of 1.8 V for both divide by 2 and 3 modes. The proposed pre-scaler consumes considerably lesser power when compared to that of the existing pre-scaler circuit. The circuits are implemented in 180 nm CMOS technology using Cadence Virtuoso and simulated using Cadence Spectre.

Keywords: AVLG, AVLS, CMOS, Flip-flop, Pre-scaler, TSPC.

I. INTRODUCTION

Frequency synthesizer is an important element in the wireless communication system. The speed of the Frequency synthesizer is determined by that of the pre-scaler and voltage-controlled oscillator (VCO). The pre-scaler is used as a fundamental block in case of a wide-band frequency synthesizer implemented using a phase-locked loop (PLL). In PLL, the high-speed dual-modulus frequency pre-scalers plays an important part [14]. They use a single divider to allow multiple division ratios. The criterion considered for designing pre-scalers are: power, speed and the division ratios. Nowadays, supply voltage and channel length are decreasing rapidly as the process technology reduces. Therefore, pre-scaler must work at low operating voltages and as well as high frequencies. The flip-flops consume 30-50 % of chip energy as it works as an integral part of the clock circuitry [2], thus necessitates the selection of flip-flop designs and the way in which the logic gates are incorporated.

The true single-phase clock (TSPC) has a simpler clock distribution and reduces the number of transistors when compared to a traditional flip-flop.

The clocked CMOS logic [5, 6] which has gained a wide popularity incorporates a non-overlapping pseudo clock containing two phases. Between two pairs of clock signals, there are four clock signals that have to be distributed without any overlap. Issues such as clock skew might come up in such circuits which result in a decrease in the circuit speed [7]. The Clock Skew caused by the clock delay between different logic blocks in a large system can be minimized by reverse clock distribution and the D-latch structure. The dynamic CMOS (TSPC) circuit technique uses a clock signal which is never inverted [9]. As a result, the clock skew problem can be minimized and also clock frequencies of higher values can be achieved.

A single-phase clock is used for the purpose of synchronization. The properties of TSPC are: they occupy less area, no clock skew problem and can work at higher clock frequencies. The above properties improve the performance of the digital system [8]. In addition, designs having lower phase noise can be implemented using TSPC logic. In circuits such as frequency dividers and phase/frequency detectors (PFDs), TSPC technique enables low phase noise. Benefits such as simple and compact clock distribution, high speed, and logic design flexibility can be obtained using the TSPC logic. TSPC reduces the requirement of number of clock signals, the cost of wiring and have no problems regarding phase overlapping.

Today, compact devices with minimum power and maximum efficiency are in demand. But, due to the increased requirement for a high speed and complexity, the power consumption of very-large-scale-integration (VLSI) chips has proportionally increased. Few of the recent low power technologies include Adiabatic logic, Reversible logic [3] and Quantum-dot Cellular Automata (QCA) technology [4]. QCA are realized in nanostructure which requires separate fabrication. Adiabatic circuits reduce power, but occupy large area and delay is also a critical factor [11].

Adaptive voltage level (AVL) is a technique that is being used for the operation of the circuit at low power [7]. The Adaptive Voltage Level at Ground (AVLG) technique is used as a low power application where the potential of ground is raised. Similarly, in case of the AVL at source technique, the potential of the supply is increased in order to reduce the value of total power dissipation. The frequency synthesizers use pre-scalers, similarly the pre-scalers can be designed using TSPC based D flip-flops and basic gates. A normal TSPC based D flip-flop employs dynamic logic because of which toggling is more, resulting in increase of power consumption [7]. Therefore, integrating AVLS in the TSPC based D flip-flop for the design of pre-scalers will reduce the power consumption of pre-scalers.

The rest of the paper is organized as follows. Section II describes the literature review in which different papers were

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analyzed and the particular topics are discussed accordingly. Section III describes the AVL technique which is used for reducing the power consumption of the circuit. Section IV discusses the implementation of TSPC based circuits. Simulation results are discussed in section V along with tables. Finally, the conclusion is presented in Section VI.

II. LITERATURE REVIEW

The pre-scaler is a fundamental block in case of a wide-band frequency synthesizer which is implemented using PLL. Since high frequency input is provided for pre-scalers, the amount of power consumed is very high. This paper proposes the methodologies implemented in order to reduce the power consumption of 2/3 pre-scaler which in turn reduces the power in PLL. Modified PLL reduces the amount of power consumed in a frequency synthesizer.

An N/N+1 dual modulus pre-scaler consists of flip-flops and few other logics which have been implemented using logic gates. Various flip-flop-based architectures have been proposed to improve the operating speed of the dual-modulus pre-scalers. The maximum frequency of operation is limited by the large load capacitance, which is considered to be a major drawback. This drawback leads to increase in the power consumption. To reduce the complexity of the circuit, power dissipation and to increase the speed of operation, methods of dynamic and sequential circuits or logic gates which are clocked such as TSPC, can be used [1].

The various architectures of the 2/3 dual modulus pre-scaler are discussed keeping in mind the delay and power in order to help the designer to select the best architecture for their design specification is provided in [2]. A 2/3 pre-scaler divides the given input frequency of the clock by two or by three depending upon the mode in which it is working, as it works in dual mode. Many techniques such as device sizing, body biasing can be done to decrease the delay and power of the circuit. Four different architectures of pre-scalers were discussed in [2], out of which two of them are based on TSPC D flip-flop and the other two are based on ETSPC D flip-flop.

Bernard et al., [15] proposes a various CMOS TSPC circuits. The TSPC based circuits have proven to be of good performance at higher frequency operations. It describes some significant elements that ought to be considered in the making of a TSPC split output cell library. The characterization of the effects of the fanout and the length of interconnects were analyzed in the paper. Another interesting aspect in terms of VLSI implementation is that the split-output latches are robust when we consider the clock signal degradations. To overcome the Clock Skew problems, the TSPC circuit is operated with one clock signal. TSPC logic circuits exhibit higher switching power [6].

Flip-flops are being used in the applications where the devices which are small in size, having a demand for maximum efficiency and minimum power consumption. Data storage, microprocessors are the wide variety of applications in which flip-flops can be used. Anwesha et al. [7] proposed circuit for the TSPC based D flip-flop for low power consumption, where the techniques of AVL and body biasing are being talked about. An AVL technique is usually used to control the circuits either at the supply end (pull-up network) or the ground end (pull-down network) of the circuit. The method of AVL in which the circuit is connected to the supply using a pull-up network is known as the AVLS and correspondingly, the connection of the circuit to the ground using the pull-down network is known as AVLG.

TSPC based D flip-flop can be considered to design pre-scalers, which are used for the implementation of wide band frequency synthesizers. In PLL, the high frequency output of VCO is coupled directly to the pre-scaler. On a larger scale, the power consumption becomes a major issue in the existing architectures. To address this, a new architecture using AVLS technique which reduces the power significantly, is implemented with TSPC.

III. ADAPTIVE VOLTAGE LEVEL

The AVL circuit is constructed using one PMOS and two series connected NMOS, which will result in the reduction of voltage applied to the load circuit. Sleep control signal controls the AVL circuit [7]. When the sleep signal is low, the series connected NMOSs are in OFF state, but the PMOS is in ON state. This results in achieving of full voltage out of the AVL circuit. When sleep signal makes a transition from low to high, this will turn-off PMOS, and turns-on series connected NMOSs.

A. Adaptive Voltage Level Ground

An AVLG consists of a combination of one-NMOS and two-PMOS transistors which are connected in parallel, which becomes the additional control circuit to the existing conventional circuit. A clock, which acts as an input to the circuit is applied to the terminal of the NMOS transistor whereas the PMOS transistors are connected to the ground. Fig. 1 illustrates the basic AVLG circuit [7] which is present at the ground terminal of the conventional circuit. To reduce the amount of power consumed in the circuit, the potential of the ground is elevated. The output varies depending upon the input and the clock is used to prevent any defects during power consumption.

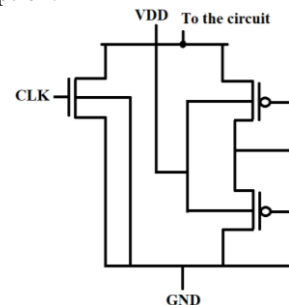


Fig. 1. Basic AVLG Circuit

B. Adaptive Voltage Level Source

AVLS consists of NMOS transistors which are two in number and one PMOS transistors which are connected in parallel. The NMOS transistors are connected to the supply voltage. A clock which acts as an input to the circuit is applied to the terminal of the PMOS transistor whereas the NMOS transistors are connected to the supply. An input clock is provided for the PMOS transistor. Fig. 2 shows the basic AVLS circuit [7] which is used to place in between the supply voltage and the conventional circuits to reduce the supply node potential. The NMOS transistors are forward biased which leads them to ON state, while PMOS toggles from one

state to another due to the clock. This leads to reduction of leakage flowing through PMOS of AVLS and hence reduces the power consumption in the circuit.

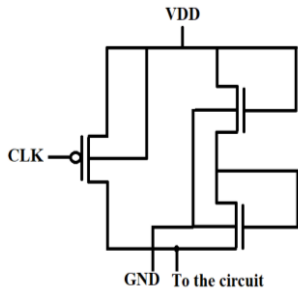


Fig. 2. Basic AVLS Circuit

IV. DESIGN AND IMPLEMENTATION

Implementations of the circuits are performed using Cadence Virtuoso in the 180 nm technology. Simulation of the design is performed using Cadence Spectre. The Cadence Spectre simulation platform contains multiple solvers to allow a designer to move easily and seamlessly between circuit-, block-, and system-level simulation tasks.

A. Realization of TSPC based Latch

A latch is a logic circuit which has two stable states, active high and active low. The latch is used for storage of data. It is a level sensitive circuit having a feedback path which enables it to act as a memory device. Whenever the device is on, it can store 1-bit of information. The latches are used in high speed microprocessor designs which typically employ master slave latches instead of flip flops so that logic can be added between rising and falling clock edges. Fig. 3 shows the circuit of a positive edge triggered 5 transistor TSPC based latch [5, 13]. The 5T TSPC latch is constructed using two PMOS and three NMOS transistors. The latch uses a single phase of clock for synchronization. It consumes lesser area as it uses only 5 transistors, but has more delay. The 6T TSPC latch is constructed using 2 PMOS and 4 NMOS transistors which consume 1 extra transistor area than the 5T TSPC latch [13], as shown in Fig. 4.

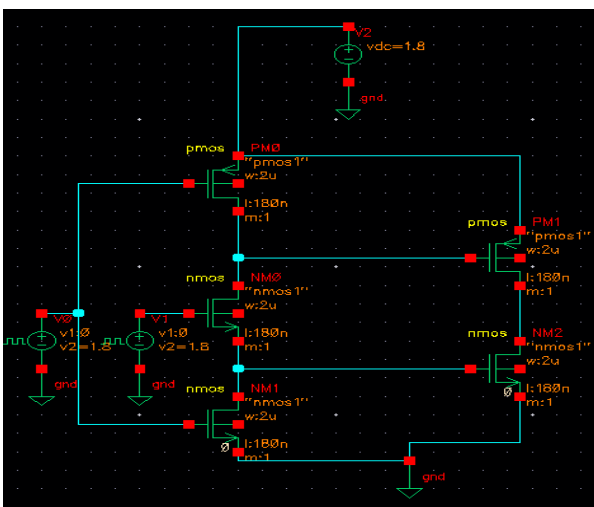


Fig. 3. Circuit of 5T TSPC latch

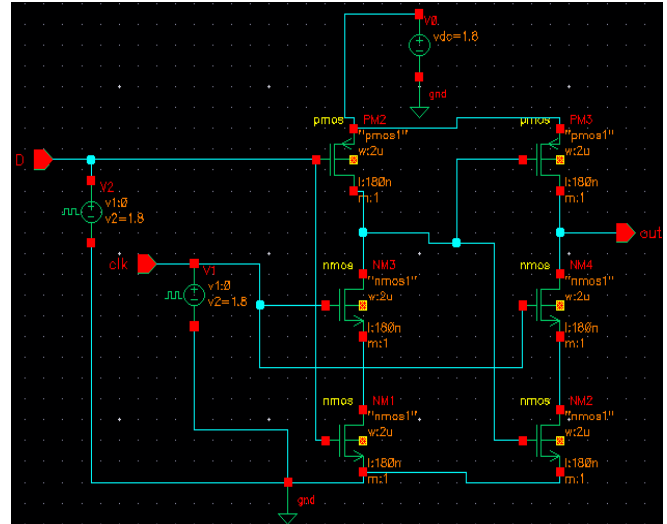


Fig. 4. Circuit of 6T TSPC latch

The computed power and delay of both 5T (Fig. 3) and 6T (Fig. 4) TSPC latch is listed in Table I. The values were calculated for a frequency of 1 MHz. From Table I, it can be inferred that delay of 6T TSPC latch is better than that of the 5T, even though the area of 6T latch may be more than that of the 5T latch.

The body biasing was another aspect considered during the circuit simulations where the circuits were simulated with and without the bulk. Static body biasing is mainly used for decreasing the leakage current which reduces the power consumption. The voltage of the body terminal is altered by applying some potential at it. Fig. 5 shows the basic implementation of static body biasing. A significant difference could be seen in the power consumed between the two which is shown in Table II. From the Table II it can be inferred that body biasing consumes less power, therefore further circuits can be analysed with body biased condition.

The 5T TSPC latch circuit is implemented integrating AVLG and AVLS techniques [7] is shown in Fig. 6 and 7 respectively. The power and delay is calculated and tabulated in the Table III and Table IV. AVLS and AVLG logic were implemented in the 5T latch and were both found to consume less power than the existing architecture. AVLS based latch has higher power efficiency as compared to that of AVLG, which can be analysed Table III. Proposed 6T AVLS TSPC based latch is shown in Fig. 8. The area increases by three transistor count but the power reduces by a factor of two (Table IV), which is very significant in terms of low power applications. Hence, there is a trade-off between the power and area.

Table I. Power and delay analysis of 5T and 6T TSPC latches

Latch	Power (nw)	Delay (ns)
5T TSPC Latch	635.5	3.464
6T TSPC Latch	739.2	2.78

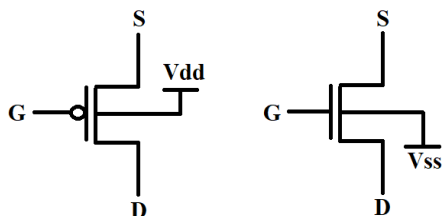


Fig. 5. Static body biasing

Table II. Power and Delay analysis of 5T and 6T latches

Latch	Power (nw)		Delay (ns)	
	With Bulk	Without Bulk	With Bulk	Without Bulk
5T TSPC Latch	484.8	635.5	4.268	3.464
6T TSPC Latch	532.1	739.2	2.89	2.78

Table III. Power and delay analysis of 5T latch using AVL Techniques

TSPC based Latch	Power (nw)
5T Latch	484.8
5T AVLS [7]	233.8
5T AVLG [7]	413

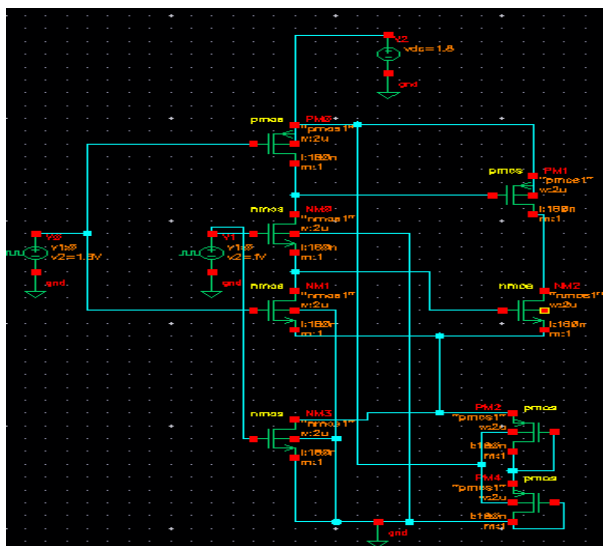


Fig. 6. Circuit of 5T TSPC AVLG latch

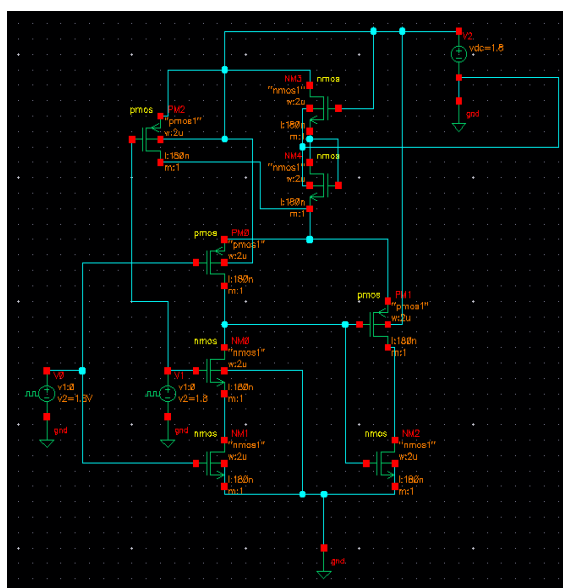


Fig. 7. Circuit of 5T TSPC AVLS latch

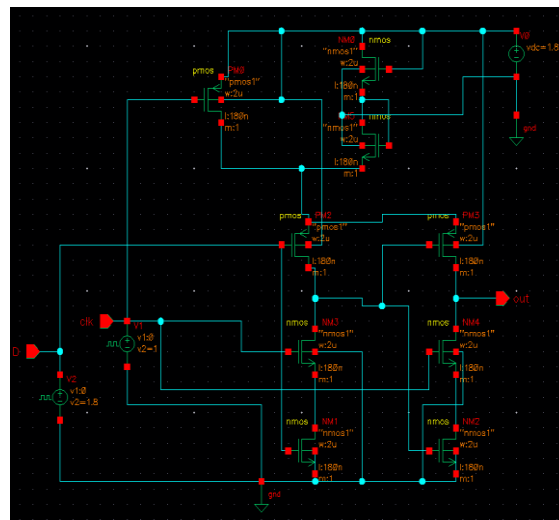


Fig. 8. Circuit of proposed 6T TSPC AVLS

Table IV. Power and Delay analysis of 6T latch using AVL Techniques

TSPC based Latch	Power (nw)
6T Latch	532.1
Proposed 6T AVLS	262

B. Realization of TSPC based D Flip-flop

Flip-flop is a bi-stable element, that is, it has two stable states, and can be used for storing binary data. Flip-flops are sequential elements, which can be used as a data storage element. The flip-flops are always clocked and it is either negative edge or positive edge triggered which concludes that output is affected by the input when the clock goes from high-to-low or low-to-high respectively.

TSPC has been an efficient method to realize high speed flip-flops. Fig. 9 shows the circuit of a TSPC D flip-flop constructed using 11 transistors [12]. The flip-flop consists of 5 PMOS and 6 NMOS for which the power and delay is computed. A proposed 11T TSPC based D flip-flop is constructed using the AVLS technique to reduce the power of 11T TSPC D flip-flop. Fig. 10 shows the proposed circuit of 11T AVLS-TSPC based D flip-flop is constructed by integrating AVLS to the 11T TSPC based D Flip-flop. The power and delay calculated were analyzed with operating frequency of 1 MHz.

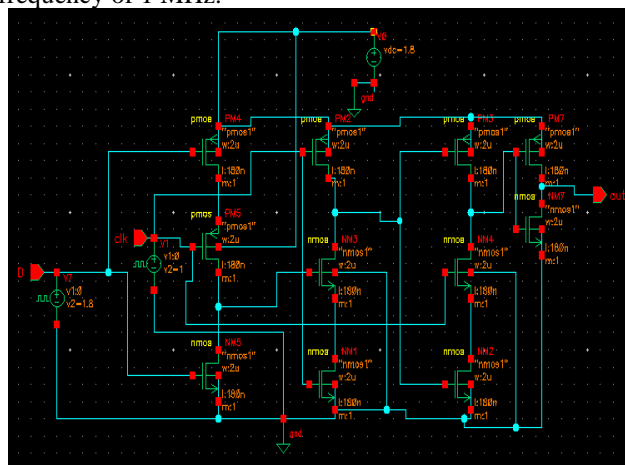


Fig. 9. Circuit of 11T TSPC based D flip-flop

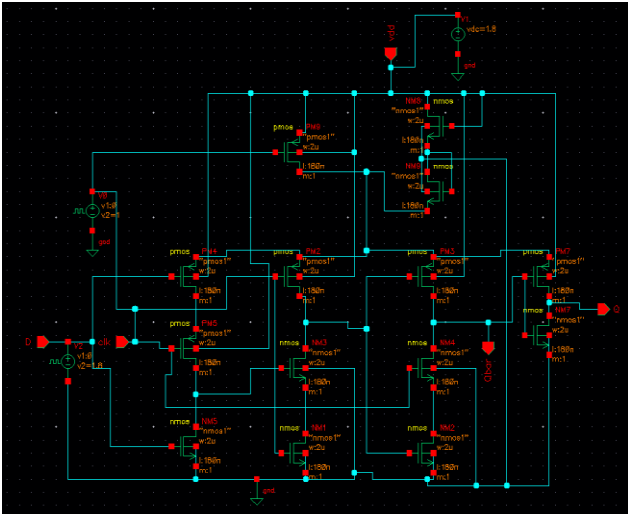


Fig. 10. Proposed circuit of 11T AVLS-TSPC based D flip-flop

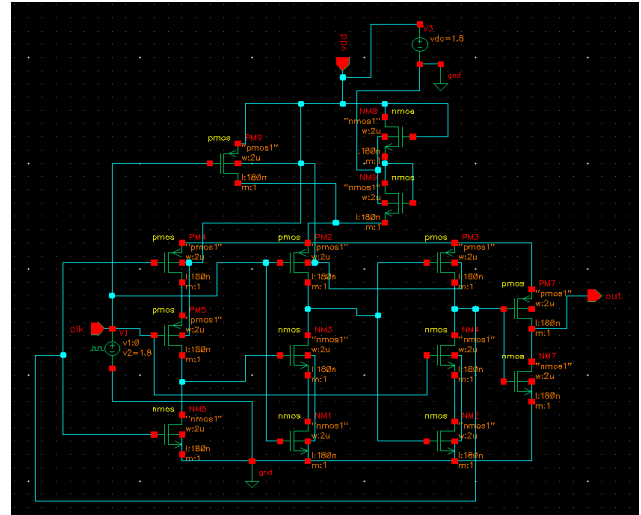


Fig. 12. Proposed circuit of AVLS Divide-by-2 counter

C. Realization of TSPC based Divide-by-2 counter

The applications of counters include practical digital systems, computer applications, scientific instruments, industrial controls and communication systems. Counters are usually clocked at high rate and a counter counting in terms of n-bits has 2n different states. A D flip-flop can be used as binary frequency divider (divide-by-2 counter). Fig. 11 shows the circuit of a TSPC based divide-by-2 frequency divider or a counter [10] where the output which is in inverted form is directly given as a feedback to the data input terminal D. The power and delay were calculated for the same circuit and tabulated. Fig. 12 shows the proposed circuit of Divide-by-2 counter using AVLS technique for which the power and delay was calculated and compared with the power and delay of the conventional circuit.

D. Realization of TSPC based Pre-scaler

An N/N+1 dual modulus pre-scaler consist of flip-flops and other logics implemented using logic gates.

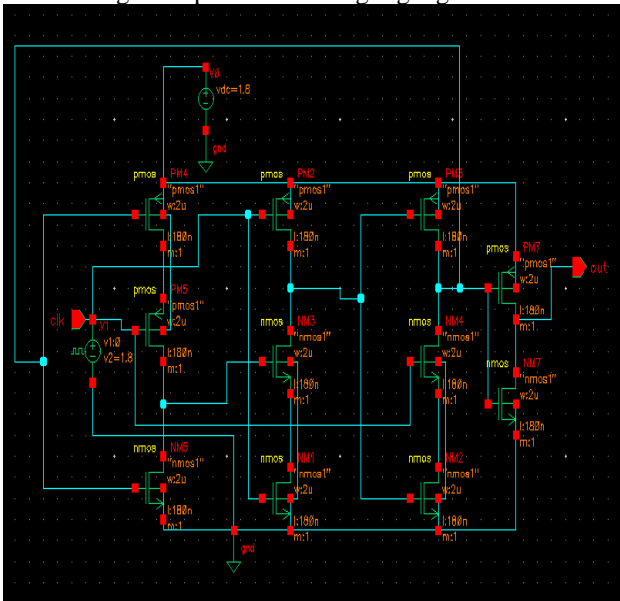


Fig. 11. Circuit of Divide-by-2 counter

The method consists of two new designs of TSPC 2/3 pre-scaler. The improved TSPC based 2/3 pre-scaler in [1] results in low power dissipation and an improved speed in delay. The design consists of two D flip-flops and two NOR gates in between the flip-flops. Fig. 13 depicts this design. The NOR gate drives the DFF1 and DFF2 is driven by another NOR gate. A single NMOS is used to embed the first NOR gate into the 3rd stage of DFF1 while the other NOR gate is embedded into the 1st stage of DFF2. The embedding eliminates the additional stages which are introduced by the digital gates in between DFF1 and DFF2. A reduction happens from 12 to 7 in the number of switching nodes because of this technique, resulting in a reduction of propagation delay and power consumption. Fig. 14 shows the proposed AVLS based pre-scaler. It is implemented by integrating the AVLS technique to the existing circuit, to compute the power and delay of the circuit.

V. RESULTS AND DISCUSSION

The circuits discussed in section IV are implemented using cadence virtuoso and simulated using cadence spectre. The power and delay analysis were made for all the circuits and were compared. The circuits are implemented at an operating frequency of 1 MHz. The power and delay analysis of 11T TSPC based D Flip-flops is listed in Table V. From Table V, it can be inferred that, the power consumption in the proposed circuit is reduced by 50 % as compared to [12], with a marginal increase in area.

The circuits in Fig. 11 and 12 are implemented, followed by the power and delay analysis and values are tabulated in Table VI. From the Table VI, it can be inferred that, the proposed divide by 2 counter consumes lesser power when compared to [10]. The circuits in the Fig. 13 and 14 are implemented, followed by the power and delay analysis and values are tabulated in Table VII. From the Table VII, it can be inferred that, the proposed AVLS TSPC based Pre-scaler consumes lesser power when compared to the reference architecture [1], but there is a marginal increase in delay which can be inferred from Table VII.



Table V. Power and Delay analysis of 11T TSPC D flip-flop using AVL Techniques

Flip-flop	Power (μw)	Delay (ns)
11 T [12]	21.9	3.74
Proposed 11 T AVLS	9.304	4.021

Table VI. Power and Delay analysis of Divide by 2 Counter

Counter	Power (μw)	Delay (ns)
Divide by 2 Counter [10]	44.16	50.39
Proposed AVLS Divide by 2 Counter	1.397	50.96

Table VII. Power and Delay analysis of 2/3 Pre-scalers

Pre-scaler	Divide by 2		Divide by 3	
	Power (μw)	Delay (ns)	Power (μw)	Delay (ns)
Pre-scaler [1]	6.475	50.4	8.895	50.419
Proposed AVLS Pre-scaler	4.525	50.41	4.73	50.429

VI. CONCLUSION

This paper deals with the reduction of power consumption of TSPC based latches, flip-flops, divide by 2 counter and pre-scaler circuits by integrating the AVL technique. In case of AVL, there are two types, namely AVLS and AVLG. AVLS has lesser power consumption compared to that of AVLG and hence, integrated with TSPC. A 11T TSPC circuit without AVLS technology has a power consumption of 21.9 μW with the integration of AVLS it is reduced to 9.304 μW with marginal increase in area. Pre-scaler circuit without AVLS technology in divide by 2 mode consumes power of 6.45 μW with the integration of AVLS there is a decrease of power by 1.95 μW . In case of divide by 3 mode, the power is reduced by 4.1 μW which is almost 50 % less than the power consumed by pre-scaler circuit without AVLS integration.

The AVL technique is not only limited to its use in Pre-scalers, but also can be integrated along with digital circuits such as Adders, Multipliers etc., which will in turn reduce the power consumption of those digital circuits.

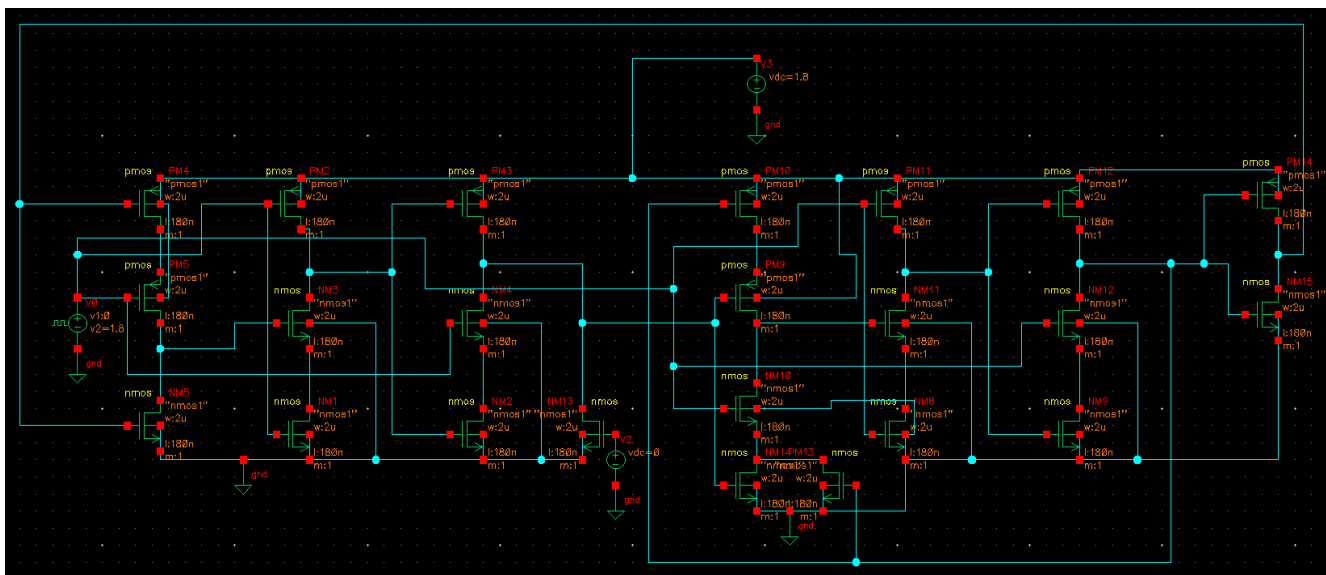


Fig. 13. Circuit of TSPC 2/3 Pre-scaler

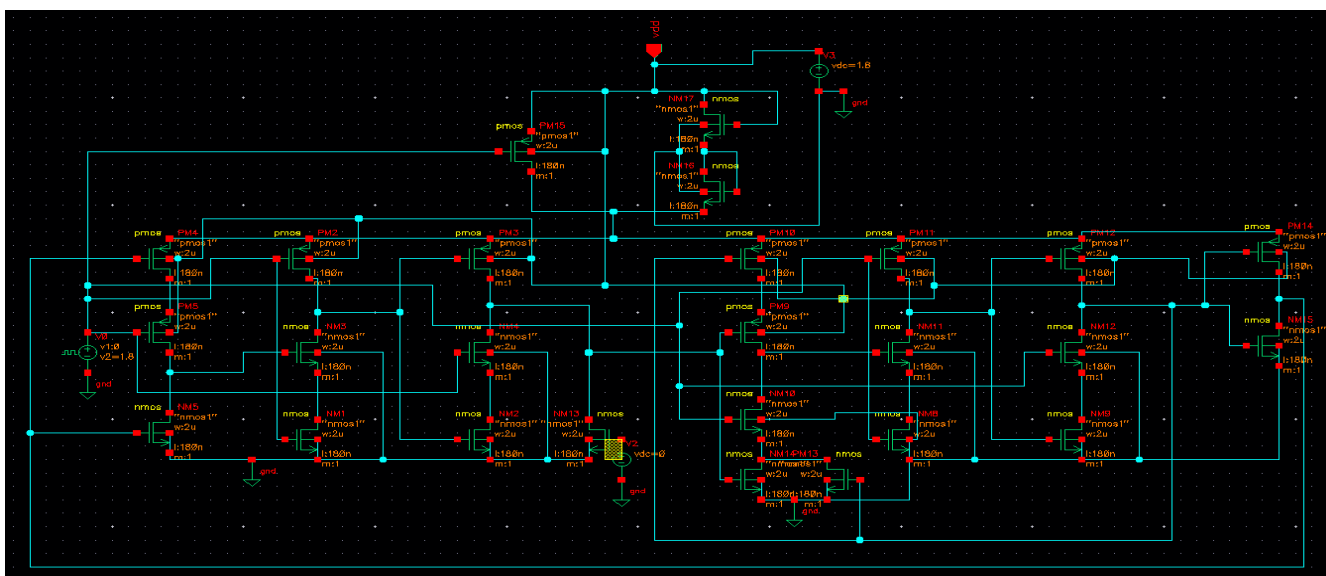


Fig. 14. Proposed circuit of AVLS TSPC 2/3 Pre-scaler

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